FAST 74F13
Schmitt Trigger
Dual 4-Input NAND Schmitt Trigger

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F13	7.8 ns	5.5 mA

DESCRIPTION

The 74F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mv) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than VT_{+MAX}, the gate will respond in the transition of the other input as shown in Waveform 1.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to $+70°C$
14-Pin Plastic DIP	N74F13N
14-Pin Plastic SO	N74F13D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

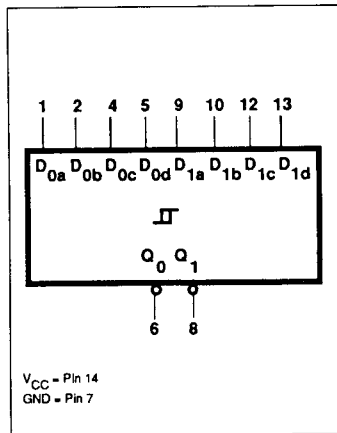**NOTE:**
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

D_{0a}	1	14	V_{CC}
D_{0b}	2	13	D_{1d}
NC	3	12	D_{1c}
D_{0c}	4	11	NC
D_{0d}	5	10	D_{1b}
$\overline{Q}_0$	6	9	D_{1a}
GND	7	8	$\overline{Q}_1$

TOP VIEW

LOGIC SYMBOL

Pins: 1 2 4 5 9 10 12 13

D_{0a} D_{0b} D_{0c} D_{0d} D_{1a} D_{1b} D_{1c} D_{1d}

Q_0 Q_1

6 8

V_{CC} = Pin 14
GND = Pin 7
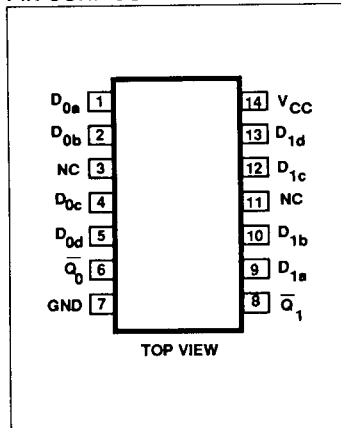
LOGIC SYMBOL (IEEE/IEC)

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1
2
4
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9
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12
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6

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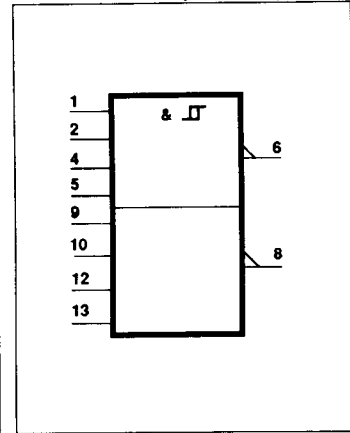
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LOGIC DIAGRAM

V_{CC} = pin 14
GND = pin 7
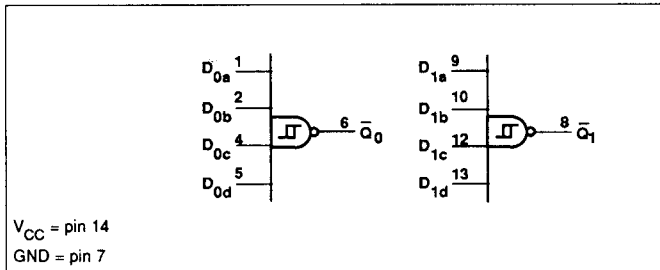
FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{na}	D_{nb}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_K	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} =5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	V_{CC} =5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+}- V_{T-})	V_{CC} =5.0V		0.4	0.8		V
V_{OH}	High-level output voltage	V_{CC} =MIN,	±10%V_{CC}	2.5			V
		V_I=V_{T-MIN}, I_{OH} =MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} =MIN,	±10%V_{CC}		0.30	0.50	V
		V_I=V_{T+MAX}, I_{OL} =MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold	V_{CC} =5.0V, V_I = V_{T+}			0		μA
I_{T-}	Input current at negative-going threshold	V_{CC} =5.0V, V_I = V_{T-}			-350		μA
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} =MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX	V_{IN}=GND		4.5	8.5	mA
		I_{CCL}		V_{IN}=4.5V		7.0	10.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
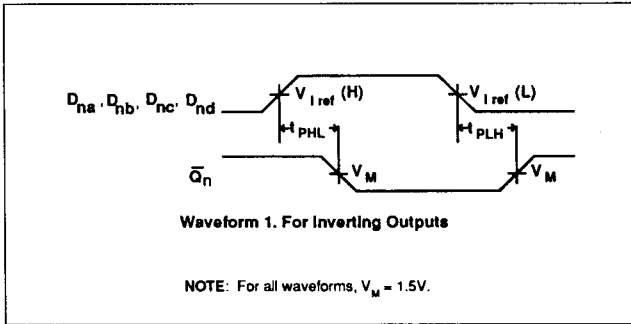
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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	4.0 9.0	5.5 11.0	7.0 13.5	4.0 9.0	8.0 13.5	ns

AC WAVEFORMS

Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS

Test Circuit For Totem-Pole Outputs

Input Pulse Definition

$V_M = 1.5V$

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns