



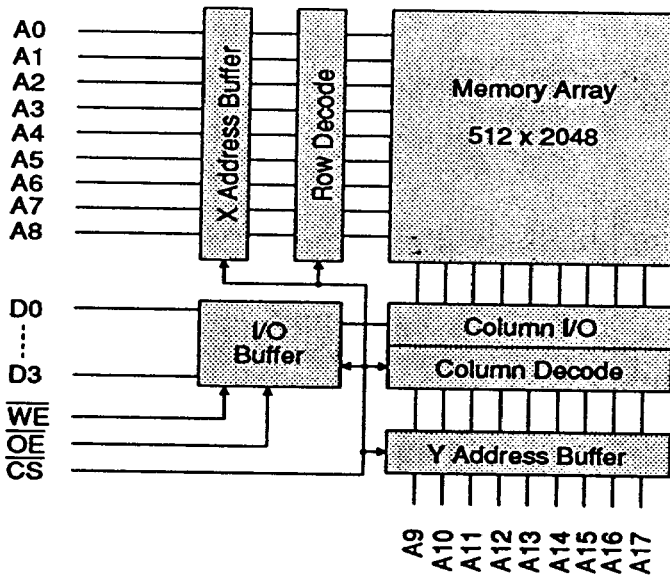
Mosaic Semiconductor Inc.

262,144 x 4 CMOS High Speed Static RAM

Features

- Very Fast Access Times of 25/35/45/55 ns.
- JEDEC Standard 28 pin Footprint.
- VIL™ High Density Package.
- 32 pad LCC and JLCC for surface mount applications.
- Operating Power 350mW(typ.)
- Low Power Standby 100μW (typ.)-L Version.
- 2.0V Data Retention Mode.
- Completely Static Operation.
- Equal Access and Cycle Times.
- Battery Back-up Capability.
- Directly TTL Compatible.
- May be Processed to MIL-STD 883, non-compliant.

Block Diagram



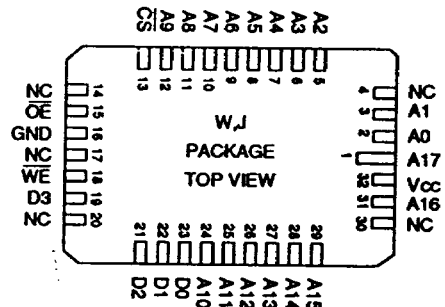
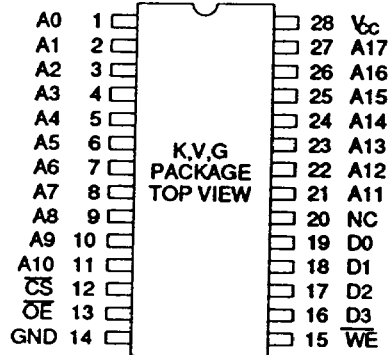
256K x 4 CMOS SRAM

MSM4256-25/35/45/55

Issue 1.4 : October 1992

ADVANCE PRODUCT INFORMATION

Pin Definitions



Pin Functions

- A0-A17 Address Inputs
- D0-3 Data Input/Output
- CS Chip Select
- WE Write Enable
- OE Output Enable
- NC No Connect
- V_{cc} Power (+5V)
- GND Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
28	0.4" Dual-in-Line (DIL)	K	Ceramic	JEDEC
28	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
28	Bottom Brazed Flatpack	G	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	W	Ceramic	ASIC
32	J-Leaded Chip Carrier (JLCC)	J	Ceramic	ASIC

See pages 6,7 for Package dimensions and outlines.
 VIL is a trademark of Mosaic Semiconductor Inc., US Patent No. D316251.

Absolute Maximum Ratings ⁽¹⁾

Voltage on any pin relative to V_{SS} ⁽²⁾	V_T	-0.5 to +7	V
Power Dissipation	P_T	1.0	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
 (2) Pulse width:- 2.0V for less than 10ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (suffix I)
	T_{AM}	-55	-	125	°C (suffix M, MB)

DC Electrical Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 0V$ to V_{CC}	-	-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $V_{IO} = GND$ to V_{CC}	-	-	2	μA
Operating Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{IO} = 0mA$, Min. Cycle, Duty=100%	-	-	120	mA
Standby Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, I/P's static	-	-	40	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$, $0.2V \geq V_{IN} \geq V_{CC} - 0.2V$	-	0.02	2	mA
	-L Version I_{SB2}	As above	-	-	100	μA
Output Voltage	V_{OL}	$I_{OL} = 8.0mA$	-	-	0.4	V
	V_{OH}	$I_{OH} = -4.0mA$	2.4	-	-	V

Typical values are at $V_{CC} = 5.0V$, $T_A = 25^\circ C$ and specified loading.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$)

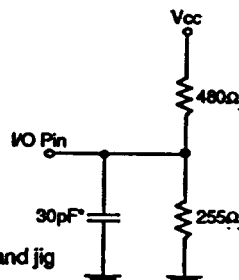
Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	C_{IN}	$V_{IN} = 0V$	-	5	pF
I/O Capacitance:	C_{IO}	$V_{IO} = 0V$	-	10	pF

Note: This parameter is calculated and not 100% tested

AC Test Conditions

Output Load Circuit

- * Input pulse levels: GND to 3.0V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: See Diagram
- * $V_{CC} = 5V \pm 10\%$

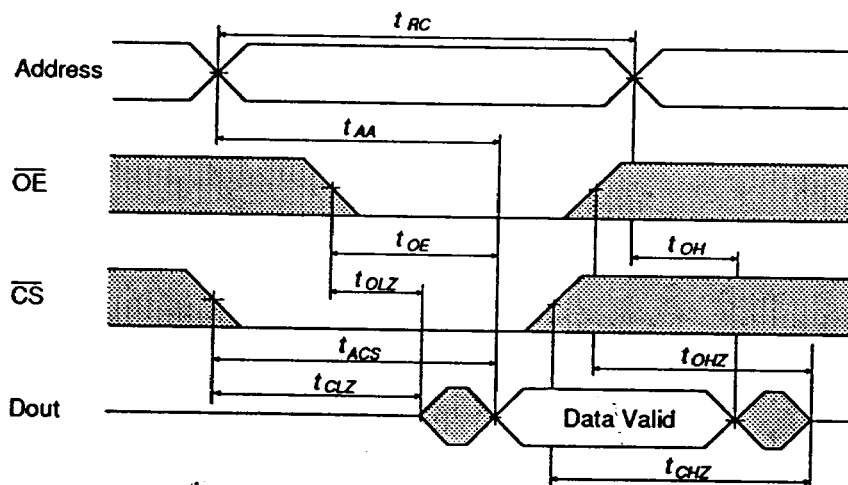


*Including scope and jig

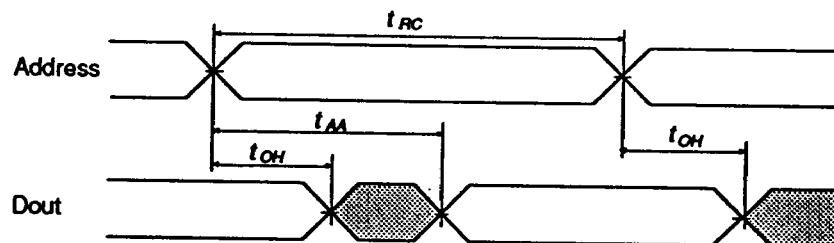
Read Cycle Timing

Parameter	Symbol	-25		-35		-45		-55		Unit	Note
		min	max	min	max	min	max	min	max		
Read Cycle Time	t_{RC}	25	-	35	-	45	-	55	-	ns	
Address Access Time	t_{AA}	-	25	-	35	-	45	-	55	ns	
Chip Select Access Time	t_{ACS}	-	25	-	35	-	45	-	55	ns	
Output Enable to Output Valid	t_{OE}	-	12	-	15	-	18	-	18	ns	
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	5	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	5	-	ns	1
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	12	0	15	-	18	-	18	ns	1
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	0	10	0	10	ns	1

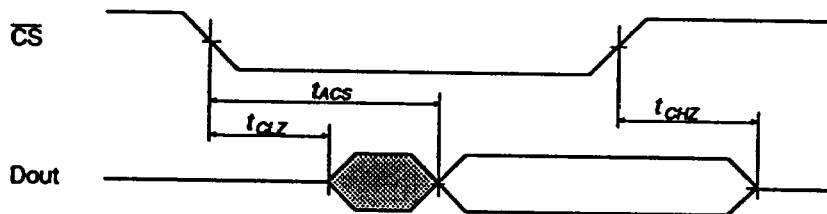
Read Cycle Timing Waveform(1) ^(1,2)



Read Cycle Timing Waveform (2) ^(1,2,3,5)



Read Cycle Timing Waveform (3) ^(1,2,4,5)



Notes:

1. This parameter is not 100% tested.
2. \overline{WE} is High for Read Cycle.
3. Device is continuously selected, $\overline{CS}=V_L$.
4. Address valid prior to or coincident with \overline{CS} transition Low.
5. $\overline{OE}=V_L$.

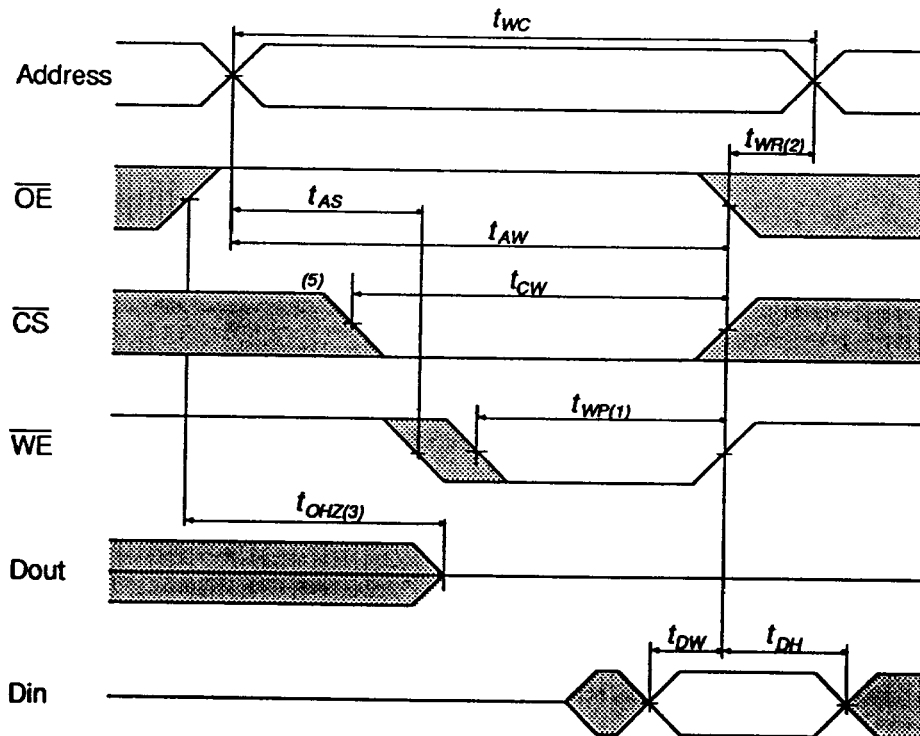
Write Cycle Timing

Parameter	Symbol	-25		-35		-45		-55		Unit	Note
		min	max	min	max	min	max	min	max		
Write Cycle Time	t_{RC}	25	-	35	-	45	-	55	-	ns	
Chip Selection to End of Write	t_{CW}	17	-	25	-	32	-	32	-	ns	
Address Valid to End of Write	t_{AW}	20	-	30	-	40	-	50	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	17	-	25	-	32	-	32	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns	
Write to Output in High Z	t_{WHZ}	0	15	0	20	0	25	0	30	ns	1
Data to Write Time Overlap	t_{DW}	15	-	20	-	25	-	30	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns	
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	0	10	0	10	ns	1
Output Active from End of Write	t_{OW}	0	-	0	-	0	-	0	-	ns	1

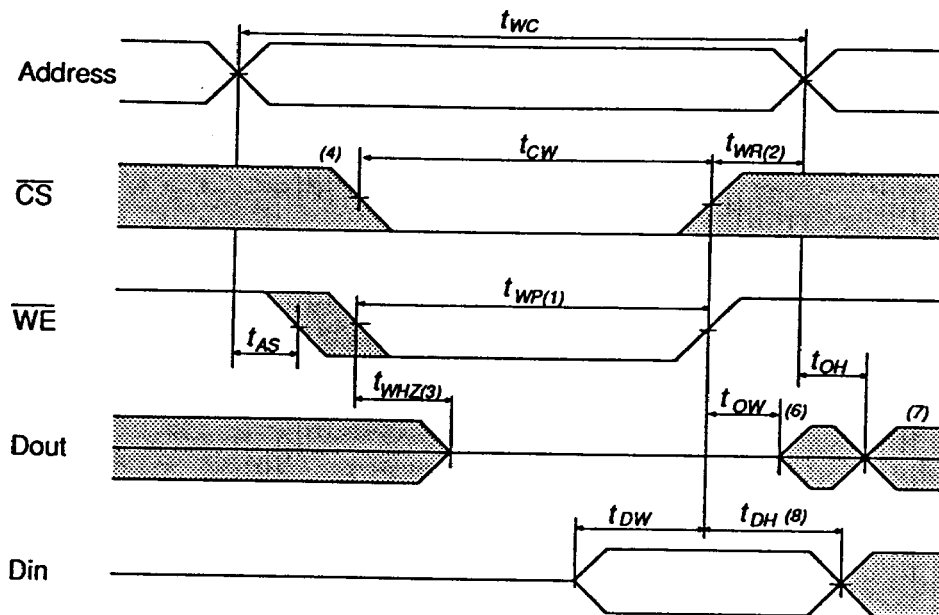
Notes:

1. This parameter is not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform ⁽⁵⁾



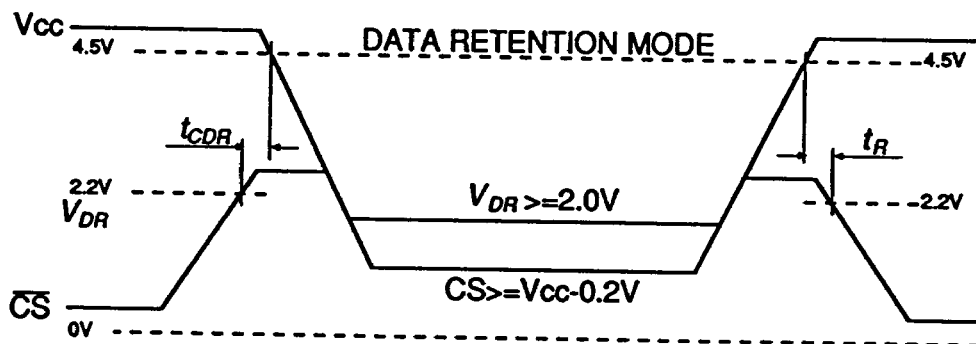
Notes:

1. A write occurs during the overlap (t_{WR}) of a low \overline{CS} and a low \overline{WE} .
2. t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
4. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, O/P's remain in a high impedance state.
5. \overline{OE} is continuously low. ($OE=V_i$)
6. Dout is in the same phase as written data of this write cycle.
7. Dout is the read data of next address.
8. If \overline{CS} is low during this period, I/O pins are in the output state. I/P signals out of phase must not be applied to I/O pins.

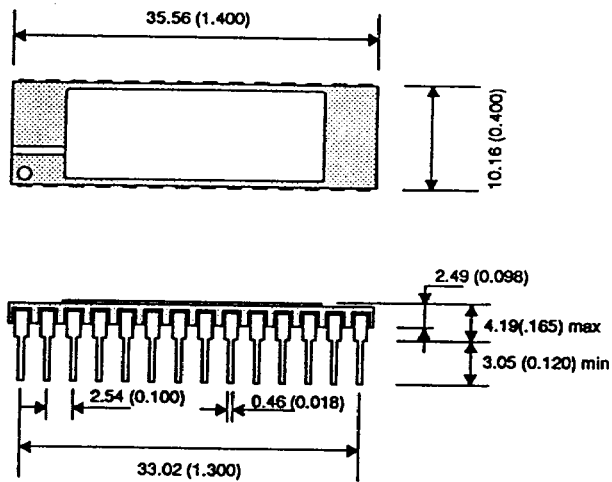
Low V_{CC} Data Retention Characteristics - L Version Only ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} > V_{CC} - 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0V, \overline{CS} \geq V_{CC} - 0.2$	-	2	100	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

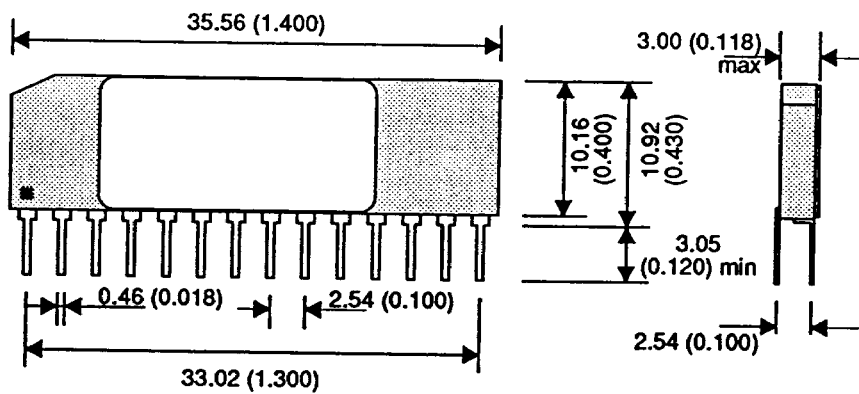
Low V_{CC} Data Retention Timing Waveform



28 Pin 0.4" Dual-In-Line (DIL) - ('K' Package)

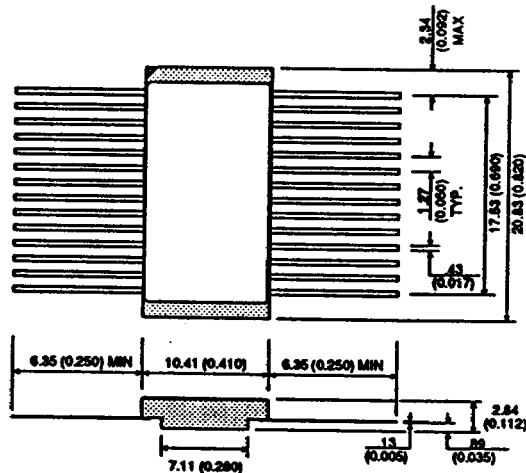


28 Pin 0.1" Vertical-In-Line (VIL) - ('V' Package)

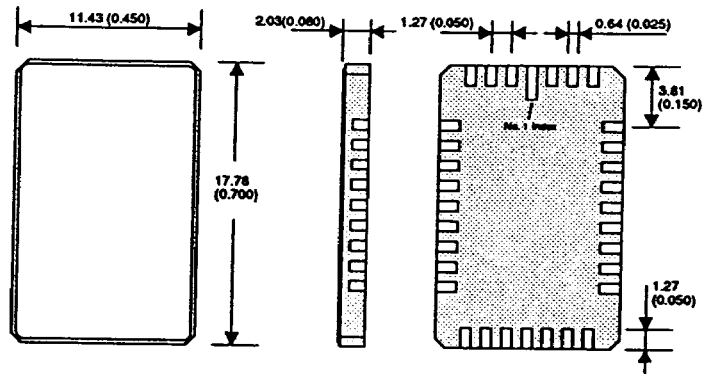


Dimensions in mm (inches).
Tolerance on all dimensions ± 0.254 (0.010).

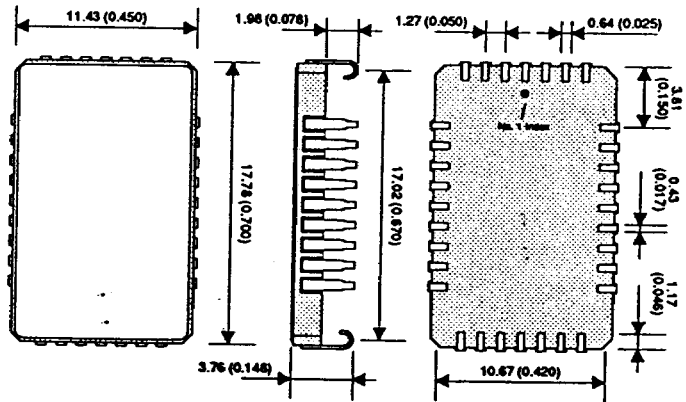
28 Pin Bottom Brazed Flatpack - ('G' Package)



32 Pad Extended Leadless Chip Carrier (LCC) - ('W' Package)



32 Pin Extended 'J' Leaded Chip Carrier (JLCC) - ('J' Package)



Dimensions in mm (inches).
Tolerance on all dimensions ± 0.254 (0.010).

Ordering Information

MSM4256KLMB-25

<p>Speed</p> <p>Temp. range/screening</p> <p>Power Consumption</p> <p>Package</p>	<p>25 = 25 ns</p> <p>35 = 35 ns</p> <p>45 = 45 ns</p> <p>55 = 55 ns</p> <p>Blank = Commercial Temp.</p> <p>I = Industrial Temp.</p> <p>M = Military Temp.</p> <p>MB = Processed to MIL-STD 883 Method 5004, non-compliant.</p> <p>Blank = Standard Part</p> <p>L = Low Power Part</p> <p>K = 28 Pin 0.4" DIL</p> <p>V = 28 Pin 0.1" VIL</p> <p>G = 28 Pin Ceramic Flatpack</p> <p>W = 32 Pad LCC</p> <p>J = 32 Pad JLCC</p>
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Note: For more information regarding screening levels, contact Mosaic Semiconductor Inc. for a 'Screening Level Applications Note.'



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