1.5A DUAL HIGH-SPEED FET DRIVERS

FEATURES

- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand >0.5A Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected ..... 4 kV
- High Peak Output Current 1.5A
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive Capability ..... 1000 pF in 25 ns
- Short Delay Time ..... <40 ns Typ
- Consistent Delay Times With Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage From 2.4V to V_{DD}
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - With Logic "1" Input ..... 4 mA
  - With Logic "0" Input ..... 400 µA
- Low Output Impedance 7Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Pinout Same as TC426/TC427/TC428
- Available in Inverting, Noninverting, and Differential Configurations

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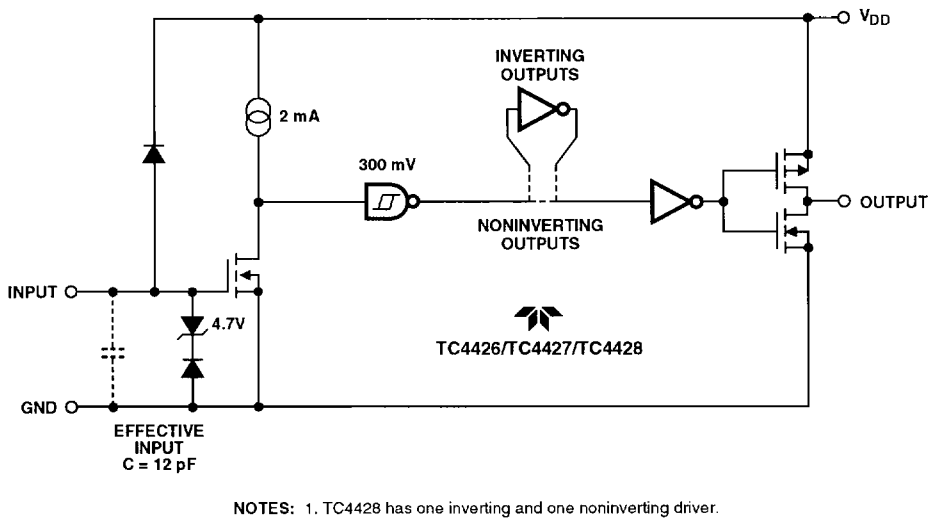
FUNCTIONAL DIAGRAM



NOTES: 1. TC4428 has one inverting and one noninverting driver.
2. Ground any unused driver input.

TC4426
TC4427
TC4428

GENERAL DESCRIPTION

The TC4426/4427/4428 are CMOS buffer/drivers built using Teledyne Components' new Tough CMOS process. They are improved versions of the earlier TC426/427/428 family of buffer/drivers (with which they are pin compatible) and are capable of giving reliable service in far more demanding electrical environments. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4 kV of electrostatic discharge.

In addition, Teledyne now uses a custom-developed molding epoxy for plastic packages which, in tests, produced zero device failures after 10,000 hours in an 85°C–85% R.H. environment, and contains 50% less sodium and chlorine contamination than standard commercial molding compounds, increasing device lifetimes.

As a result, the TC4426/4427/4428 drivers are much easier to use, more flexible in operation, and much more forgiving than any other drivers (CMOS or bipolar) currently available. Because they are fabricated in CMOS, they dissipate a minimum of power and provide rail-to-rail voltage swings to ensure the logic state of any load they are driving.

Although primarily intended for driving power MOSFETs, the TC4426/4427/4428 drivers are equally well-suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the TC4426/4427/4428. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

As MOSFET drivers, the TC4426/4427/4428 can easily switch 1000 pF gate capacitances in under 30 ns, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

Generally, the design of the TC4426/4427/4428 has taken into account 5 years of field use (and abuse) of Teledyne's earlier parts, with the goal of making these parts immune to all forms of improper operation known from that period, except exceeding the breakdown voltage and power dissipation ratings.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4426COA	8-Pin SOIC	0°C to +70°C
TC4426EOA	8-Pin SOIC	–40°C to +85°C
TC4426CPA	8-Pin Plastic DIP	0°C to +70°C
TC4426EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4426EJA	8-Pin CerDIP	–40°C to +85°C
TC4426MJA	8-Pin CerDIP	–55°C to +125°C
TC4427COA	8-Pin SOIC	0°C to +70°C
TC4427EOA	8-Pin SOIC	–40°C to +85°C
TC4427CPA	8-Pin Plastic DIP	0°C to +70°C
TC4427EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4427EJA	8-Pin CerDIP	–40°C to +85°C
TC4427MJA	8-Pin CerDIP	–55°C to +125°C
TC4428COA	8-Pin SOIC	0°C to +70°C
TC4428EOA	8-Pin SOIC	–40°C to +85°C
TC4428CPA	8-Pin Plastic DIP	0°C to +70°C
TC4428EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4428EJA	8-Pin CerDIP	–40°C to +85°C
TC4428MJA	8-Pin CerDIP	–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

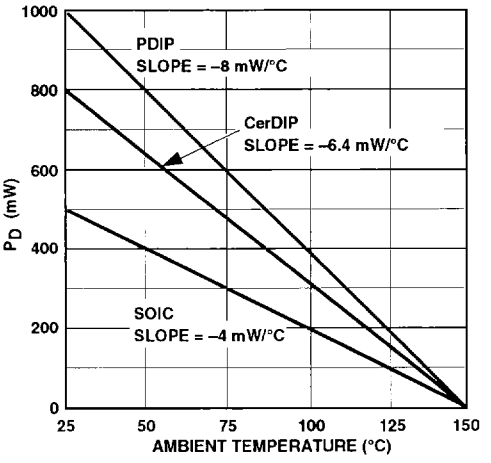
Supply Voltage ..... +22V
Input Voltage, IN A or IN B ..... V_{DD}+0.3V to GND–5.0V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 250°C/W
- SOIC $R_{\theta J-C}$ ..... 75°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... –40°C to +85°C
- M Version ..... –55°C to +125°C

Power Dissipation
- Plastic ..... 1000 mW
- CerDIP ..... 800 mW
- SOIC ..... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Power Dissipation



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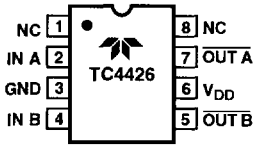
ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

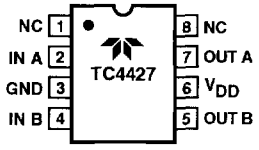
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	7	10	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	25	30	ns
t_F	Fall Time	Figure 1	—	25	30	ns
t_{D1}	Delay Time	Figure 1	—	—	30	ns
t_{D2}	Delay Time	Figure 1	—	—	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	— —	4.5 0.4	mA mA

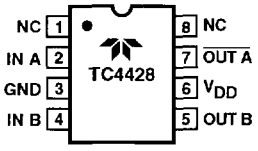
NOTE: 1. Switching times are guaranteed by design.

TC4426
TC4427
TC4428

PIN CONFIGURATIONS

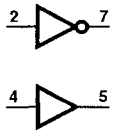






INVERTING

NONINVERTING



DIFFERENTIAL

NC = NO INTERNAL CONNECTION

NOTE: SOIC pinout is identical to DIP.

ELECTRICAL CHARACTERISTICS

Specifications measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	9	12	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	—	40	ns
t_F	Fall Time	Figure 1	—	—	40	ns
t_{D1}	Delay Time	Figure 1	—	—	40	ns
t_{D2}	Delay Time	Figure 1	—	—	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	— —	8 0.6	mA mA

NOTE: 1. Switching times are guaranteed by design.

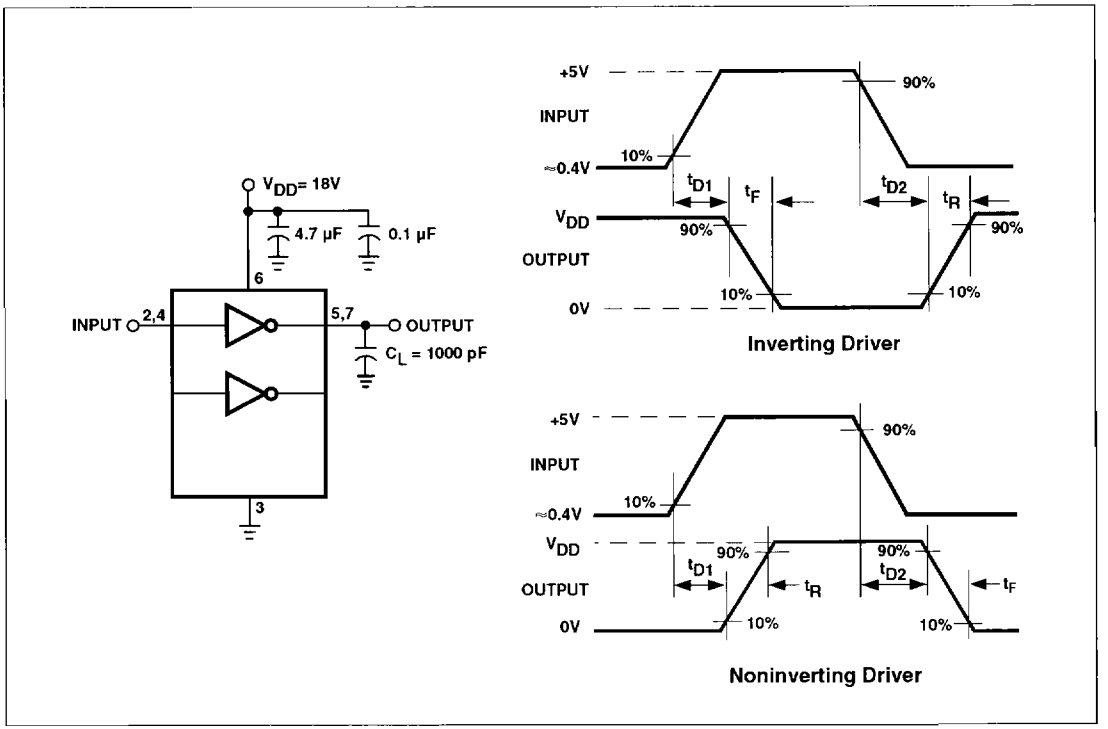
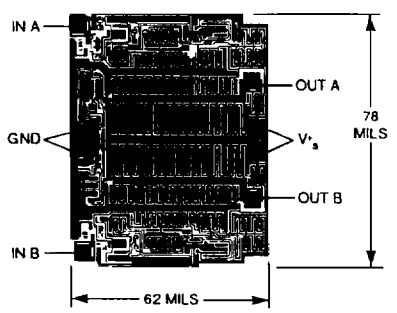


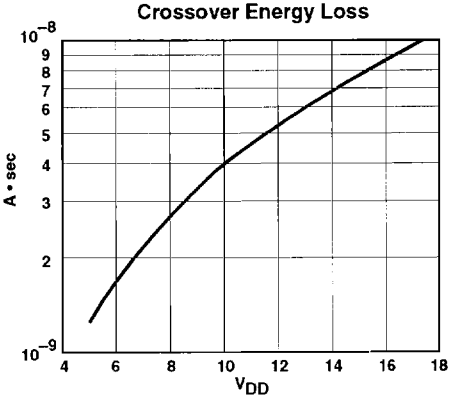
Figure 1. Switching Time Test Circuit

BONDING DIAGRAM



NOTES:
1. Back of die is common to V_{DD}.
2. Back of die is not metallized.

Crossover Energy Loss

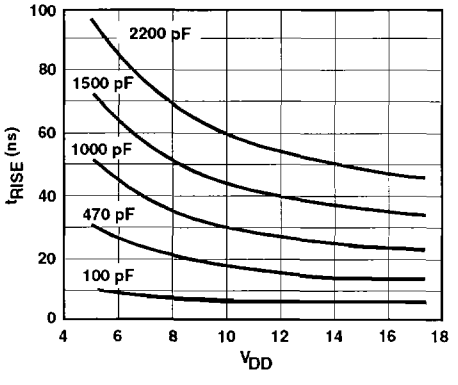


NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

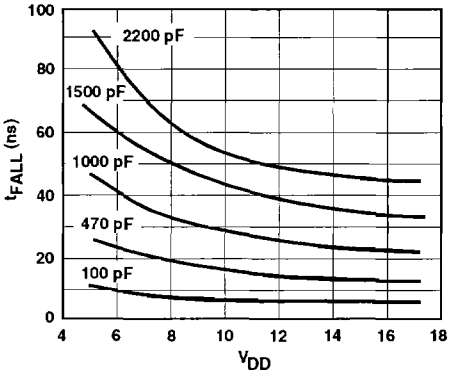
TC4426
TC4427
TC4428

TYPICAL CHARACTERISTICS CURVES

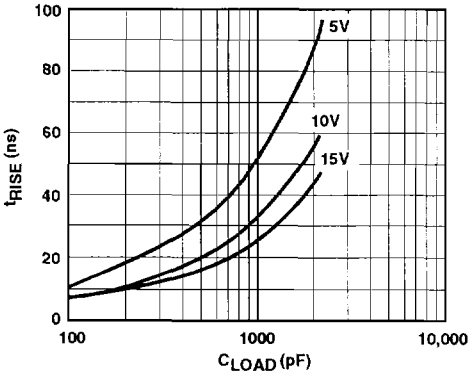
Rise Time vs Supply Voltage



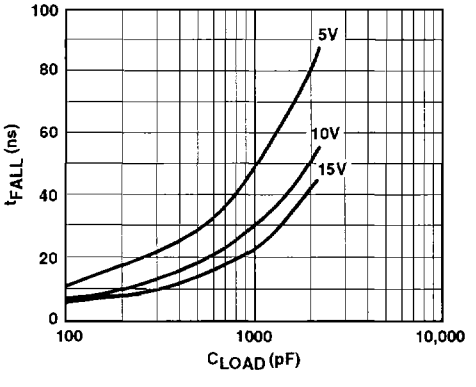
Fall Time vs Supply Voltage



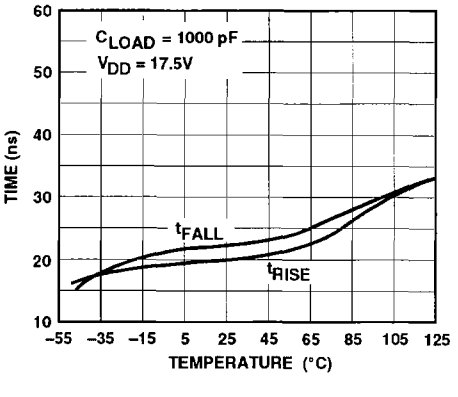
Rise TIme vs Capacitive Load



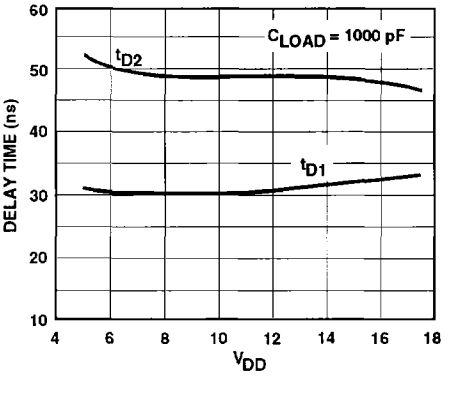
Fall TIme vs Capacitive Load



Rise and Fall Times vs Temperature

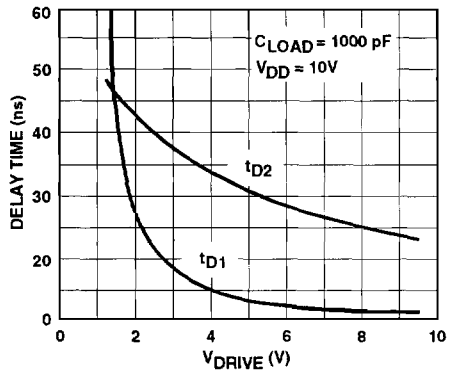


Propagation Delay vs Supply Voltage

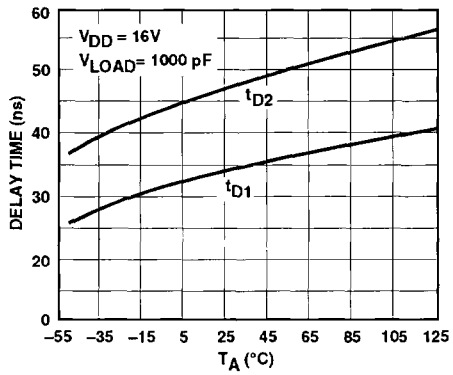


TYPICAL CHARACTERISTICS CURVES (Cont.)

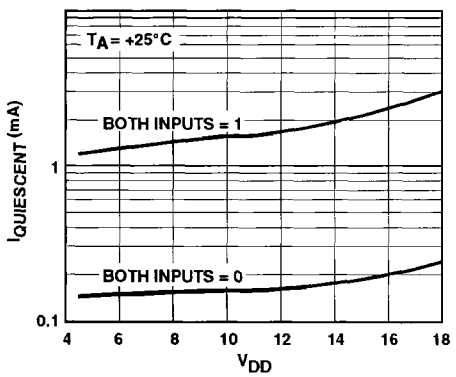
Effect of Input Amplitude on Delay Time



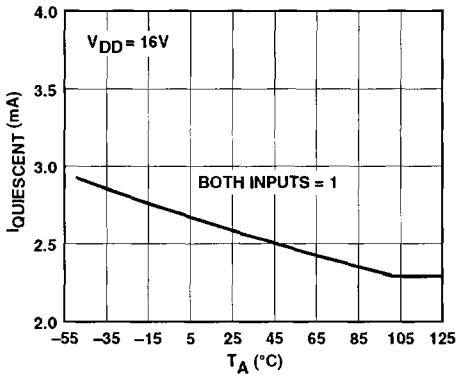
Propagation Delay Time vs Temperature



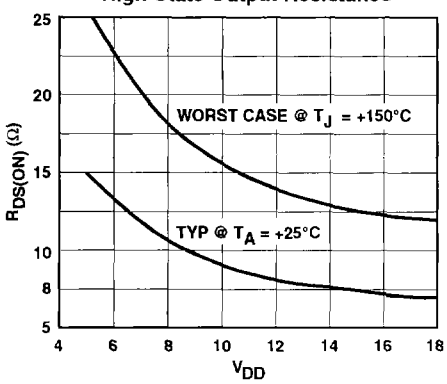
Quiescent Supply Current vs Voltage



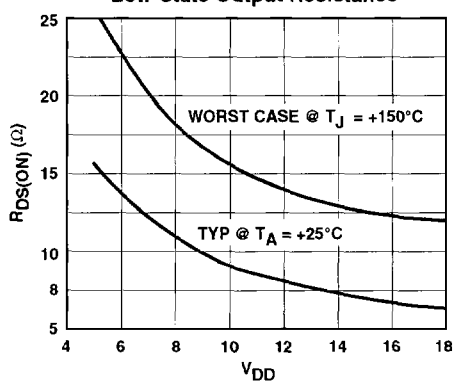
Quiescent Supply Current vs Temperature



High-State Output Resistance



Low-State Output Resistance



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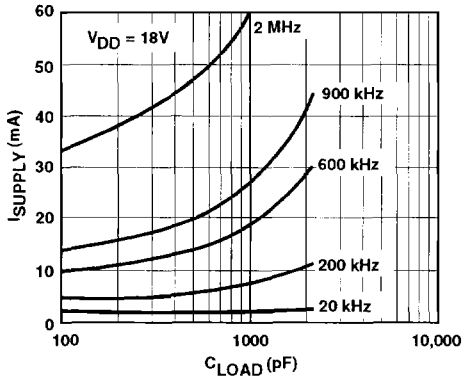
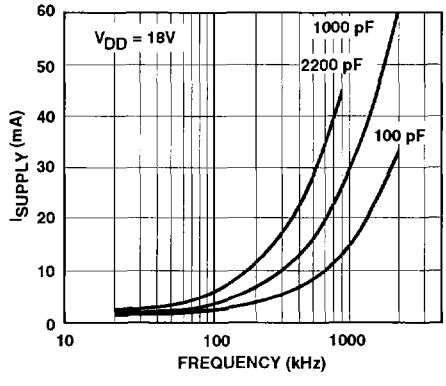
TC4426
TC4427
TC4428

SUPPLY CURRENT CHARACTERISTICS CURVES (Load on Single Output Only)

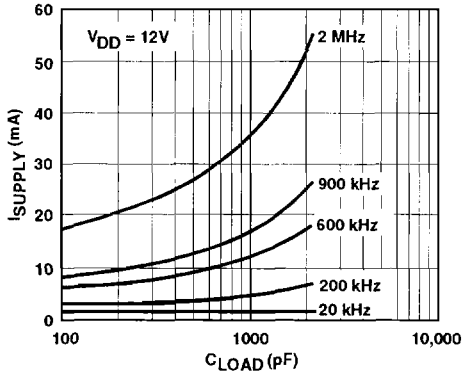
Supply Current vs Capacitive Load



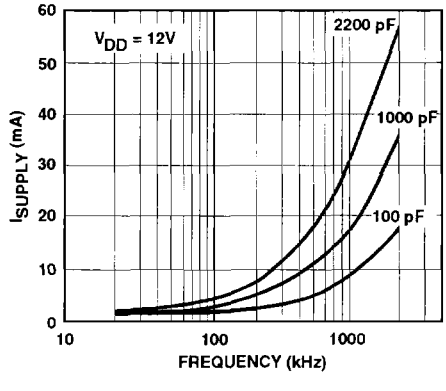
Supply Current vs Frequency



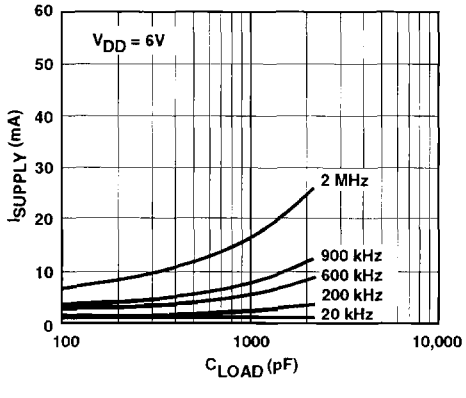
Supply Current vs Capacitive Load



Supply Current vs Frequency



Supply Current vs Capacitive Load



Supply Current vs Frequency