256K Static RAM
32K x 8-Bit

Features

- ☐ High speed access times
  Com'l: 10, 12, 15, 20 and 25ns
  Ind'l: 10, 12, 15, 20, and 25ns
  Mil : 12, 15, 20, 25, and 35ns

- ☐ Low power operation
  - PDM41256SA
    Active: 400mW (typ.)
    Standby: 150 mW (typ.)
  - PDM41256LA
    Active: 350mW (typ.)
    Standby: 25 mW (typ.)

- ☐ Single +5V (±10%) power supply
- ☐ TTL compatible inputs and outputs
- ☐ Military product MIL-STD-883
- ☐ Packages
  Plastic DIP (300 mil) - P
  Cerdip (300 mil) - D
  Plastic SOJ (300 mil) - SO
  Ceramic LCC - L32
  Cerpack (400 mil) - E

Description

The PDM41256 is a high performance CMOS static RAM organized as 32,768 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this devices is accomplished when the write enable (WE) and the chip enable (CE) inputs are both LOW. Reading is accomplished when WE remains HIGH and CE and OE are both LOW.

The PDM41256 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41256 comes in two versions, the standard power version PDM41256SA and a low power version the PDM41256LA. The two versions are functionally the same and only differ in their power consumption.

The PDM41256 is available in a 28-pin 300 mil PDIP, a 24-pin 300 mil CERDIP, in a 32-pin LCC, a 28-pin 300 mil SOJ and a 28-pin 400 mil Cerpack for surface mount applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883.

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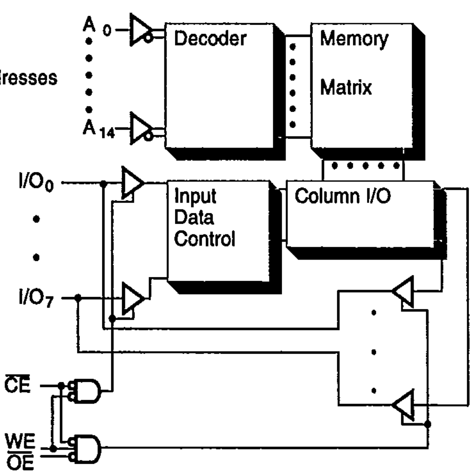
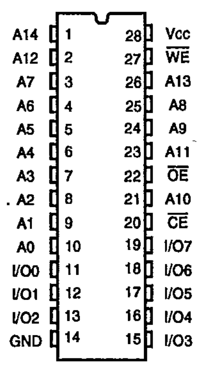
Functional Block Diagram

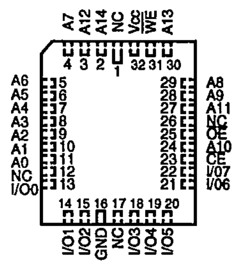


Pin Configuration

DIP
SOJ



LCC



Truth Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind./Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
Military	Ambient Temperature	-55	25	125	°C
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	-0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±10%)

Symbol	Parameter	Test Conditions		PDM41256SA		PDM41256LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	MIL. Com'l	-10 -5	10 5	-5 -2	5 2	μA
I_{LO}	Output Leakage Current	V_{CC} = MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. Com'l	-10 -5	10 5	-5 -2	5 2	μA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			-0.5(1)	0.8	-0.5(1)	0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = -3.0V for pulse width less than 20ns.

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Power Supply Characteristics

Symbol	Parameter	Power	10(1)	12		15		20		25		35	Unit
			Com'l.	Com'l.	Ind./Mil.	Com'l.	Ind./Mil.	Com'l.	Ind./Mil.	Com'l.	Ind./Mil.	Mil.	
I_{CC}	Operating Current $\overline{CE}$ = V_{IL}	SA	190	180	190	170	180	160	170	150	160	150	mA
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max I_{OUT} = 0mA	LA	170	160	170	150	160	140	150	130	140	130	mA
I_{SB}	Standby Current $\overline{CE}$ = V_{IH}	SA	70	60	60	50	50	40	40	35	35	30	mA
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max	LA	70	60	60	50	50	40	40	35	35	30	mA
I_{SB1}	Full Standby Current $\overline{CE}$ ≥ V_{CC} – 0.2V	SA	20	20	20	10	20	10	20	10	20	20	mA
	f = 0 V_{CC} = Max V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	LA	5	5	10	5	10	5	10	5	10	10	mA

NOTE: All values are maximum guaranteed values.
1. V_{CC} = 5V ± 5%.

Capacitance(1) (T_A = +25°C, f=1.0 Mhz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load for 12-35ns speed grades	See figures 1 and 2

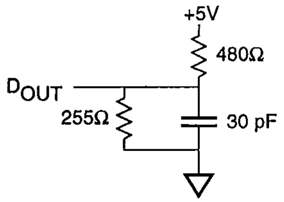


Figure 1. Output Load Equivalent

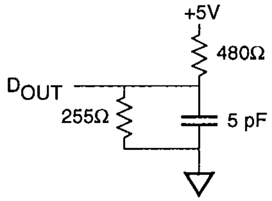
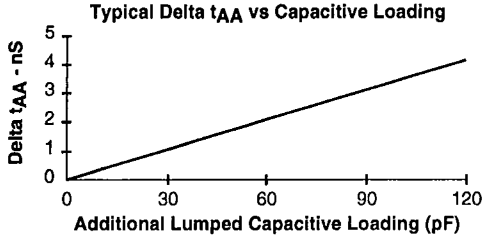
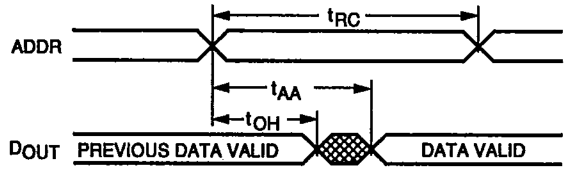


Figure 2. Output Load Equivalent
(for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

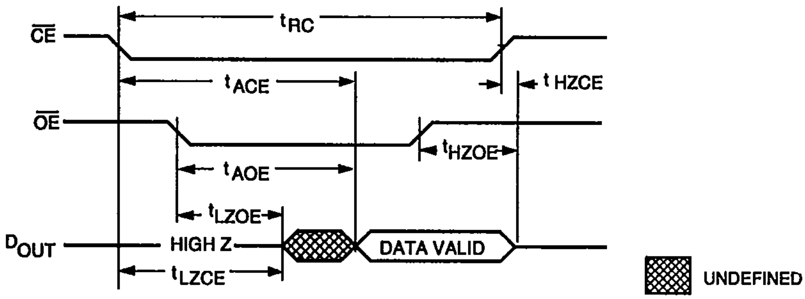
Typical Delta t_{AA} vs Capacitive Loading



Read Cycle No. 1(1)



Read Cycle No. 2(2)

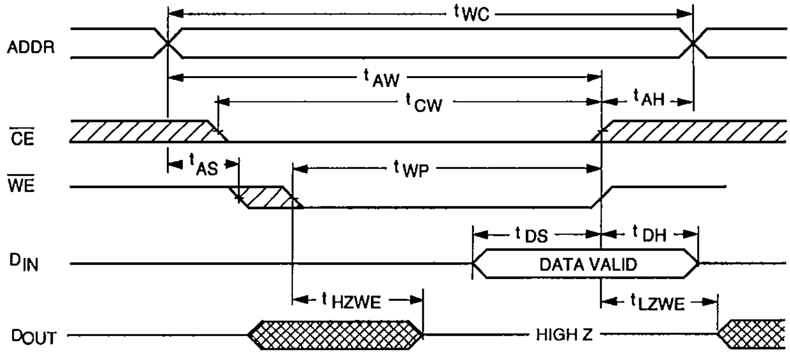


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

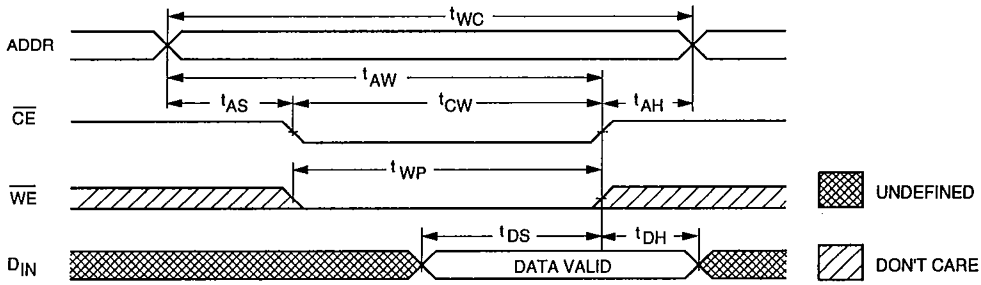
Description		-10(6)		-12		-15		-20		-25		-35		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	10		12		15		20		25		35		ns
Address access time	t_{AA}		10		12		15		20		25		35	ns
Chip enable access time	t_{ACE}		10		12		15		20		25		35	ns
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns
Chip enable to output in low Z(3, 4, 5)	t_{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z(3, 4, 5)	t_{HCZE}		5		5		5		5		10		10	ns
Chip enable to power up time(4)	t_{PU}	0		0		0		0		0		0		ns
Chip disable to power down time(4)	t_{PD}		10		12		15		20		25		35	ns
Output enable access time	t_{AOE}		5		6		8		10		12		15	ns
Output enable to output in low Z(4, 5)	t_{LZOE}	0		0		0		0		0		0		ns
Output disable to output in high Z(4, 5)	t_{HZOE}		5		5		5		5		10		10	ns

Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



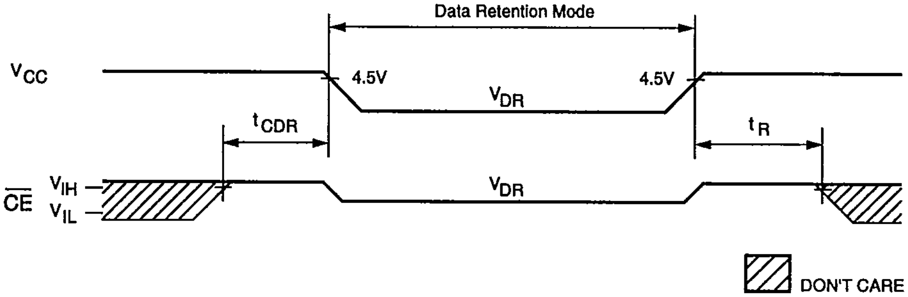
Write Cycle No. 2 (Chip Enable Controlled)



AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-10(6)		-12		-15		-20		-25		-35		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE Cycle time	t_{WC}	10		12		15		20		25		35		ns
Chip enable to end of write	t_{CW}	10		10		12		13		15		20		ns
Address Valid to end of write	t_{AW}	10		10		12		13		15		20		ns
Address set-up time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP}	10		10		11		12		15		20		ns
Data set-up time	t_{DS}	7		7		8		9		10		12		ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns
Write disable to output in low Z(4, 5)	t_{LZWE}	0		0		0		0		0		0		ns
Write enable to output in high Z(4, 5)	t_{HZWE}		3		3		3		3		5		8	ns

Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current (15-35 ns)	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$	—	95	500	µA
			$V_{CC} = 3V$	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(4)	Operation Recovery Time			t_{RC}	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. The device is continuously selected. All the Chip Enables are held in their active state.
2. The address is valid prior to or coincident with the latest occuring Chip Enable.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. The parameter is tested with CL = 5pF as shown in Figure 2. Transition is measured ±200mV from steady state voltage.
6. See fig. 3 for output load. $V_{CC} = 5V \pm 5\%$.

Ordering Information

PDM XXXXX A XX A A

Device Type	Power	Speed	Package	
XXXXX	A	XX	A	A

Temperature range (last A):

Blank	Commercial (0° to +70°C)
I	Industrial (-40°C to +85°C)
M	Military Temp. Only (-55°C to +125°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD 883

Package:

P	300 mil Plastic Dip
D	300 mil Cerdip
L32	450 x 550 LCC
SO	300 mil Plastic SOJ
E	400 mil Cerpack

Speed:

10	Commercial Only
12	
15	
20	
25	
35	Military Only

Power:

SA	Standard Power
LA	Low Power

Device Type:

41256	256K (32K x 8) Static RAM

Chip	Package Type
PDM41256	28 pin Plastic DIP
	28 pin Plastic SOJ
	28 pin Cerdip
	32 pin-LCC
	28 pin Cerpack