



### 3.3V CMOS DUAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

IDT74ALVC74

#### FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$ , Normal Range
- $V_{cc} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SOIC, SSOP, and TSSOP packages

#### DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Suitable for Heavy Loads

#### APPLICATIONS:

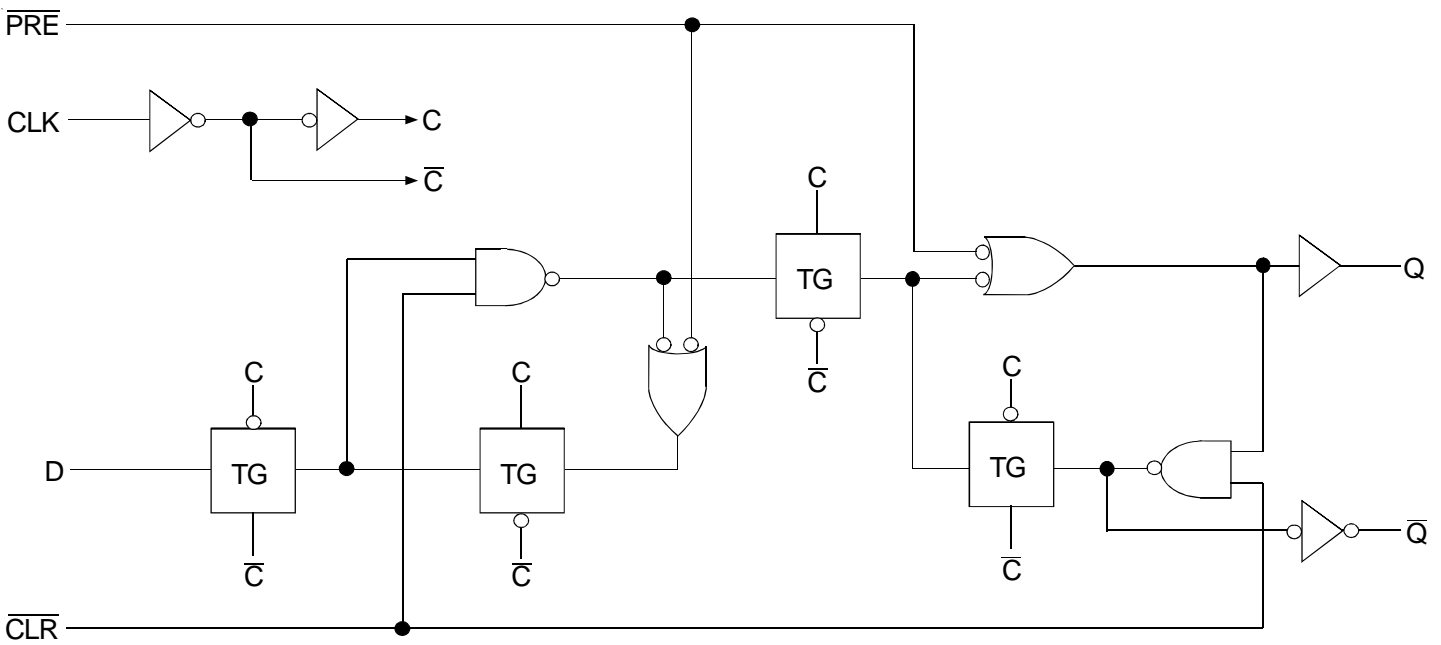
- 3.3V high speed systems
- 3.3V and lower voltage computing systems

#### DESCRIPTION:

This dual positive-edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The ALVC74 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

#### FUNCTIONAL BLOCK DIAGRAM

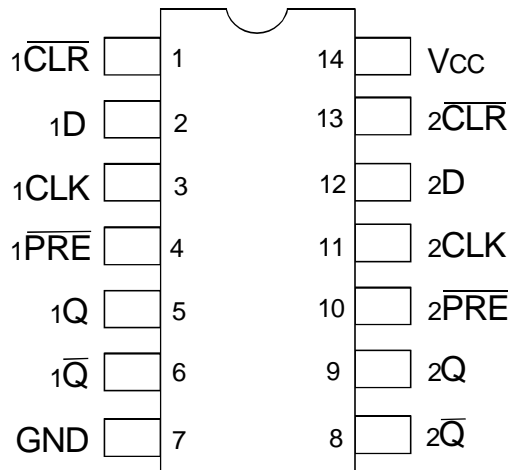


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INDUSTRIAL TEMPERATURE RANGE

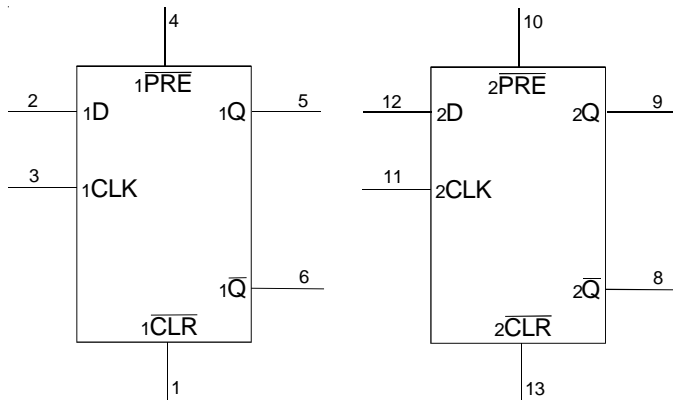
JUNE 2000

### PIN CONFIGURATION



SOIC/SSOP/TSSOP  
TOP VIEW

### LOGIC SYMBOLS



### PIN DESCRIPTION

Pin Names	Description
xCLK	Clock Inputs
xCLR	Clear Inputs
xPRE	Preset Inputs
xD	Data Inputs
xQ, xQ $\bar$	Data Outputs

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

### CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

**NOTE:**

- As applicable to the device type.

### FUNCTION TABLE<sup>(1)</sup>

Inputs				Outputs	
xPRE	xCLR	xCLK	xD	xQ	xQ $\bar$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(2)</sup>	H <sup>(2)</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sup>(3)</sup>	Q $\bar$ <sup>(4)</sup>

**NOTES:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance  
↑ = LOW-to-HIGH Transition
- This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (HIGH) level.
- Level of Q before the indicated steady-state input conditions were established.
- Complement of Q or level of Q $\bar$  before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ 

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = V <sub>CC</sub>	—	—	±10	μA
			V <sub>O</sub> = GND	—	—	±10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IIN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	10	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	μA

## NOTE:

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3V		2.4	—	
		V <sub>CC</sub> = 3V	I <sub>OH</sub> = -24mA	2	—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3V	I <sub>OL</sub> = 24mA	—	0.55	

## NOTE:

1. V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

OPERATING CHARACTERISTICS,  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per Flip-Flop	C <sub>L</sub> = 0pF, f = 10Mhz	20	31	pF

SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>MAX</sub>								MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xCLK to xQ or x $\bar{Q}$	1	6	1	5	1	3.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay x $\overline{\text{PRE}}$ or x $\overline{\text{CLR}}$ to xQ or x $\bar{Q}$	1	6.2	1	5.2	1	4	ns
t <sub>w</sub>	Pulse Duration, x $\overline{\text{PRE}}$ or x $\overline{\text{CLR}}$ LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>w</sub>	Pulse Duration, xCLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t <sub>SU</sub>	Setup Time, data before xCLK $\uparrow$	3	—	3	—	3	—	ns
t <sub>SU</sub>	Setup Time, x $\overline{\text{PRE}}$ or x $\overline{\text{CLR}}$ inactive	2	—	2	—	2	—	ns
t <sub>H</sub>	Hold Time, data after xCLK $\uparrow$	1	—	1	—	0	—	ns

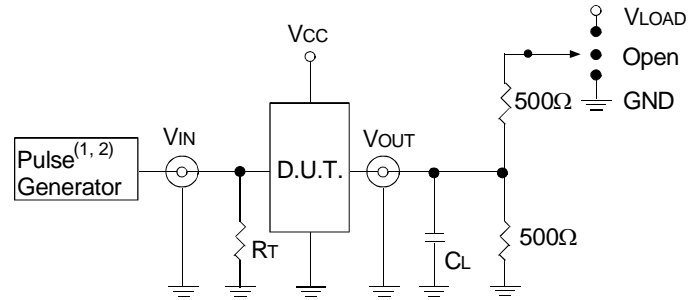
NOTE:

1. See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V	V <sub>CC</sub> <sup>(1)</sup> =2.7V	V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

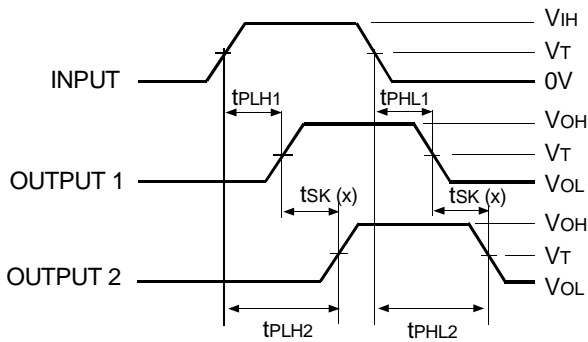
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Z<sub>out</sub> of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; tr ≤ 2ns; tr ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

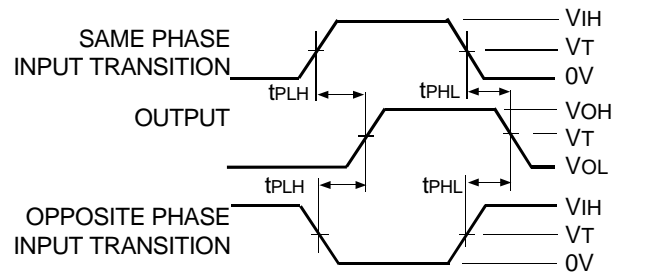


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

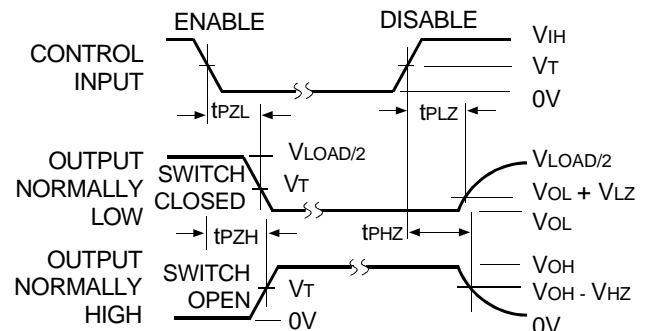
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



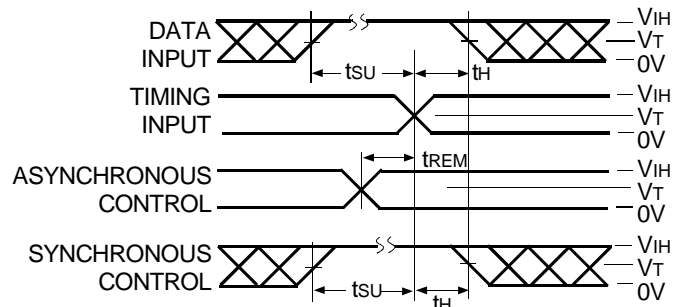
Propagation Delay



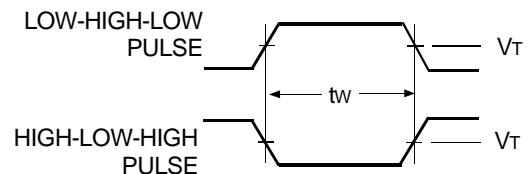
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

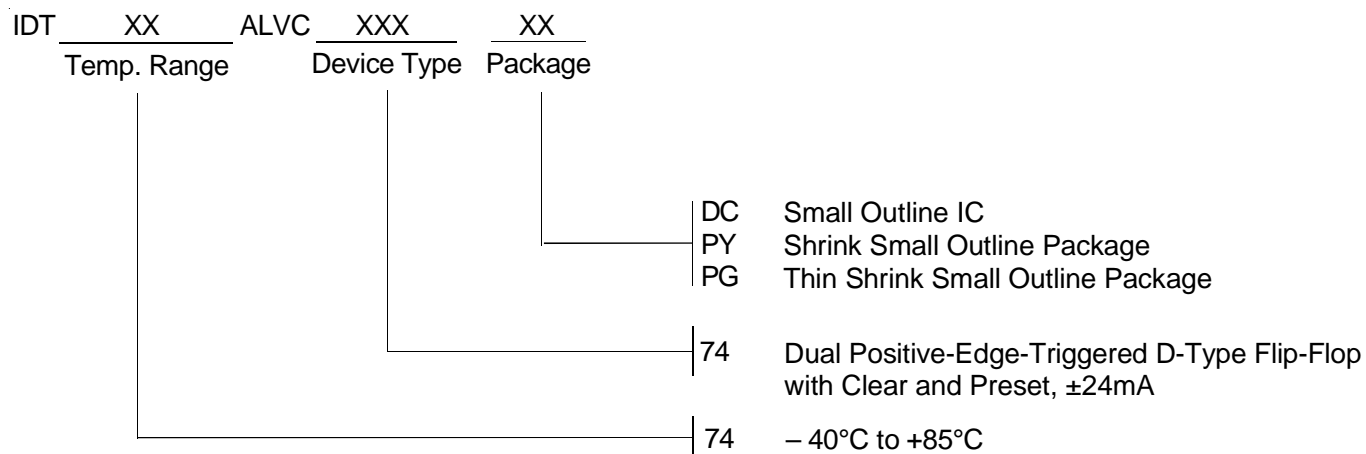


Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION



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