Signetics

74LS253, S253
Multiplexers

Dual 4-Input Multiplexer (3-State)
Product Specification

Logic Products

FEATURES
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION
The '253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

TYPE	TYPICAL PROPAGATION DELAY (From Data)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS253	15ns	8mA
74S253	8ns	48mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74S253N, N74LS253N
Plastic SO-16	N74LS253D, N74S253D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S	74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE:
A 74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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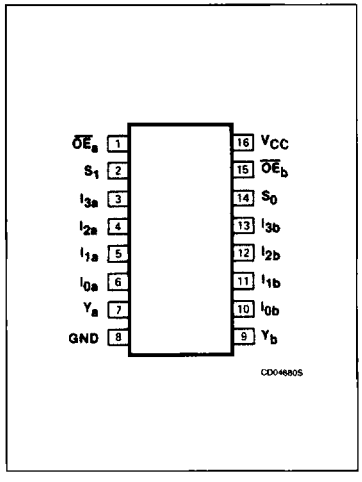
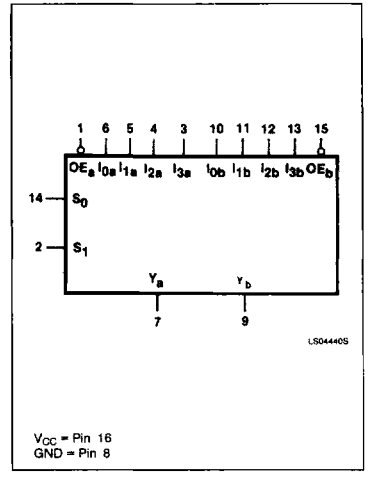
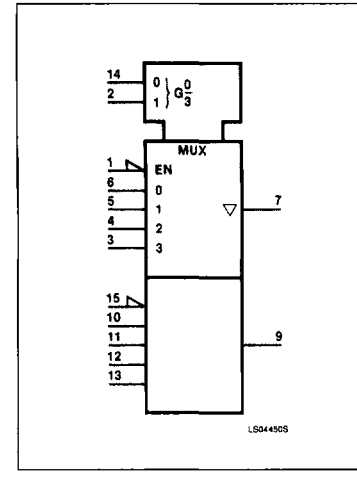
PIN CONFIGURATION



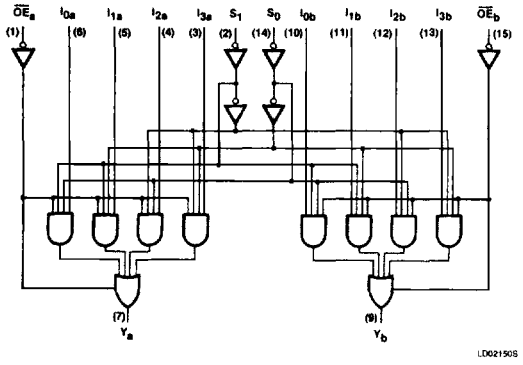
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

The '253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Y}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care.
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	HIGH-level output current			−2.6			−6.5	mA
I_{OL}	LOW-level output current			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74LS253			74S253			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4	3.1		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.35	0.5			0.5	V
			I_{OL} = 4mA (74LS)		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V			20				μA
			V_O = 2.4V						50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V			−20				μA
			V_O = 0.5V						−50	μA
I_I	Input current at maximum Input voltage	V_{CC} = MAX	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V			20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4				mA
			V_I = 0.5V						−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−15		−100	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1		7	12			70	mA
			Condition 2		8.5	14				mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured under the following conditions with the outputs open: *Condition* 1: All inputs grounded. *Condition* 2: $\overline{OE}$ at 4.5V, all inputs grounded.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS C_L = 15pF, R_L = 2kΩ		74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Output	Waveform 1		25 20		9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		45 32		18 18	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		28		13	ns
t_{PZL}	Output enable to LOW level	Waveform 3		23		14	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF		41		8.5	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF		27		14	ns

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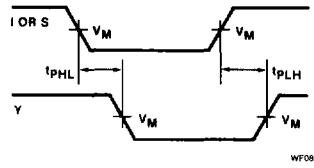
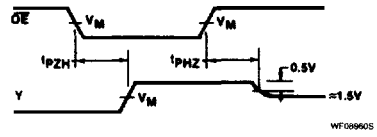
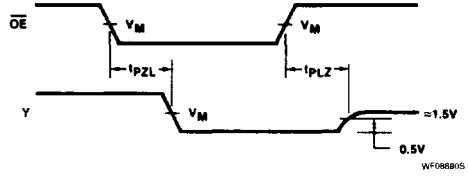
AC WAVEFORMS



Waveform 1. Propagation Delay Data Or Select To Output



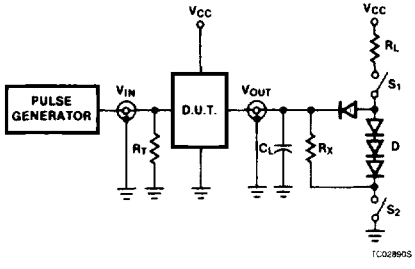
Waveform 2. 3-State Enable Time To High Level And Disable Time From High Level



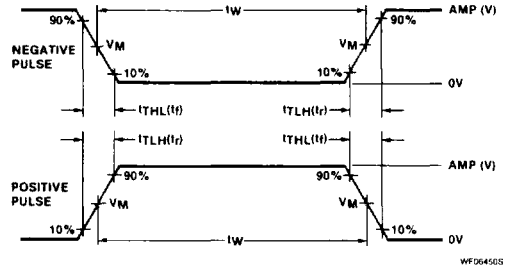
For all waveforms, V_M = 1.3V for 74LS; V_M = 1.5V for 74 and 74LS.

Waveform 3. 3-State Enable Time To Low Level And Disable Time From Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns