Am9311 • Am54/74154
Demultiplexer/One of Sixteen Decoder

Distinctive Characteristics:

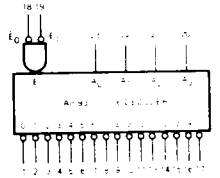
- 100% reliability assurance Testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am9311 Demultiplexer/One-of-Sixteen Decoder accepts four inputs and selects one of sixteen mutually exclusive active LOW outputs as shown in Table II. The Am9311 is enabled by a LOW signal on $\overline{E}_0$ and $\overline{E}_1$ inputs.

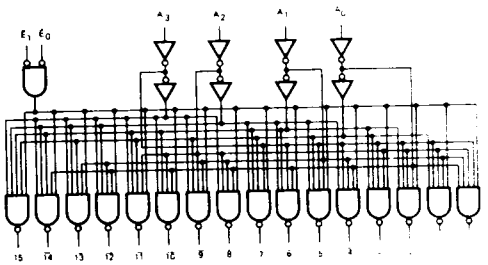
Incoming data on either $\overline{E}_0$ or $\overline{E}_1$ with the other enable input held LOW can be demultiplexed to any one of the sixteen outputs, zero through fifteen, with binary addressing at inputs A_0, A_1, A_2 and A_3. This demultiplexing capability is shown in Figure 9.

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

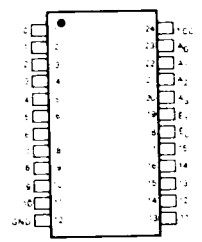


Am9311/Am54/74154 ORDERING INFORMATION

Package Type	Ambient Temperature	Am9311 Order Number	Am54/74154 Order Number
Molded DIP	0°C to +75°C	Am9311C	SN74154N
Hermetic DIP	0°C to +75°C	U6N931159X	SN74154J
Hermetic DIP	−55°C to +125°C	U6N931151X	SN54154J
Flat Pak	−55°C to +125°C	U4M931151X	SN54154W
Dice	Note	UXX9311XXD	SN74154D

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM NGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +1
Temperature (Ambient) Under Bias	−55°C to +1
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V
DC Input Voltage	−0.5 V to +1
Output Current, Into Outputs	1
DC Input Current	−30 mA to +5

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93115BX Am74154 T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am93115IX Am54154 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am931151X Am54154		35	49	mA
			Am931158X Am74154		35	56	

Notes 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics (T_A = 25°C)

Parameters		Test Conditions	Min	Typ	Max	Units
$t_{pd+}(\overline{AO})$	Turn Off Delay A input to output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Figure 6	10	22	31	ns
$t_{pd-}(\overline{AO})$	Turn On Delay A input to output		7	21	28	ns
$t_{pd+}(\overline{EO})$	Turn Off Delay Enable input to output		10	15	23	ns
$t_{pd-}(\overline{EO})$	Turn On Delay Enable input to output		7	15	22	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Decoder/Demultiplexer On the basis of an applied instruction, channels of communication are selected which connect certain sources of information to certain destinations e.g., the distribution of timing signals; the interconnection between arithmetic registers.

$\overline{E}_0$, $\overline{E}_1$ Enable Inputs. The device is enabled when both the Enable inputs are LOW.

Fan-Out The logic HIGH or LOW output drive capability in terms of input Unit Loads.

Input Unit Load One T²L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

$\overline{O}_j$ Active LOW output of Demultiplexer/Decoder j = 0-15.

OPERATIONAL TERMS:

I_{OH} Output HIGH current forced out of output in V_{OH} test

I_{OL} Output LOW current forced into the output in V_{OL} test

I_{IH} Reverse input load current with V_{CC} applied to input

Negative Current Current flowing out of the device

Positive Current Current flowing into the device

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 7

V_{IL} Maximum logic LOW input voltage. Refer to Figure 7

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

$t_{pd+}(A\overline{O})$ The propagation delay from input address transition to the output LOW to HIGH transition

$t_{pd-}(A\overline{O})$ The propagation delay from input address transition to the output HIGH to LOW transition

$t_{pd+}(\overline{E}\overline{O})$ The propagation delay from input Enable LOW to HIGH transition to the output LOW to HIGH transition

$t_{pd-}(\overline{E}\overline{O})$ The propagation delay from input Enable HIGH to LOW transition to the output HIGH to LOW transition

PERFORMANCE CURVES

Input/Output Characteristics

Input Current Versus Input Voltage

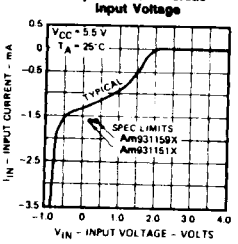


Figure 1

Output Current Versus Output Voltage Output Low

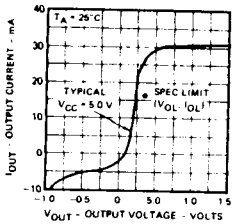


Figure 2

Output Current Versus Output Voltage Output High

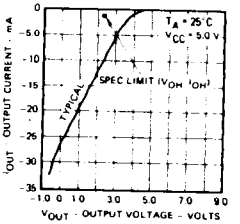


Figure 3

Switching Characteristics

Typical Turn On Delay Versus Temperature

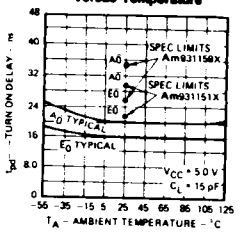


Figure 4

Typical Turn Off Delay Versus Temperature

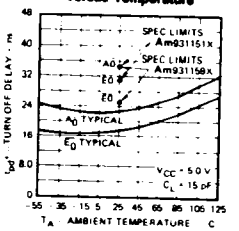
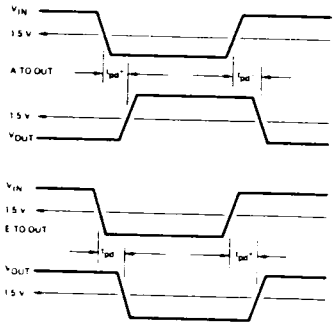


Figure 5

SWITCHING TIME TEST CIRCUIT & WAVEFORMS



PULSE GEN CHARACTERISTICS
Freq. ≈ 1 MHz
Pulse Width ≈ 100 ns
$t_r = t_f \leq 15$ ns
Amplitude ≈ 4 V

*Includes all probe and jig capacitance

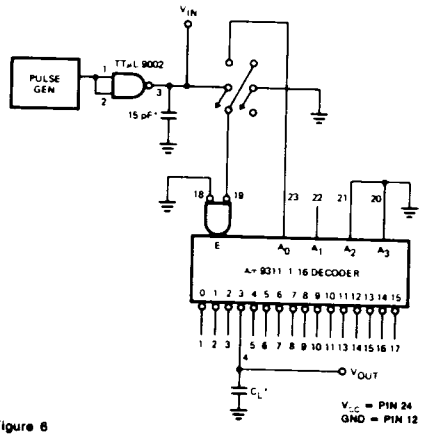


Figure 6

Am9311 LOADING RULES (In unit loads)

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{0}_{OUT}$	1	—	20	10
$\overline{1}_{OUT}$	2	—	20	10
$\overline{2}_{OUT}$	3	—	20	10
$\overline{3}_{OUT}$	4	—	20	10
$\overline{4}_{OUT}$	5	—	20	10
$\overline{5}_{OUT}$	6	—	20	10
$\overline{6}_{OUT}$	7	—	20	10
$\overline{7}_{OUT}$	8	—	20	10
$\overline{8}_{OUT}$	9	—	20	10
$\overline{9}_{OUT}$	10	—	20	10
$\overline{10}_{OUT}$	11	—	20	10
GND	12	—	—	—
$\overline{11}_{OUT}$	13	—	20	10
$\overline{12}_{OUT}$	14	—	20	10
$\overline{13}_{OUT}$	15	—	20	10
$\overline{14}_{OUT}$	16	—	20	10
$\overline{15}_{OUT}$	17	—	20	10
$\overline{E}_0$	18	1	—	—
$\overline{E}_1$	19	1	—	—
A_3	20	1	—	—
A_2	21	1	—	—
A_1	22	1	—	—
A_0	23	1	—	—
V_{CC}	24	—	—	—

Table I

TRUTH TABLE

INPUTS $\overline{E}_0$	$\overline{E}_1$	A_3	A_2	A_1	A_0	OUTPUTS $\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table II

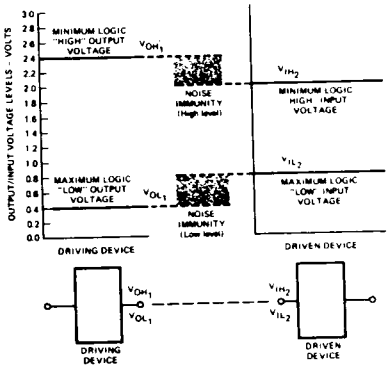
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75 85	1	1
DTL Series 930	12	1

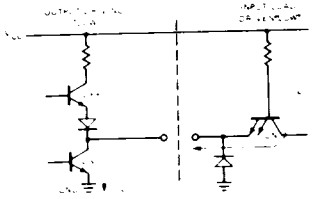
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

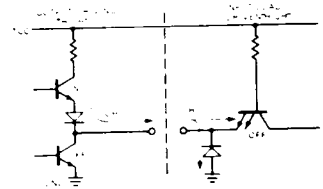
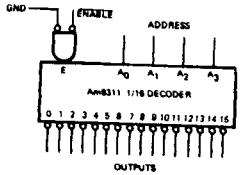


Figure 7

Am9311 APPLICATIONS

Decode any 4 bit BCD code

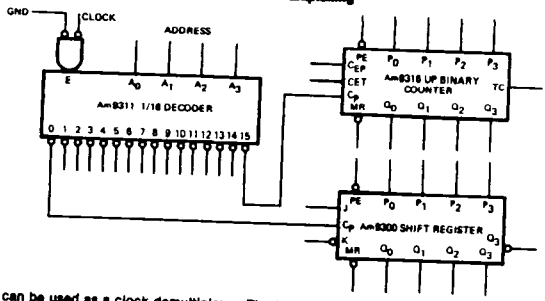


Decode any BCD code using a 9311 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

Figure 8

DECIMAL DIGIT	OUTPUT SELECTION: BCD CODE 8421	BCD CODE 5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

Clock Demultiplexing



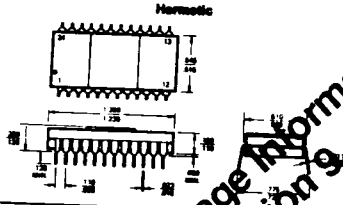
The Am9311 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Up to 5 register counter stages can be driven by one decoder output allowing word lengths of 20 bits to be controlled. Any sequential circuit in the 9300 MSI family can be used in this configuration.

Figure 9

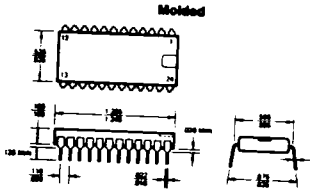
PHYSICAL DIMENSIONS

Dual-In-Line

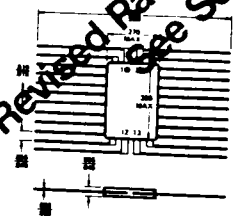
Hermetic



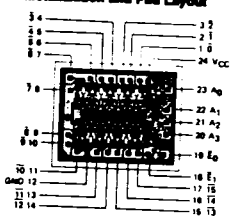
Molded



Flat Package



Metallization and Pad Layout



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

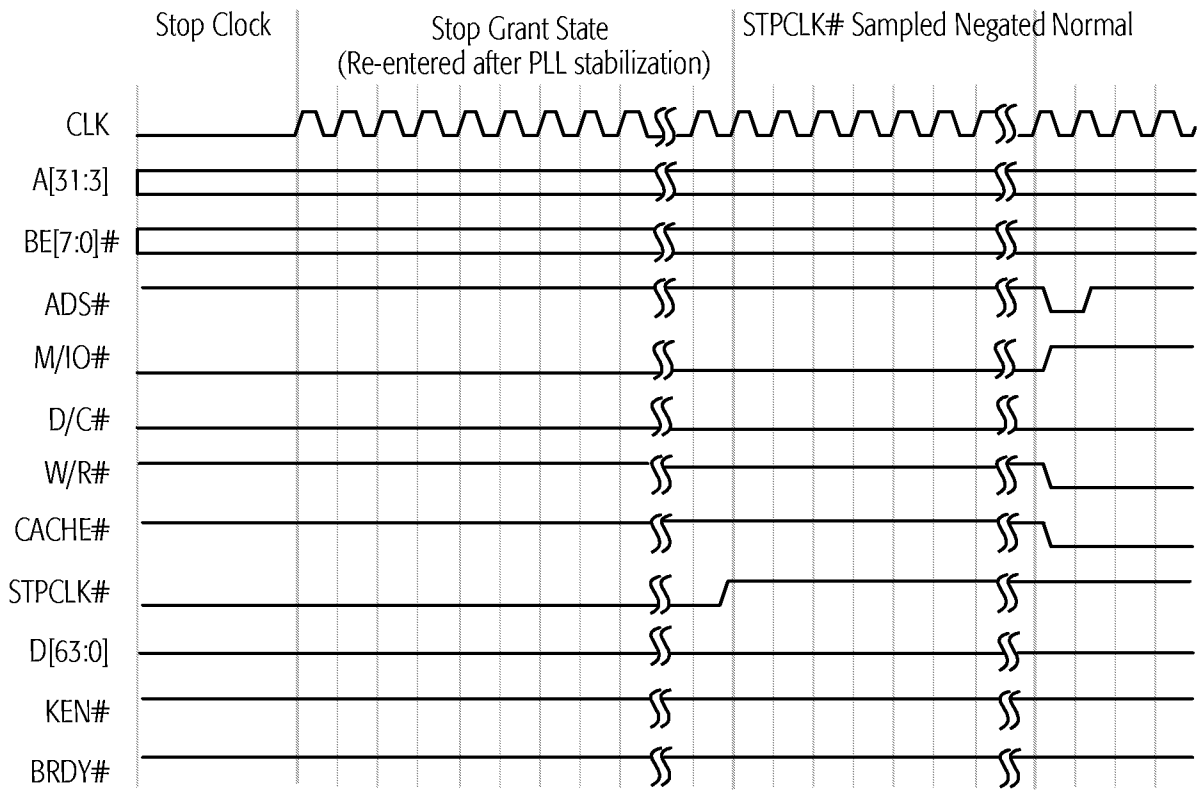


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

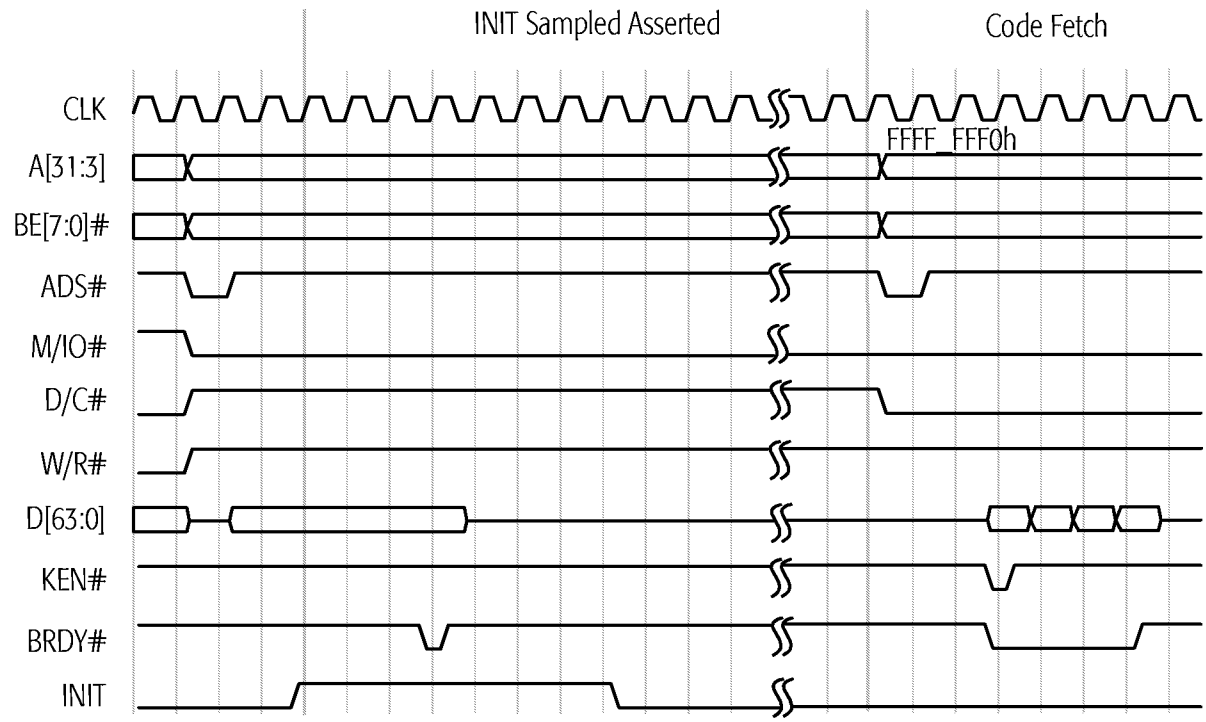


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.