

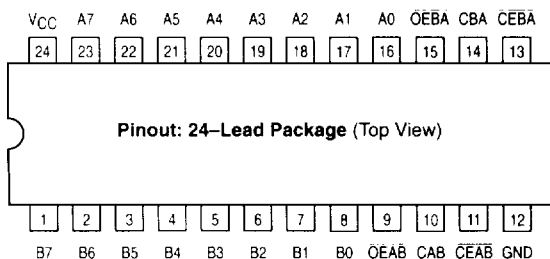
*Product Preview*

**Low-Voltage CMOS Octal Registered Transceiver With Dual Output and Clock Enables**  
**With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)**

The MC74LCX2952 is a high performance, non-inverting octal registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX2952 inputs to be safely driven from 5V devices. The MC74LCX2952 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Two 8-bit back to back registers store data from either of two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CAB, CBA) provided that the Clock Enable ( $\overline{CEAB}$ ,  $\overline{CEBA}$ ) is Low. The data is then presented at the 3-state output buffers, but is only accessible when the Output Enable ( $\overline{OEAB}$ ,  $\overline{OEBA}$ ) is Low. The operation of the MC74LCX2952 is symmetrical — A inputs to B outputs occurs in the same manner as B inputs to A outputs.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I<sub>OFF</sub> Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVC MOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



**MC74LCX2952**

**LCX**

**LOW-VOLTAGE CMOS  
OCTAL REGISTERED  
TRANSCEIVER**



**DW SUFFIX**  
PLASTIC SOIC  
CASE 751E-04



**SD SUFFIX**  
PLASTIC SSOP  
CASE 940D-03



**DT SUFFIX**  
PLASTIC TSSOP  
CASE 948H-01

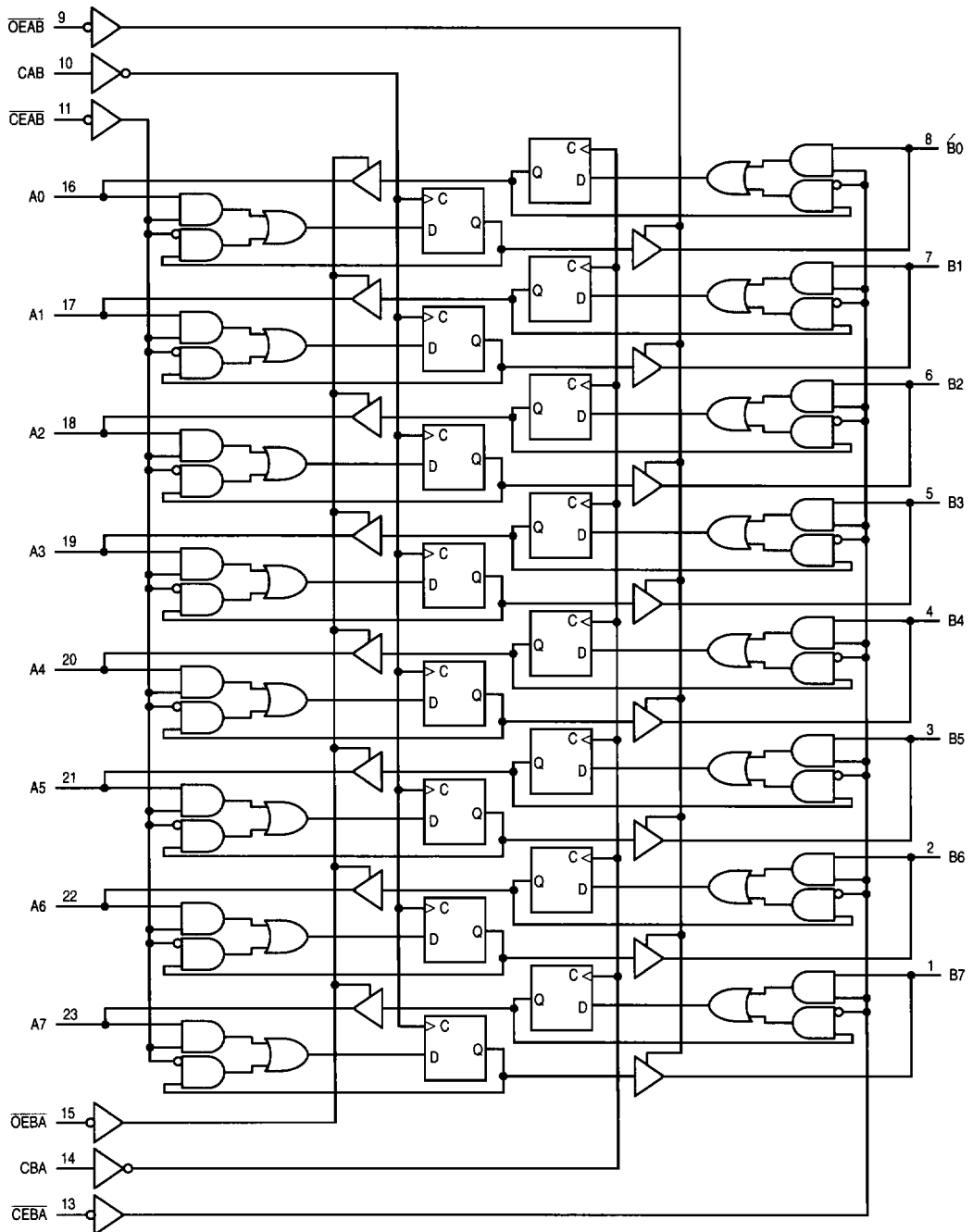
**PIN NAMES**

Pins	Function
A0–A7	Side A Inputs/Outputs
B0–B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
$\overline{CEAB}$ , $\overline{CEBA}$	Clock Enable Inputs
$\overline{OEAB}$ , $\overline{OEBA}$	Output Enable Inputs

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



## LOGIC DIAGRAM



FUNCTION TABLE

Inputs								Internal Register		Outputs		Operating Mode
An	OEAB	CEAB	CAB	Bn	OEBA	CEBA	CBA	QABn	QBAn	An	Bn	
h l	L L	l l	↑ ↑	U U	H H	X X	X X	H L	X X	NA NA	H L	Load A to B Register; Read B Output
X	L	h	X	U	H	X	X	NC	X	NA	NC	Hold; Read B Output
h l	H H	l i	↑ ↑	X X	H H	X X	X X	H L	X X	NA NA	Z Z	Load A to B Register; Disable B Outputs
X	H	h	X	X	H	X	X	NC	X	NA	Z	Hold; Disable B Outputs
U U	H H	X X	X X	h l	L L	l l	↑ ↑	X X	H L	H L	NA NA	Load B to A Register; Read A Output
U	H	X	X	X	L	h	X	X	NC	NC	NA	Hold; Read A Output
X X	H H	X X	X X	h l	H H	l l	↑ ↑	X X	H L	Z Z	NA NA	Load B to A Register; Disable A Outputs
X	H	X	X	X	H	h	X	X	NC	Z	NA	Hold; Disable A Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to Clock Low-to-High Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to Clock Low-to-High Transition; NA = Not Applicable; U = Undriven; Z = High Impedance State; X = Don't Care; NC = No Change; ↑ = Low-to-High Transition

ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5 <sup>1</sup>	Output in HIGH or LOW State	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. I<sub>O</sub> absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	2.0	3.3	3.6	V
	Operating Data Retention Only	1.5	3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State) (3-State)	0		V <sub>CC</sub> 5.5	V
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			-24	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			-12	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
Δt <sub>AV</sub>	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 1)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 1)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>O</sub> ≤ 5.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = GND or V <sub>CC</sub>		10	μA
		2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

1. These values of V<sub>I</sub> are used to test DC electrical characteristics only. Functional test should use V<sub>IH</sub> ≥ 2.4V, V<sub>IL</sub> ≤ 0.5V.

**AC CHARACTERISTICS** ( $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			$V_{CC} = 3.0\text{V to } 3.6\text{V}$		$V_{CC} = 2.7\text{V}$		
			Min	Max	Min	Max	
$f_{\text{max}}$	Clock Pulse Frequency	3	150				MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Clock to Output	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time From High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
$t_s$	Setup Time, HIGH to LOW Data to Clock	3	2.5		2.5		ns
$t_h$	Hold Time, HIGH to LOW Data to Clock	3	1.5		1.5		ns
$t_s$	Setup Time, HIGH to LOW $\overline{CE}_{\text{EX}}$ to Clock	3	2.5		2.5		ns
$t_h$	Hold Time, HIGH to LOW $\overline{CE}_{\text{EX}}$ to Clock	3	1.5		1.5		ns
$t_w$	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
$t_{\text{OSHL}}$ $t_{\text{OSLH}}$	Output-to-Output Skew (Note 2)			1.0 1.0			ns

- These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{\text{OSHL}}$ ) or LOW-to-HIGH ( $t_{\text{OSLH}}$ ), parameter guaranteed by design.

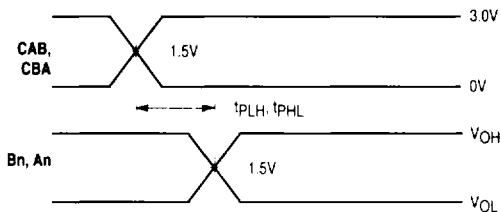
**DYNAMIC SWITCHING CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{\text{OLP}}$	Dynamic LOW Peak Voltage <sup>1</sup>	$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ , $V_{\text{IH}} = 3.3\text{V}$ , $V_{\text{IL}} = 0\text{V}$		0.8		V
$V_{\text{OLV}}$	Dynamic LOW Valley Voltage <sup>1</sup>	$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ , $V_{\text{IH}} = 3.3\text{V}$ , $V_{\text{IL}} = 0\text{V}$		0.8		V

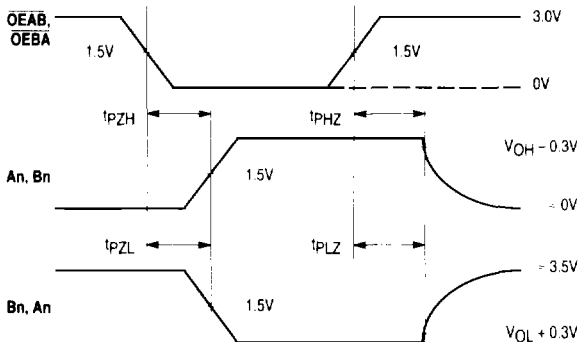
- Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

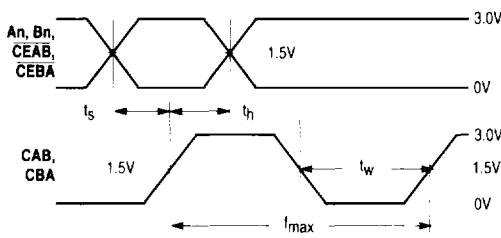
Symbol	Parameter	Condition	Typical	Unit
$C_{\text{PD}}$	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	25	pF
$C_{\text{IN}}$	Input Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	7	pF
$C_{\text{I/O}}$	Input/Output Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	8	pF



**WAVEFORM 1 – Cxx to An/Bn PROPAGATION DELAYS**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ,  $t_W = 500\text{ns}$

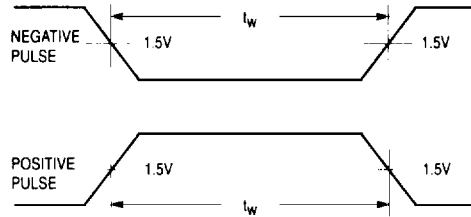


**WAVEFORM 2 – OE $\bar{x}$ x to An/Bn OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ,  $t_W = 500\text{ns}$



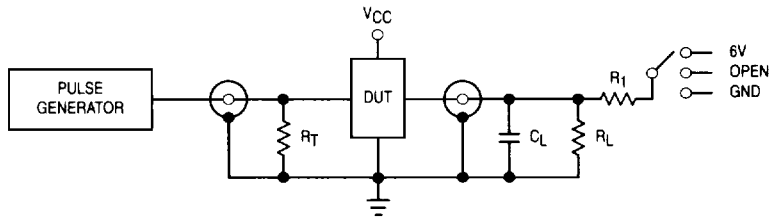
**WAVEFORM 3 – Cxx MINIMUM PULSE WIDTH, An/Bn/CE $\bar{x}$ x to Cxx SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ,  $t_W = 500\text{ns}$  except when noted

**Figure 1. AC Waveforms**



**WAVEFORM 4 - INPUT PULSE DEFINITION**  
 $t_r = t_f = 2.5\text{ns}$ , 10% to 90% of 0V to 2.7V

**Figure 2. AC Waveforms**



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 3. Test Circuit**