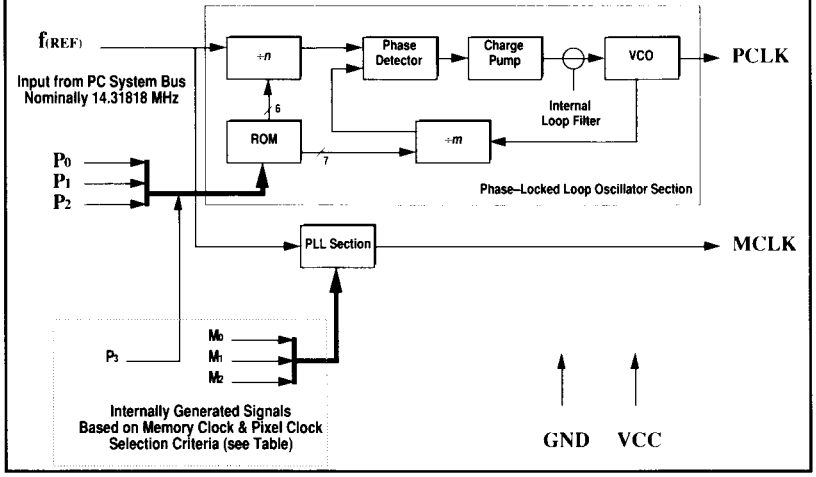
ICD2043

Dual VGA Clock Generator w/Fixed Memory Clock

8–Pin Dual Oscillator for Personal Computer Graphic Boards Handles all Frequency Requirements of Popular VGA/8514 Chip Sets.

- **2 Independent Clock Outputs — Handles Separate Pixel Clock and Fixed Memory Clock**
- **Phase–Locked Loop Oscillator Input Derived from PC System Bus**
- **Available in Tiny 8–Pin Plastic DIP Configuration — Features Smallest Frequency Generation Footprint in Industry**
- **Sophisticated Internal Loop–Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters**
- **Ideally Suited for VGA/EGA, Super VGA, and 8514 Graphic Applications**
- **Device Selection Tables Fit Most Popular Chip Sets**
- **Low–Power, High–Speed 1.25µ CMOS Technology**
- **5–Volt Operation**

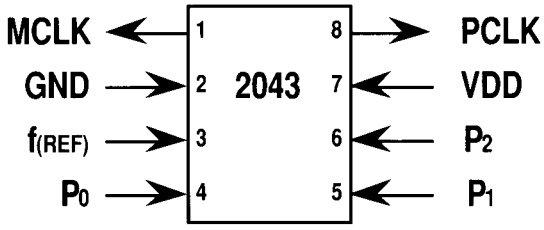
ICD2043 Dual VGA Clock Generator w/Fixed Memory Clock Block Diagram



Pixel Clock Selection Table Available Frequencies (MHz)		
14.31818	32.514	57.2727
16.257	36.0	65.0
25.175	40.0	80.0
28.332	44.9	
32.0	50.35	

Memory Clock Selection Table Available Frequencies (MHz)		
25.0	32.0	44.0
28.0	36.0	48.0
30.0	40.0	

Pin Descriptions



Signal Descriptions

Signal	Pin Number	Signal Function
MCLK	1	Memory Clock Oscillator Output (see Memory Clock Selection Table for specific frequency)
GND	2	Ground
$f_{(REF)}$	3	Input Reference Oscillator (nominally 14.31818 MHz derived from PC system bus.)
P_0	4	Input Pixel Clock Selection Signal
P_1	5	Input Pixel Clock Selection Signal
P_2	6	Input Pixel Clock Selection Signal
VDD	7	+5 Volts
PCLK	8	Pixel Clock Oscillator Output (see Pixel Clock Selection Table)

General

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of these oscillators required to build such multi–function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2043 Dual VGA Clock Generator supports new designs using the newer graphic chip sets which generate output frequency select information. The ICD2043 features two independent clock outputs for the pixel clock and the memory clock. The pixel clock output values are chosen via select lines. Additional features include a tiny 8–pin package and direct support for popular PC–AT chip set selection decodes.

PCLK Pixel Clock Oscillator Selection

The output frequency value of the pixel clock oscillator is selected by the three pixel clock selection inputs: P_0, P_1, and P_2. This feature allows the ICD2043 to support different video configurations. The selection table for the different pixel clock ROM decode options are shown below:

P_2	P_1	P_0	Pixel Clock ROM Option A	Pixel Clock ROM Option B
0	0	0	80.00000	50.35000
0	0	1	65.00000	44.90000
0	1	0	n/a	65.00000
0	1	1	32.51400	36.00000
1	0	0	25.17500	25.17500
1	0	1	28.33200	28.33200
1	1	0	36.00000	57.27270
1	1	1	40.00000	40.00000

[Note: 80MHz operation is only available in the ICD2043B speed selected part.]

At any time during operation the selection lines can be changed to select a different frequency. The output will settle to the new frequency value after a short transition period.

MCLK Memory Clock Oscillator Selection

The output frequency value of the memory clock oscillator is fixed. Different MCLK values may be ordered by the appropriate part number. The various clock options are shown below:

Desired MCLK Value	Memory Clock Order Number
48.00000	1
40.00000	2
30.00000	3
25.00000	4
28.00000	5
32.00000	6
44.00000	7
36.00000	8

PC System Bus Reference Clock

Normal operation requires a nominal 14.31818 MHz reference signal which comes from the PC system bus. In modern PC designs, this signal is stable enough for use with the ICD2043.

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2043.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher dot clock frequencies above 50MHz.

A full power and ground plane layout should be employed both under and around the IC package. The power pin should be bypassed to ground with a 0.1μf multi–layer ceramic capacitor and a 2.2μf/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin.

The designer should also avoid routing the two output traces of the ICD2043 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2043 closest to the device requiring the highest frequency. If the high–frequency clocks must be routed to board extremes, the ICD2031 distributed 'satellite' oscillators should be considered.

Circuit Description

Each oscillator block is a classical phase–locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 Mhz (as derived from the PC system bus) and goes into a "divide–by–n" block. The resultant signal becomes the reference frequency for the phase–locked loop circuitry.

The phase–locked loop is a feedback system which phase matches the reference signal and the variable 'synthesized' signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately 'lock–on' to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal 'loop filter' provides stability and damping.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

The parts use center pins to deliver power and ground to the die instead of the more conventional corner pins. The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground–bounce and output crosstalk.

Stability and "Bit–Jitter"

The long–term frequency stability of the IC DESIGNS phase–locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short–term stability (also called "bit–jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of "bit–jitter". The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low–gain VCO's and sufficient loop filtering are design elements specifically included to minimize this "bit–jitter". The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2043 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures the loop filter will track the same process variations as does the VCO. With the ICD2043, no manufacturing "tweaks" to external filter components are required as is the case with external "de–coupled" filters.

Use with Specific Manufacturer's Chip Sets

The ICD2043 is designed to be directly compatible with most of the commercially available graphic chip sets. Please call for applications information on the use of this device with a particular graphics chip set.

Ordering Information

Part Number	Speed Designation	Package Type	Temperature Range
ICD2043	A – 65MHz	P – 8–Pin Plastic DIP	C – Commercial (0°C – +70°C)
	B – 80MHz	C – 8–Pin Ceramic DIP	

Pixel Clock ROM Option	Memory Clock Value
A	1 = 48 MHz
B	2 = 40 MHz
	3 = 30 MHz
	4 = 25 MHz
	5 = 28 MHz
	6 = 32 MHz
	7 = 44 MHz
	8 = 36 MHz

Example: order *ICD2043APC–A8* for the 65MHZ ICD2043, 8–pin plastic DIP, commercial temperature range device which utilizes the Pixel Clock ROM Option A table of decodes and has a fixed 36MHz memory clock.

Electrical Data

Maximum Ratings

Name	Description	Min	Max	Units
VCC	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input Voltage with respect to GND	–0.5	VCC + 0.5	Volts
T_{OPER}	Operating Temperature	0	+70	°C
T_{STOR}	Storage Temperature	–65	+150	°C
T_{SOL}	Max Soldering Temperature (10 sec)		+260	°C
T_J	Junction Temperature		+125	°C
P_{DISS}	Power Dissipation		125	mWatts

DC Characteristics

VCC = +5V ±10%

0°C ≤ T_{CASE} ≤ +70°C

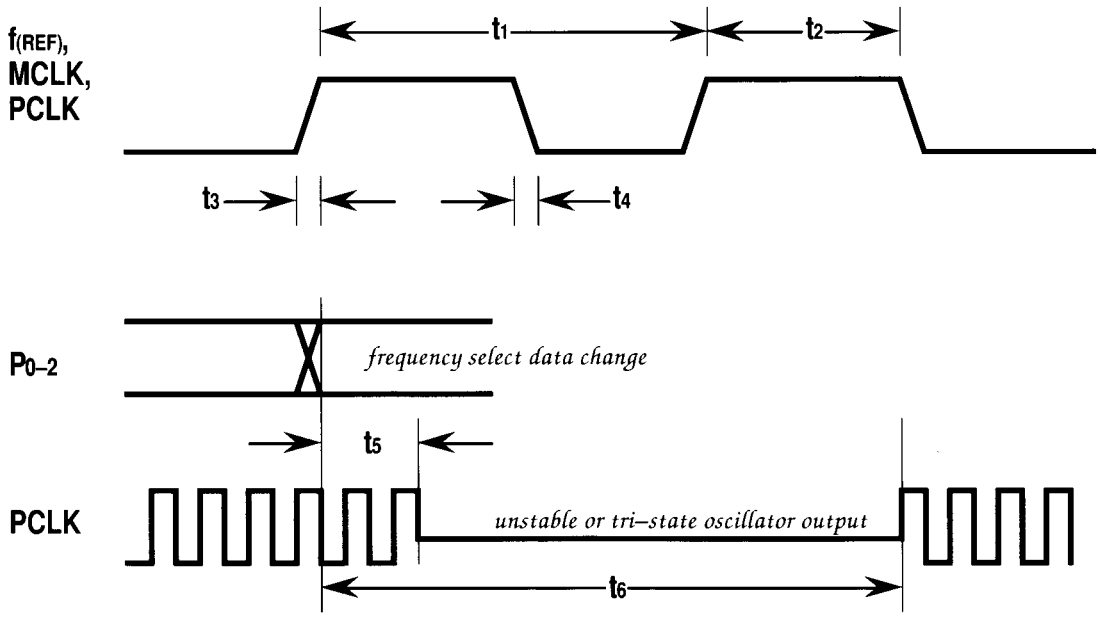
Name	Description	Min	Max	Units	Conditions
V_{IH}	High–level input voltage	2.0		Volts	
V_{IL}	Low–level input voltage		0.8	Volts	
V_{OH}	High–level output voltage	2.4		Volts	I_{OH} = -4.0 ma
V_{OL}	Low–level output voltage		0.4	Volts	I_{OL} = 4.0 ma
I_{IH}	Input high current		2.5	µa	V_{IH} = 4.6 v
I_{IL}	Input low current		-500	µa	V_{IL} = 0.4 v
I_{OL}	Output leakage current		2.5	µa	
I_{CC}	Power supply current		25	ma	
C_{IN}	Input Capacitance		10	pf	

AC Characteristics

VCC = +5V ±10%

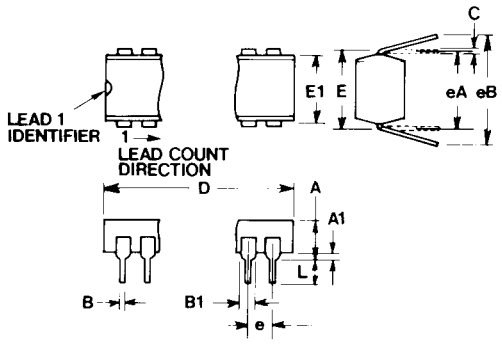
0°C ≤ T_{CASE} ≤ +70°C

Symbol	Name	Description	Min	Max	Units
t_1	ref freq	Reference Oscillator nominal value		14.31818	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as t_2/t_1	45%	55%	
t_3	rise time	Rise time for the output oscillators into a 25pf load		3	ns
t_4	fall time	Fall time for the output oscillators into a 25pf load		3	ns
t_5	clk unstable	Time the output oscillators remain valid after the P_{0-2} select signals change value		0	ns
t_6	clk stable	Time required for the output oscillators to become valid after P_{0-2} select signals change value	0.1	15	msec



Packaging Information

PDIP Outline



SYMBOL	LEAD COUNT 8 MIN	MAX
A	155	160
A1	015	—
B	018	022
B1	050	070
C	008	012
D	348	390
E	290	310
E1	220	270
e	100	TYP
eA	290	—
eB	—	310
L	100	—

(Dimensions in Inches)

IC DESIGNS
12020 — 113th Ave NE
Kirkland, WA 98034
206 / 821– 9202
Fax 206 / 823 – 8898