DATA SHEET

M 65890

16 K × 4
HIGH SPEED BICMOS SRAM
SEPARATE I/O

FEATURES

- **BICMOS FOR OPTIMUM SPEED/POWER**
- **HIGH SPEED**
  COMMERCIAL: 8/9/10/12 ns (max)
  MILITARY: 10/12/15 ns (max)
- **LOW ACTIVE POWER**
  735 mW
- **LOW STANDBY POWER**
  263 mW
- **SEPARATE INPUTS/OUTPUTS**
- **TTL-COMPATIBLE INPUTS AND OUTPUTS**
- **CAPABLE OF WITH STANDING GREATER THAN 2001 V ELECTROSTATIC DISCHARGE**

INTRODUCTION

The M-65890 is high-performance BICMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have a $\overline{CE}$ power-down feature, reducing the power consumption by 67 % when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are all LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and $\overline{OE}$ LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

The output pins remain in high-impedance state when write enable ($\overline{WE}$) is LOW or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) is HIGH, or $\overline{OE}$ if HIGH.

For military/space applications that demand superior levels of performance and reliability the M-65890 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

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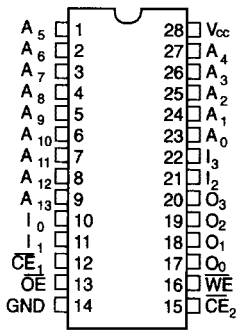
INTERFACE

PIN CONFIGURATION

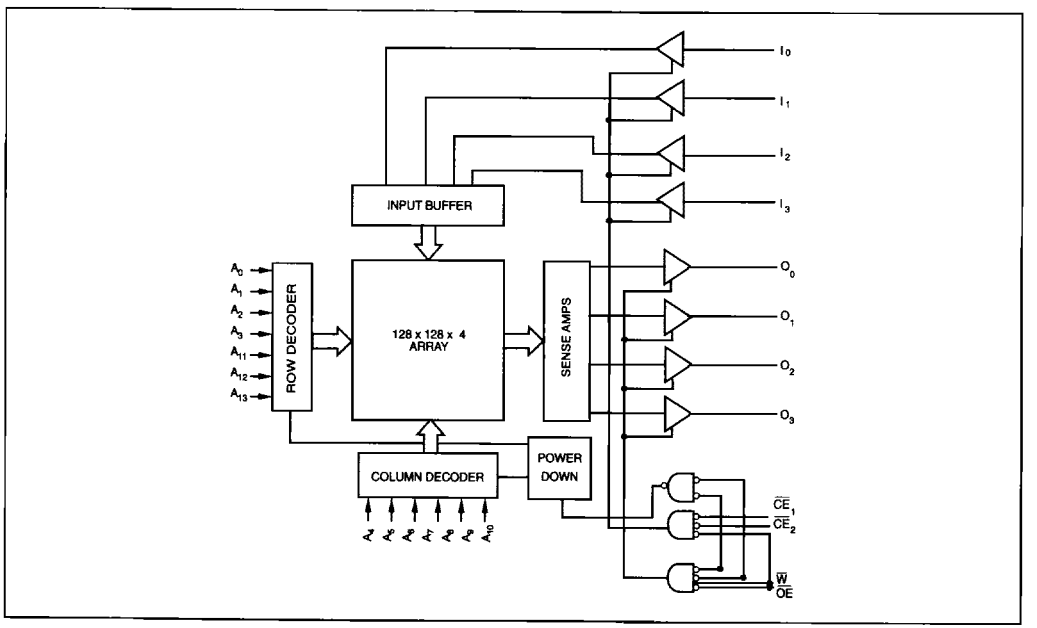
Plastic 300 mils 28 pins DIL(*)
Ceramic 300 mils 28 pins DIL
SOJ 300 mils 28 pins



(*) On Request

Pinout DIL/SOJ (Top View)

BLOCK DIAGRAM



SELECTION GUIDE

		M-65890-08	M-65890-09	M-65890-10	M-65890-12	M-65890-15
Maximum Access Time (ns)		8	9	10	12	15
Maximum Operating Current (mA)	Commercial	140	130	130	120	
	Military			145	140	135
Maximum Standby Current (mA)	Commercial	50	50	40	40	
	Military			60	55	50

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested).

Storage Temperature ..... – 65 °C to + 150 °C
Ambient Temperature with Power Applied ..... – 55 °C to + 125 °C
Supply Voltage to Ground Potential ..... – 0.5 V to + 7.0 V
DC Voltage Applied to Outputs in High Z State ..... – 0.5 V to + 7.0 V
DC Input Voltage[1] ..... – 3.0 V to + 7.0 V
Output Current into Outputs (Low) ..... 20 mA
Static Discharge Voltage ..... > 2001 V (per MIL-STD-833, Method 3015)
Latch-Up Current ..... > 200 mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	– 0 °C to + 70 °C	– 08, – 09 5 V ± 5 %
		– 10, – 12 5 V ± 10 %
Military (2)	– 55 °C to + 125 °C	5 V ± 10 %

ELECTRICAL CHARACTERISTICS Over the Operating Range

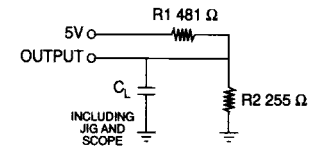
PARAMETERS	DESCRIPTION	TEST CONDITIONS			M-65890-08		M-65890-09		M-65890-10		M-65890-12		M-65890-15		UNITS
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = – 4.0 mA	Com'l	2.4		2.4		2.4		2.4				V
			I_{OH} = – 2.0 mA	Mil					2.4		2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled			– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		140		130		130		120			mA
				Mil						145		140		135	mA
I_{SB}	$\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ V_{IH} I_{OUT} = 0 mA		Com'l		50		50		40		40			mA
				Mil						60		55		50	mA

CAPACITANCE[3]

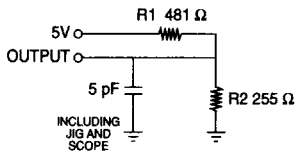
PARAMETER	DESCRIPTION	TEST CONDITIONS	MAXIMUM[4]	UNITS
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz V_{CC} = 5.0 V	5	pF
C_{OUT}	Output capacitance		7	pF

Notes : 1. VIL (min) = 3.0 V for pulse width < 20 ns
2. T_A is the "instant on" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except CERDIP, which has maximum of C_{IN} = 8 pF, C_{OUT} = 9 pF.

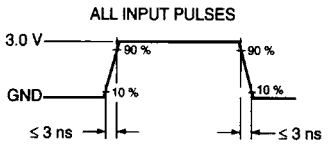
AC TEST LOADS AND WAVEFORMS



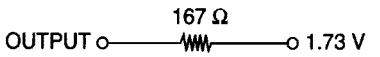
(a)



(b)



Equivalent to : THEVENIN EQUIVALENT



SWITCHING CHARACTERISTICS Over the Operating Range[5]

PARAMETERS	DESCRIPTION	M-65890-08		M-65890-09		M-65890-10		M-65890-12		M-65890-15		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
TAVAV	Read Cycle Time	8		9		10		12		15		ns
TAVQV	Address to Data Valid		8		9		10		12		15	ns
TAVQX	Output Hold from Address Change	2.5		2.5		2		3		3		ns
TELQV	$\overline{CE}$ LOW to Data Valid		8		9		10		12		15	ns
TGLQV	$\overline{OE}$ LOW to Data Valid		4.2		4.5		5		6		8	ns
TGLQX	$\overline{OE}$ LOW to Low Z	1.5		1.5		2		2		3		ns
TGHQZ	$\overline{OE}$ HIGH to High Z[6]		4		5		5		6		7	ns
TELQX	$\overline{CE}$ LOW to Low Z[5]	2		2		2		3		3		ns
TEHQZ	$\overline{CE}$ HIGH to High Z[6, 7]		4		5		5		6		7	ns
READ CYCLE												
TAVAV	Write cycle Time	8		9		10		12		15		ns
TELWH	$\overline{CE}$ LOW to white End	7		8		8		8		10		ns
TAVWH	Address Set-up to White End	7		8		8		8		10		ns
TWHAX	Address Set-Up to White End	0		0		0		0		0		ns
TAVWL	Address Set-Up to White Start	0		0		0		0		0		ns
TWLWH	$\overline{WE}$ Pulse Width	6.5		7		8		8		10		ns
TDVWH	Data Set-Up to White End	4		4.5		5		6		7		ns
TWHDX	Data Hold from White End	0		0		0		0		0		ns
TWHQX	$\overline{WE}$ HIGH to Low Z	2		2		2		2		3		ns
TWLQZ	$\overline{WE}$ LOW to High Z[6]		4		5		5		6		7	ns

Notes : 5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.

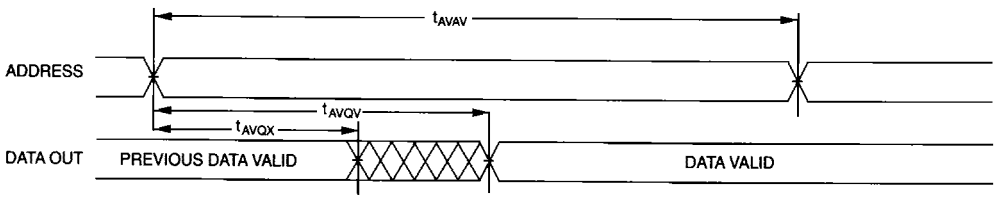
6. Specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is mesured ± 200 mV from steady stage voltage.

7. At any given temperature and voltage condition, t_{EHQZ} is less than t_{ELQX} for any given device, these parameters are guaranteed and not 100 % tested.

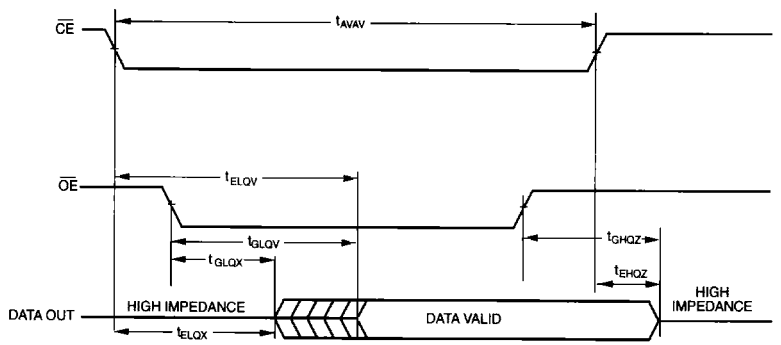
8. The internal write time of the memory is defined by the overlap of $\overline{CE_1}$ LOW, $\overline{CE_2}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

SWITCHING WAVEFORMS

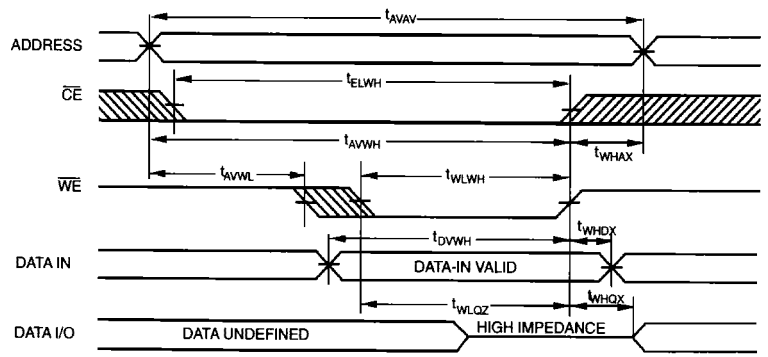
TIMING WAVEFORM OF READ CYCLE N° 1 (9, 10, 13)



TIMING WAVEFORM OF READ CYCLE N° 2 (9, 11, 13)



WRITE CYCLE N° 1 ($\overline{WE}$ controlled) (8, 13)



Notes : 9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE_1}$, $\overline{CE_2}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE_1}$ and $\overline{CE_2}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remain in a high-impedance state..
13. Both $\overline{CE_1}$ and $\overline{CE_2}$ are represented by $\overline{CE}$ in the switching characteristics and waveform section.

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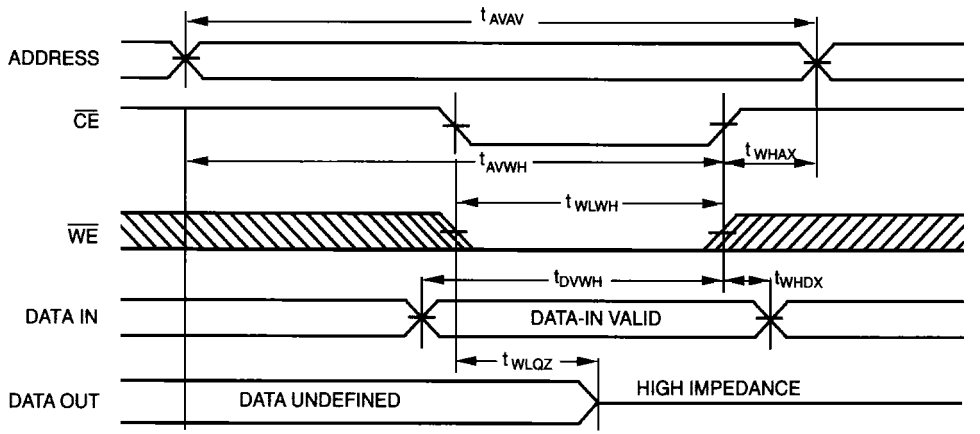
SWITCHING WAVEFORMS (continued)

TIMING WAVEFORM OF WRITE CYCLE N° 2 (CE controlled) (8, 12, 13)



M-65890 TRUTH TABLE

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	OUTPUTS	INPUTS	MODE
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	X	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

ORDERING INFORMATION

TEMPERATURE RANGE		PACKAGE		DEVICE		SPEED
C	M	UI	—	65890	—	12

C = Commercial, 0° to + 70°C
M = Military, – 50° to + 125°C

0 : chip form
1P : Ceramic 28 pins DIL
(*) 3P : Plastic 28 pins DIL
UI : SOJ 28 pins

16K x 4
HIGH SPEED STATIC RAM
SEPARATE I/O

08 : 8 ns
09 : 9 ns
10 : 10 ns
12 : 12 ns
15 : 15 ns

(*) On request. Consult sales.