



Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16952AT/BT/CT/ET
IDT54/74FCT162952AT/BT/CT/ET
IDT54/74FCT162H952AT/BT/CT/ET

FEATURES:

• Common features:

- 0.5 MICRON CMOS Technology
- **High-speed, low-power CMOS replacement for ABT functions**
- **Typical tsk(o) (Output Skew) < 250ps**
- **Low input and output leakage ≤ 1μA (max.)**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
- Extended commercial range of -40°C to +85°C

• Features for FCT16952AT/BT/CT/ET:

- High drive outputs (-32mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"
- Typical VOLP (Output Ground Bounce) < 1.0V at VCC = 5V, TA = 25°C

• Features for FCT162952AT/BT/CT/ET:

- Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

• Features for FCT162H952AT/BT/CT/ET:

- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors

DESCRIPTION:

The FCT16952AT/BT/CT/ET and FCT162952AT/BT/CT/ET

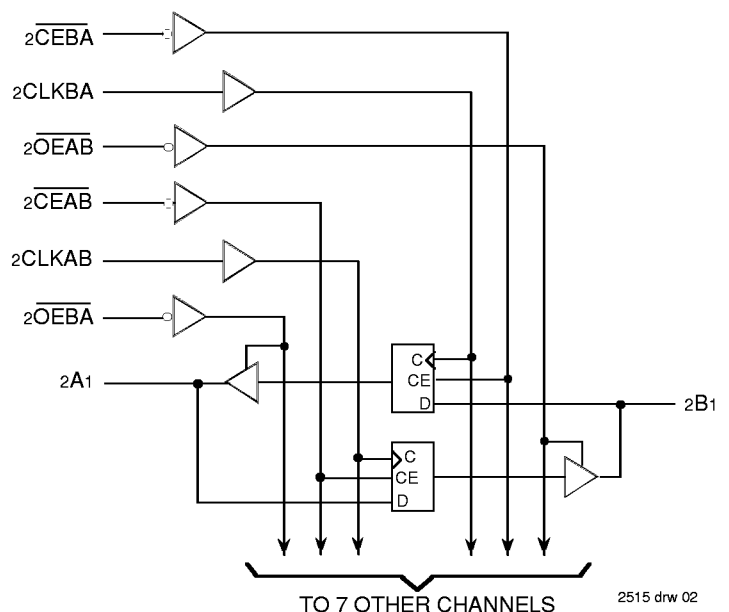
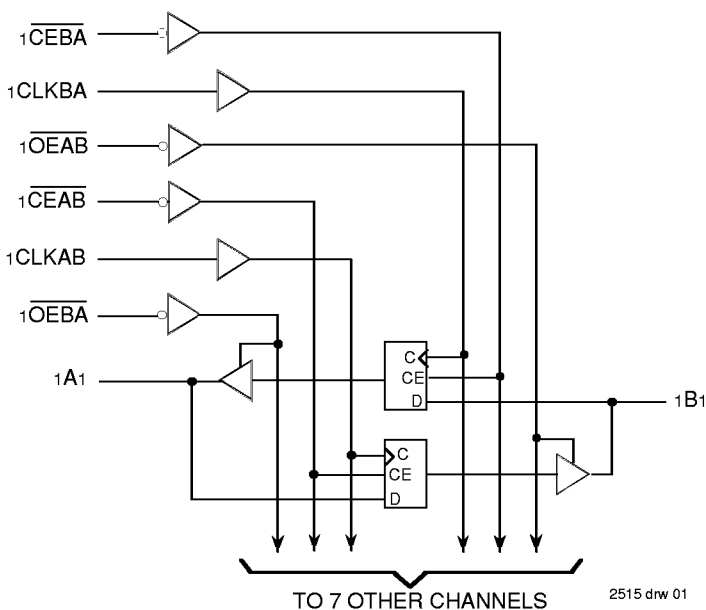
ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable (\overline{xCEAB}) must be LOW to enter data from the A port. \overline{xCLKAB} controls the clocking function. When \overline{xCLKAB} toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. \overline{xOEAB} performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using \overline{xCEBA} , \overline{xCLKBA} , and \overline{xOEBA} inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

The FCT16952AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability allowing "live insertion" of boards when used as backplane drivers.

The FCT162952AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162952AT/BT/CT/ET are plug-in replacements for the FCT16952AT/BT/CT/ET and ABT16952 for on-board bus interface applications.

The FCT162H952AT/BT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

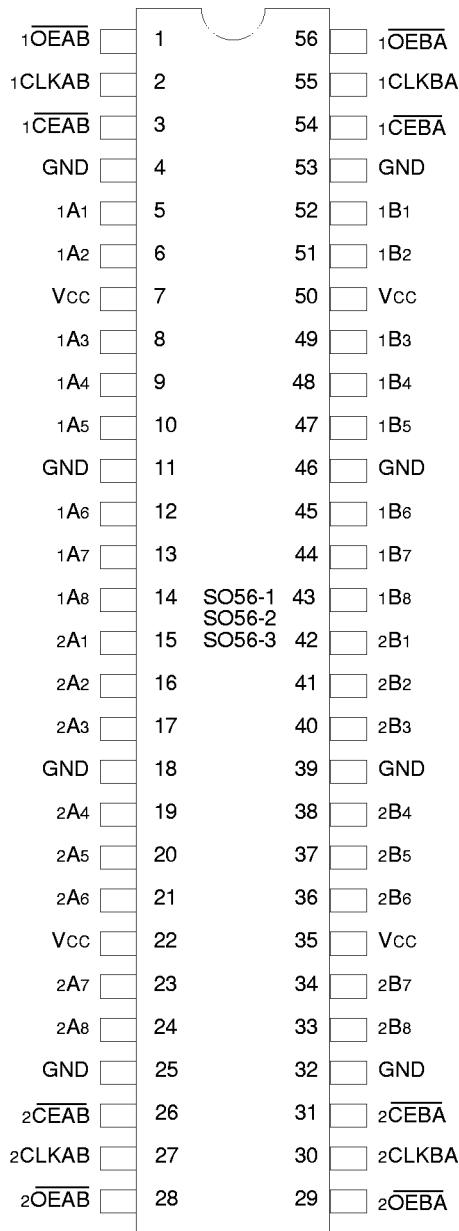


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND INDUSTRIAL TEMPERATURE RANGES

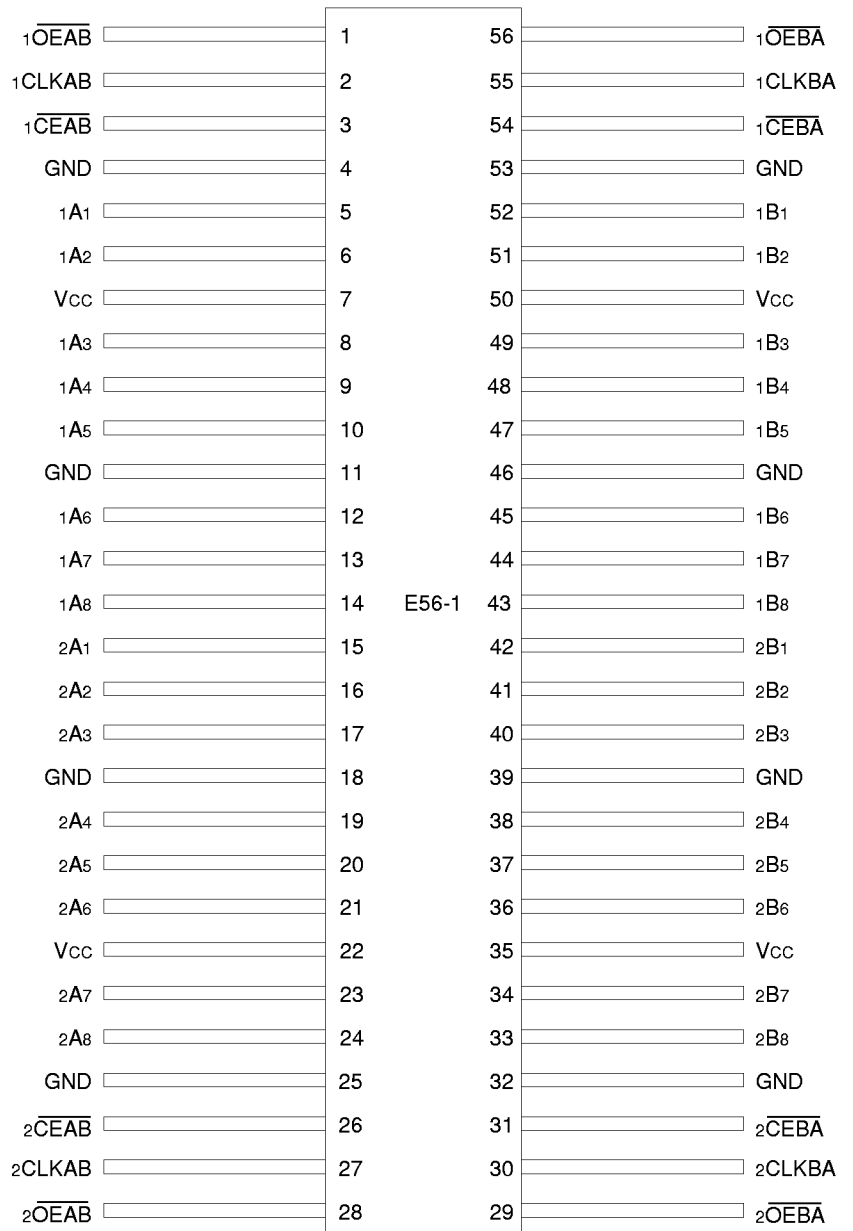
FEBRUARY 1997

PIN CONFIGURATIONS



SSOP/
TSSOP/TVSOP
TOP VIEW

2515 drw 03



CERPACK
TOP VIEW

2515 drw 04

PIN DESCRIPTION

Pin Names	Description
\overline{xOEAB}	A-to-B Output Enable Input (Active LOW)
$\overline{xOEB A}$	B-to-A Output Enable Input (Active LOW)
\overline{xCEAB}	A-to-B Clock Enable Input (Active LOW)
\overline{xCEBA}	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

2515 tbl 01

1. On FCT16xH952T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
$V_{TERM(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
$V_{TERM(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

2515 lmk 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE^(1,3)

Inputs				Outputs
\overline{xCEAB}	xCLKAB	\overline{xOEAB}	xAx	xBx
H	X	L	X	B ⁽²⁾
X	L	L	X	B ⁽²⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:

2515 tbl 02

- A-to-B data flow is shown: B-to-A data flow is similar but uses, \overline{xCEBA} , xCLKBA, and $\overline{xOEB A}$.
- Level of B before the indicated steady-state input conditions were established.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
Z = High-impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

NOTE:

2515 lmk 04

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾		—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$ $V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins) ⁽⁵⁾		—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$ $V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾	-80	-140	-250	mA
V_H	Input Hysteresis	—	—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}	—	5	500	μA

2515 Ink 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16952T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I_O	Output Drive Current	$V_{CC} = \text{Max.}$, $V_O = 2.5\text{V}$ ⁽³⁾	-50	—	-180	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.4	3.5	—	V
			$I_{OH} = -24\text{mA MIL.}$ $I_{OH} = -32\text{mA COM'L.}$ ⁽⁴⁾	2.0	3.0	—	V
			$I_{OL} = 48\text{mA MIL.}$ $I_{OL} = 64\text{mA COM'L.}$	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$	—	—	± 1	μA	

2515 Ink 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162952T

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾	60	115	200	mA	
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{OUT} = 1.5\text{V}$ ⁽³⁾	-60	-115	-200	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

2515 Ink 07

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, VCC = 5.0V ± 10%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I _{IL}	Input LOW Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _{CC} = Max.	V _I = GND	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I _{BHH} I _{BHL}	Bus Hold Sustain Current ⁽⁴⁾	Bus-hold Input	V _{CC} = Min.	V _I = 2.0V	-50	—	—	μA
				V _I = 0.8V	+50	—	—	
I _{OZH}	High Impedance Output Current (3-State Output pins) ^(5,6)		V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}				V _O = 0.5V	—	—	±1	
V _{IK}	Clamp Diode Voltage		V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current		V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-250	mA
V _H	Input Hysteresis		—		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current		V _{CC} = Max., V _{IN} = GND or V _{CC}		—	5	500	μA

2515 Ink 08

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Pins with Bus-hold are identified in the pin description.
- The test limit for this parameter is ± 5μA at TA = -55°C.
- Does not include Bus-hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $\overline{xOEAB} \text{ or } \overline{xOEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (xCLKAB)}$ 50% Duty Cycle $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$ $\overline{xOEBA} = V_{CC}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}, \text{Outputs Open}$ $f_{CP} = 10\text{MHz (xCLKAB)}$ 50% Duty Cycle $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$ $\overline{xOEBA} = V_{CC}$ Sixteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.3	20.0 ⁽⁵⁾	

NOTES:

2515 tbl 09

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT16952AT/162952AT				FCT16952BT/162952BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
tPHL	xCLKAB, xCLKBA to xBx, xAx										
tPZH	Output Enable Time		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
tPZL	xOEBA, xOEAB to xAx, xBx										
tPHZ	Output Disable Time		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
tPLZ	xOEBA, xOEAB to xAx, xBx										
tsu	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	ns
th	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.5	—	ns
tsu	Set-up Time, HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
tw	Pulse Width HIGH or LOW xCLKAB or xCLKBA ⁽⁴⁾	3.0	—	3.0	—	3.0	—	3.0	—	ns	
tsk(o)	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	—	0.5	ns	

2515 tbl 10

Symbol	Parameter	Condition ⁽¹⁾	FCT16952CT/162952CT				FCT16952ET/162952ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	2.0	6.3	2.0	7.3	1.5	3.7	—	—	ns
tPHL	xCLKAB, xCLKBA to xBx, xAx										
tPZH	Output Enable Time		1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
tPZL	xOEBA, xOEAB to xAx, xBx										
tPHZ	Output Disable Time		1.5	6.5	1.5	7.5	1.5	3.6	—	—	ns
tPLZ	xOEBA, xOEAB to xAx, xBx										
tsu	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	1.5	—	—	—	ns
th	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		1.5	—	1.5	—	0	—	—	—	ns
tsu	Set-up Time, HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		3.0	—	3.0	—	2.0	—	—	—	ns
th	Hold Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		2.0	—	2.0	—	0	—	—	—	ns
tw	Pulse Width HIGH or LOW xCLKAB or xCLKBA ⁽⁴⁾	3.0	—	3.0	—	3.0	—	—	—	ns	
tsk(o)	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	—	—	ns	

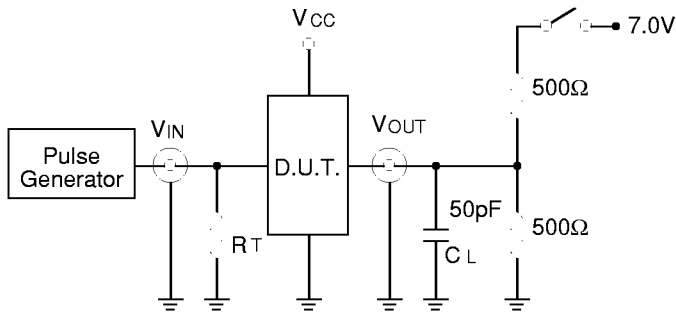
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

2515 tbl 11

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2515 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

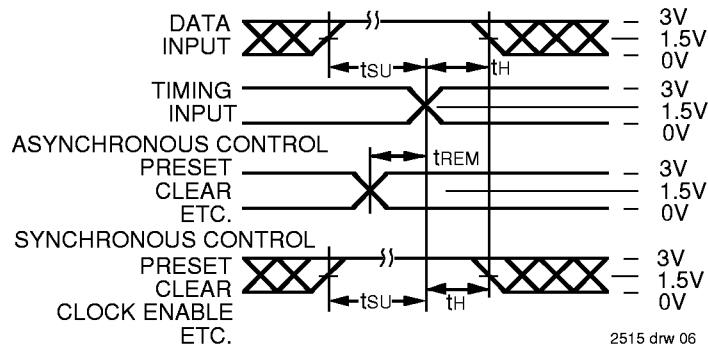
2515 Ink 12

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

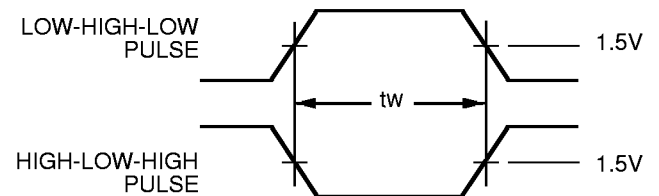
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



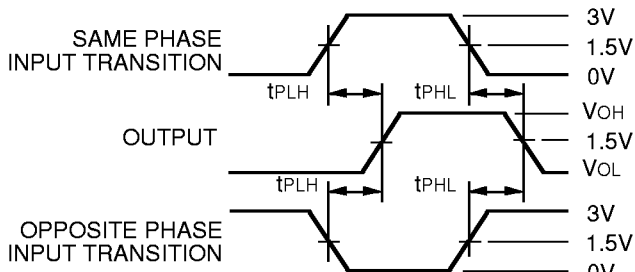
2515 drw 06

PULSE WIDTH



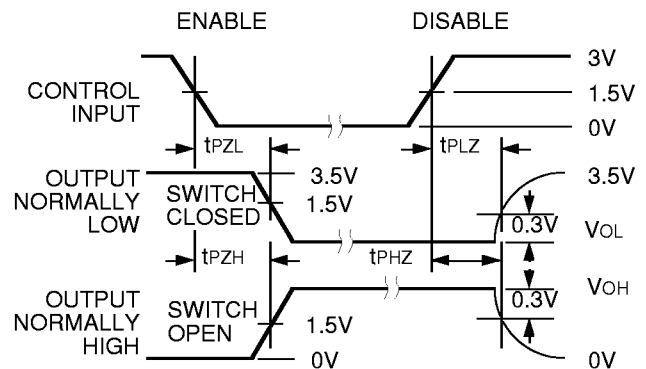
2515 drw 07

PROPAGATION DELAY



2515 drw 08

ENABLE AND DISABLE TIMES

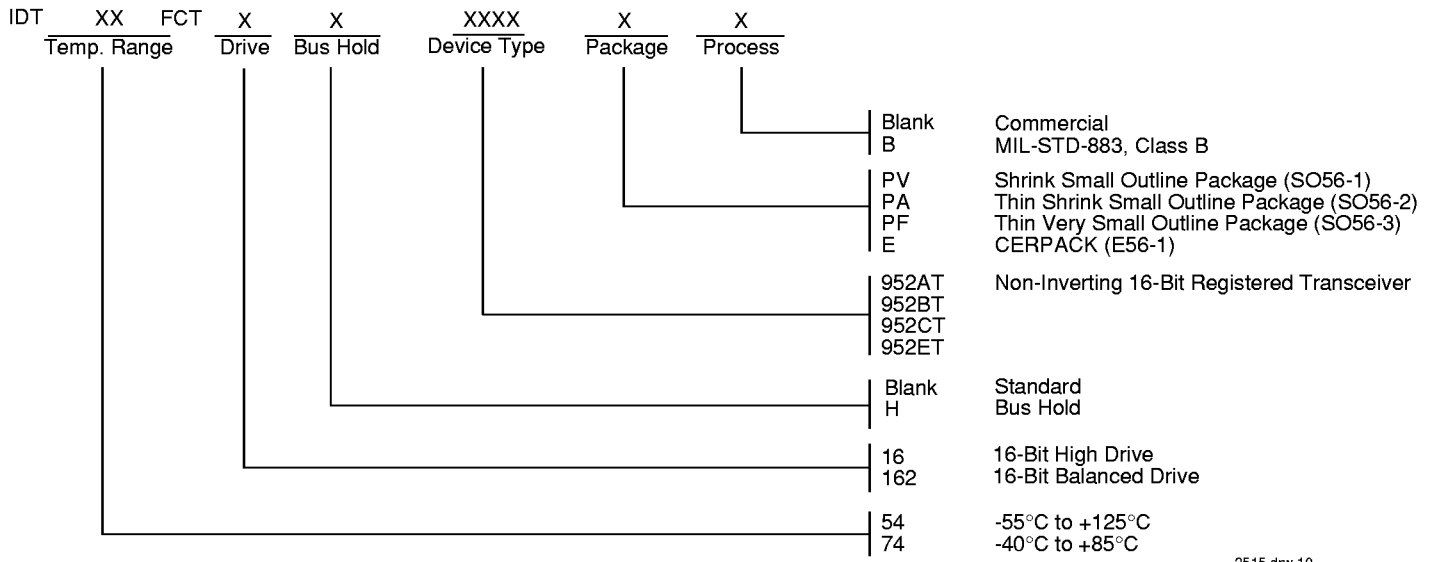


2515 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



2515 drw 10