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# HD74AC138/HD74ACT138

1-of-8 Decoder/Demultiplexer

# HITACHI

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## Description

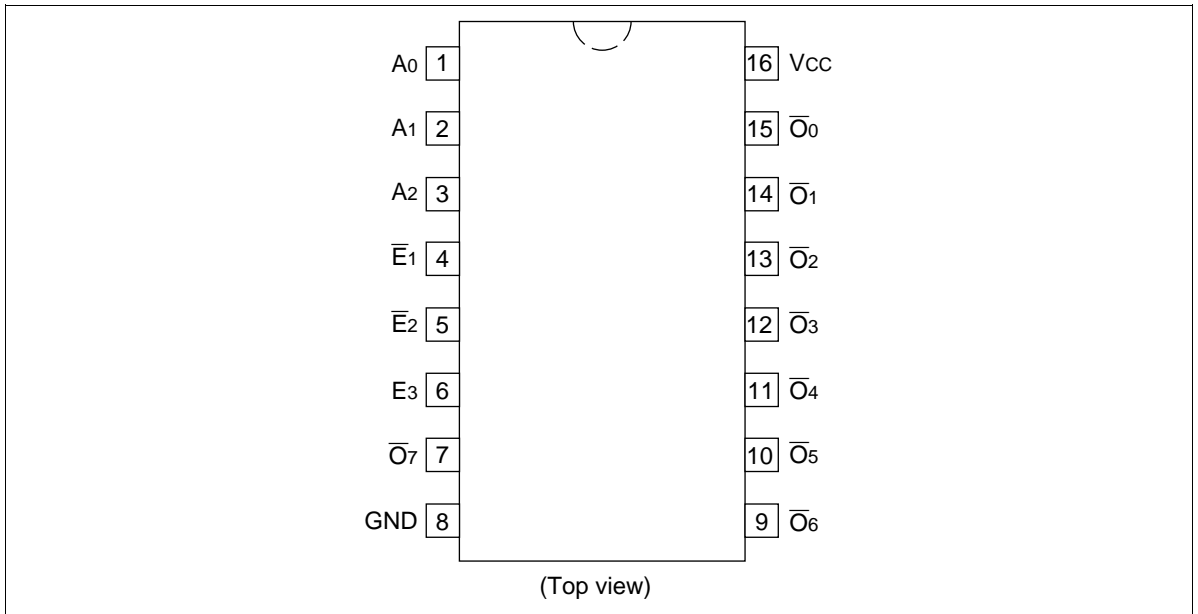
The HD74AC138/HD74ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three HD74AC138/HD74ACT138 devices or a 1-of-32 decoder using four HD74AC138/HD74ACT138 devices and one inverter.

## Features

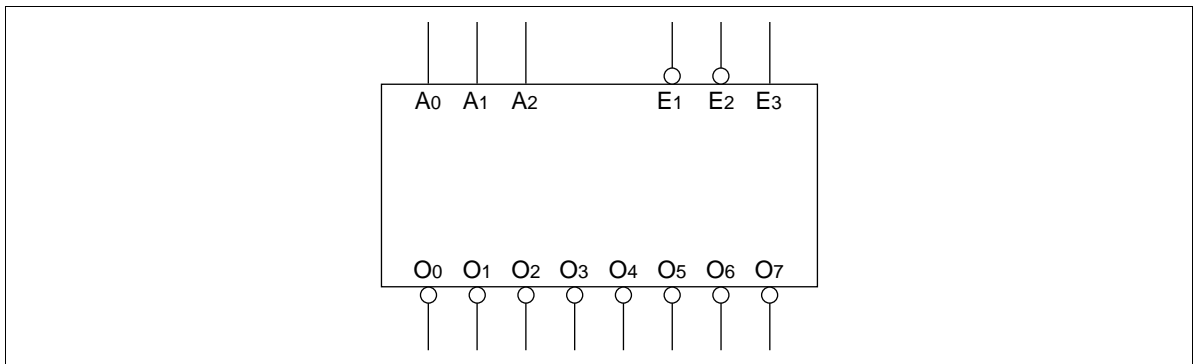
- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- HD74ACT138 has TTL-Compatible Inputs

# HD74AC138/HD74ACT138

## Pin Arrangement



## Logic Symbol



## Pin Names

- A<sub>0</sub> to A<sub>2</sub> Address Inputs
- $\bar{E}_1$  to  $\bar{E}_2$  Enable Inputs
- E<sub>3</sub> Enable Input
- $\bar{O}_0$  to  $\bar{O}_7$  Outputs

## Functional Description

The HD74AC138/HD74ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs ( $A_0, A_1, A_2$ ) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\overline{O}_0$  to  $\overline{O}_7$ ). The HD74AC138/HD74ACT138 features three Enable inputs, two active-Low ( $\overline{E}_1, \overline{E}_2$ ) and one active-High ( $E_3$ ). All outputs will be High unless  $\overline{E}_1$  and  $\overline{E}_2$  are Low and  $E_3$  is High. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four HD74AC138/HD74ACT138 devices and one inverter (See Figure a). The HD74AC138/HD74ACT138 can be used as an 8-output demultiplexer by using one of the active Low Enable inputs as the data input and the other Enable inputs as strobes. The Enables inputs which are not used must be permanently tied to their appropriate active-High or active-Low state.

## Truth Table

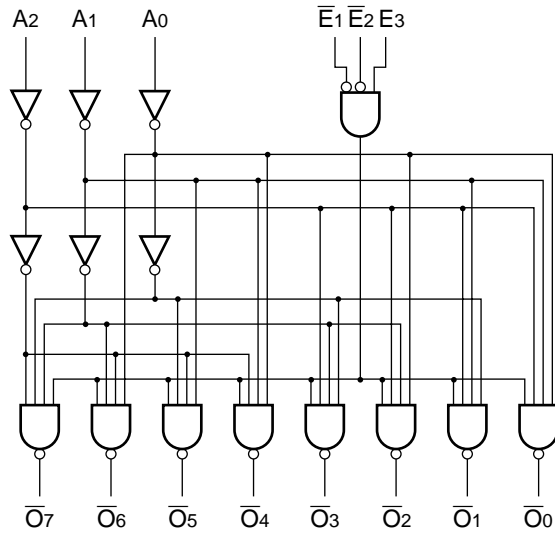
Inputs			Outputs										
$\overline{E}_1$	$\overline{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H : High Voltage Level

L : Low Voltage Level

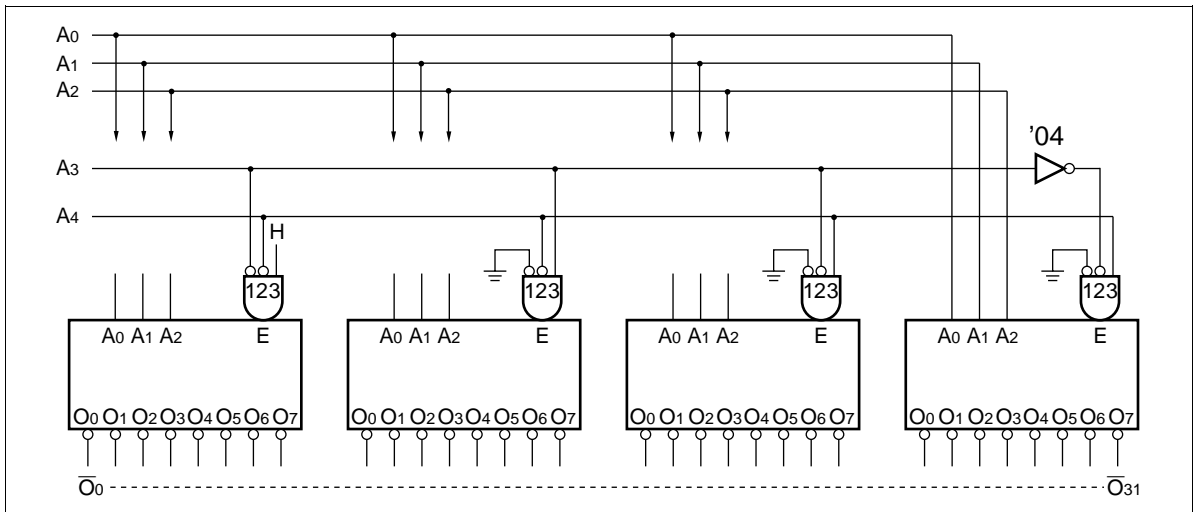
X : Immaterial

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure a: Expansion of 1-of-32 Decoding**



**DC Characteristics** (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu\text{A}$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$ , $T_a = 25^\circ\text{C}$
Maximum $I_{CC}$ /input (HD74ACT138)	$I_{CCT}$	1.5	mA	$V_{IN} = V_{CC} - 2.1\text{ V}$ , $V_{CC} = 5.5\text{ V}$ $T_a = \text{Worst case}$

**AC Characteristics: HD74AC138**

Item	Symbol	$V_{CC} (\text{V})^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	$t_{PLH}$	3.3	1.0	8.5	13.0	1.0	15.0	ns
$A_n$ to $\overline{O}_n$		5.0	1.0	6.5	9.5	1.0	10.5	
Propagation delay	$t_{PHL}$	3.3	1.0	8.0	12.5	1.0	14.0	ns
$A_n$ to $\overline{O}_n$		5.0	1.0	6.0	9.0	1.0	10.5	
Propagation delay	$t_{PLH}$	3.3	1.0	11.0	15.0	1.0	16.0	ns
$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		5.0	1.0	8.0	11.0	1.0	12.0	
Propagation delay	$t_{PHL}$	3.3	1.0	9.5	13.5	1.0	15.0	ns
$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	$t_{PLH}$	3.3	1.0	11.0	15.5	1.0	16.5	ns
$E_3$ to $\overline{O}_n$		5.0	1.0	8.0	11.0	1.0	12.5	
Propagation delay	$t_{PHL}$	3.3	1.0	8.5	13.0	1.0	14.0	ns
$E_3$ to $\overline{O}_n$		5.0	1.0	6.0	8.0	1.0	9.5	

Note: 1. Voltage Range 3.3 is  $3.3\text{ V} \pm 0.3\text{ V}$   
Voltage Range 5.0 is  $5.0\text{ V} \pm 0.5\text{ V}$

# HD74AC138/HD74ACT138

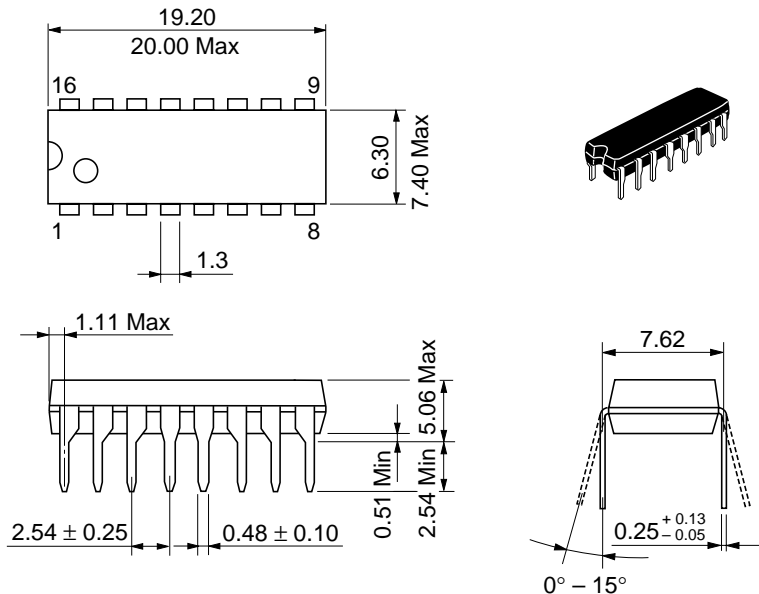
## AC Characteristics: HD74ACT138

Item	Symbol	$V_{CC}$ (V)* <sup>1</sup>	Ta = +25°C CL = 50 pF			Ta = -40°C to +85°C CL = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay An to $\bar{O}_n$	$t_{PLH}$	5.0	1.0	7.0	10.5	1.0	11.5	ns
Propagation delay An to $\bar{O}_n$	$t_{PHL}$	5.0	1.0	6.5	10.5	1.0	11.5	ns
Propagation delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$	$t_{PLH}$	5.0	1.0	8.0	11.5	1.0	12.5	ns
Propagation delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$	$t_{PHL}$	5.0	1.0	7.5	11.5	1.0	12.5	ns
Propagation delay $E_3$ to $\bar{O}_n$	$t_{PLH}$	5.0	1.0	8.0	12.0	1.0	13.0	ns
Propagation delay $E_3$ to $\bar{O}_n$	$t_{PHL}$	5.0	1.0	6.5	10.5	1.0	11.5	ns

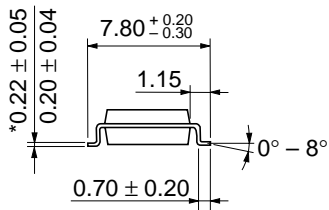
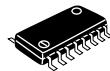
Note: 1. Voltage Range 5.0 is 5.0 V  $\pm$  0.5 V

## Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	$C_{IN}$	4.5	pF	$V_{CC} = 5.5$ V
Power dissipation capacitance	$C_{PD}$	60.0	pF	$V_{CC} = 5.0$ V



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

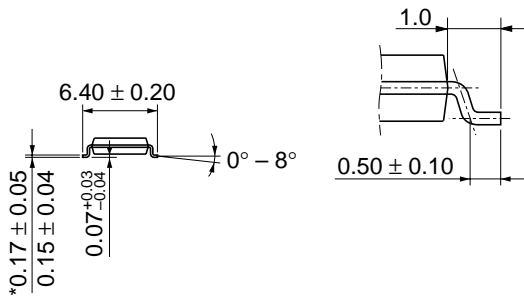
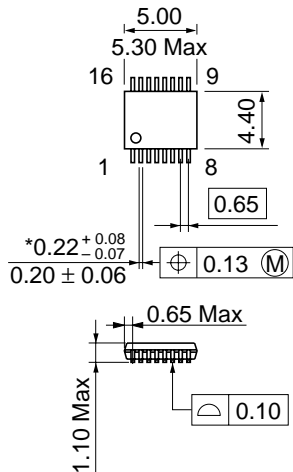
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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