SGS-THOMSON MICROELECTRONICS

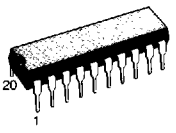
M54/74HC374/534 M54/74HC564/574

OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUT HC534/HC564 INVERTING - HC374/HC574 NON-INVERTING

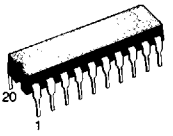
S G S-THOMSON

PRELIMINARY DATA

- HIGH SPEED
  f_{MAX} = 55 MHz (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374/534/564/574



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

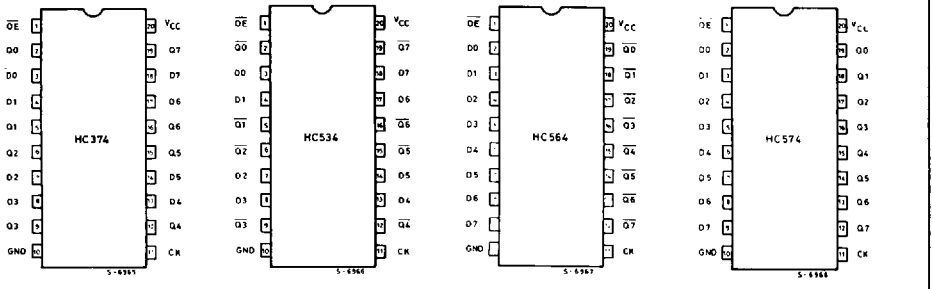
ORDERING NUMBERS:

M54HCXXX F1
M74HCXXX B1N
M74HCXXX F1
M74HCXXX C1
M74HCXXX M1

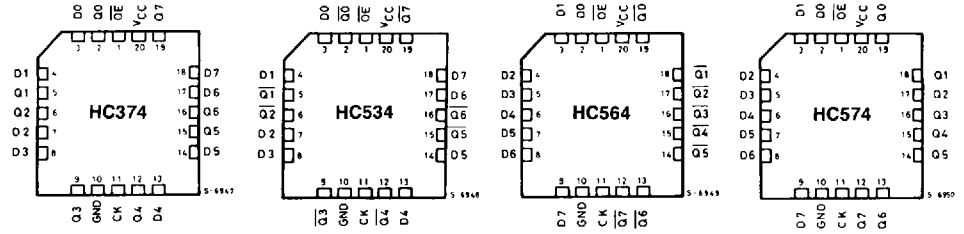
DESCRIPTION

The M54/74HC374, M54/74HC534, M54/74HC564 and M54/74HC574 are high speed CMOS OCTAL D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS fabricated with in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs (HC374 and HC574) or their complements (HC534 and HC564)
While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighbouring input/output pin layout. The HC374 and HC574 are identical, apart from pin layout as are the HC534 and HC564. The 3-state output configuration and the wide choice of outline make bus-organized systems simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



CHIP CARRIER S G S-THOMSON



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V: 0 to 1000 V_{CC} 4.5V: 0 to 500 V_{CC} 6 V: 0 to 400	ns

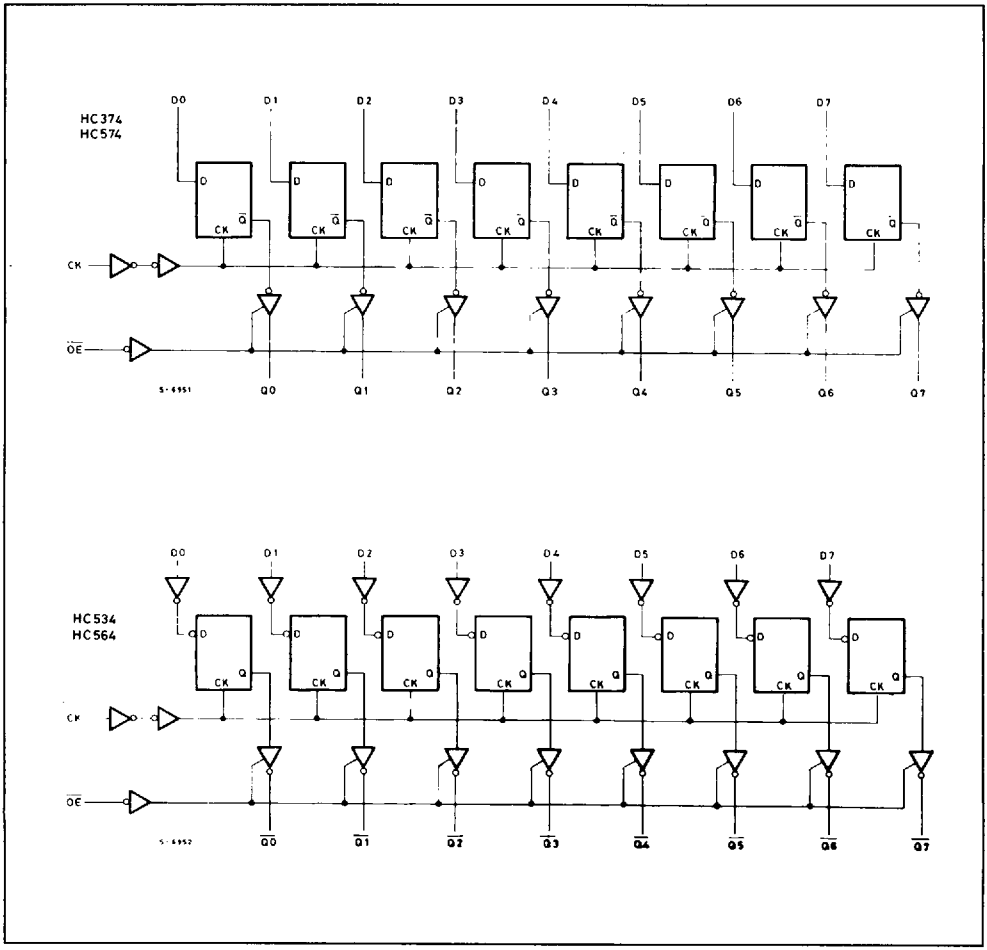
S G S-THOMSON

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374, HC574)	$\overline{Q}$ (HC534, HC564)
H	X	X	Z	Z
L	↓	X	NO CHANGE	NO CHANGE
L	↑	L	L	H
L	↑	H	H	L

X: DON'T CARE Z: HIGH IMPEDANCE

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	$-20\ \mu A$	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	$20\ \mu A$	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	± 0.5	—	± 5.0	—	± 10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4.0	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	24	60	—	75		90	ns
		4.5		—	8	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{PLH} t_{PHL}	Propagation Delay Time* (CK - Q, $\overline{Q}$)	2.0		—	88	175	—	220		265	ns
		4.5		—	22	35	—	44		53	
		6.0		—	19	30	—	37		44	
t_{PLH} t_{PHL}	Propagation Delay Time** (CK - Q, $\overline{Q}$)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	
f_{MAX}	Maximum Clock Frequency	2.0		6	12	—	5	—	4	—	MHz
		4.5		30	50	—	24	—	20	—	
		6.0		35	59	—	28	—	24	—	

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_s	Minimum Set-up Time*	2.0		—	40	100	—	125		150	ns
		4.5		—	10	20	—	25		30	
		6.0		—	9	17	—	21		26	
t_s	Minimum Set-up Time**	2.0		—	30	79	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_h	Minimum Hold Time*	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_h	Minimum Hold Time**	2.0		—	—	0	—	0	—	0	ns
		4.5		—	—	0	—	0	—	0	
		6.0		—	—	0	—	0	—	0	
t_{PZL} t_{PZH}	Output Enable Time*	2.0	R_L = 1KΩ	—	72	150	—	190	—	225	ns
		4.5		—	18	30	—	38	—	45	
		6.0		—	15	26	—	33	—	38	
t_{PZL} t_{PZH}	Output Enable Time**	2.0	R_L = 1KΩ	—	64	140	—	175	—	210	ns
		4.5		—	16	28	—	35	—	42	
		6.0		—	14	24	—	30	—	36	
t_{PZL} t_{PZH}	Output Disable Time*	2.0	R_L = 1KΩ	—	84	150	—	190	—	225	ns
		4.5		—	21	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
t_{PZL} t_{PZH}	Output Disable Time**	2.0	R_L = 1KΩ	—	84	150	—	190	—	225	ns
		4.5		—	21	30	—	38	—	45	
		6.0		—	18	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (1)	Power Dissipation Capacitance			—	51	—	—	—	—	—	pF

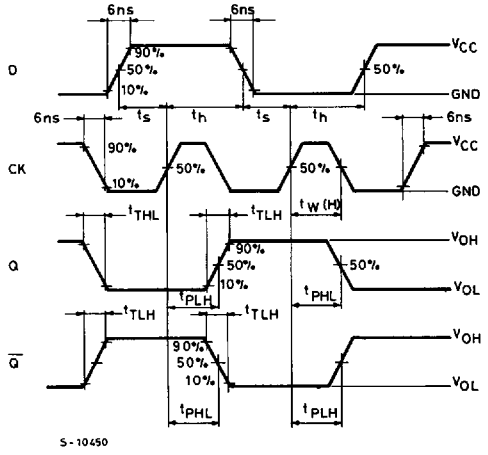
Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation:
$I_{CC\ (Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip-Flop)
And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation.
C_{PD} (TOTAL) = 34 + 17 × N [pF]

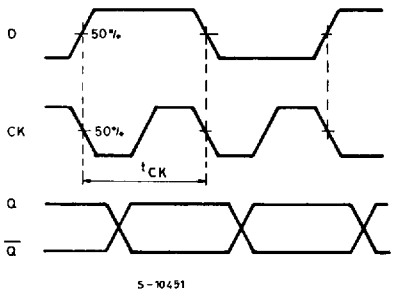
*: for HC374/534
**: for HC564/574

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{PLH}, t_{PHL}, t_s, t_h, t_w



f_{MAX}



CK DUTY:50%

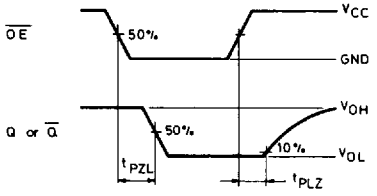
$f_{MAX} \frac{1}{t_{CK}}$

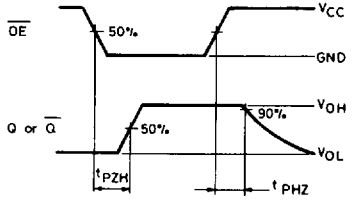
t_{PLZ}, t_{PZL}

The IKΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

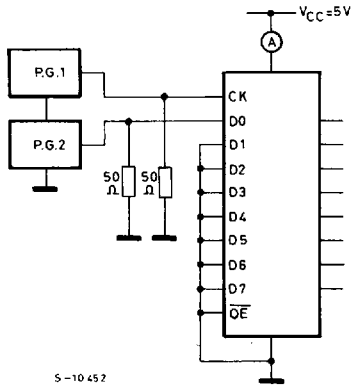
t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TEST CIRCUIT I_{CC} (Opr.) S G S-THOMSON



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.