

## DM74S112

### Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flop with Preset, Clear, and Complementary Outputs

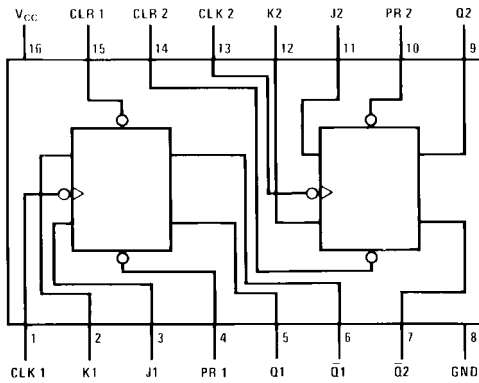
#### General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is HIGH or LOW without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

#### Ordering Code:

Order Number	Package Number	Package Description
DM74S112	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

#### Connection Diagram



#### Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

H = HIGH Logic Level

X = Either LOW or HIGH Logic Level

L = LOW Logic Level

↓ = Negative going edge of pulse.

Q<sub>0</sub> = The output logic level of Q before the indicated input conditions were established.

\* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (HIGH) level.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			-1	mA
$I_{OL}$	LOW Level Output Current			20	mA
$f_{CLK}$	Clock Frequency (Note 2)	0	125	80	MHz
$f_{CLK}$	Clock Frequency (Note 3)	0	80	60	MHz
$t_w$	Pulse Width (Note 2)	Clock HIGH	6		ns
		Clock LOW	6.5		
		Clear LOW	8		
		Preset LOW	8		
$t_w$	Pulse Width (Note 3)	Clock HIGH	8		ns
		Clock LOW	8		
		Clear LOW	10		
		Preset LOW	10		
$t_{SU}$	Setup Time (Note 4)(Note 5)	7↓			ns
$t_H$	Input Hold Time (Note 4)(Note 5)	0↓			ns
$T_A$	Free Air Operating Temperature	0		70	°C

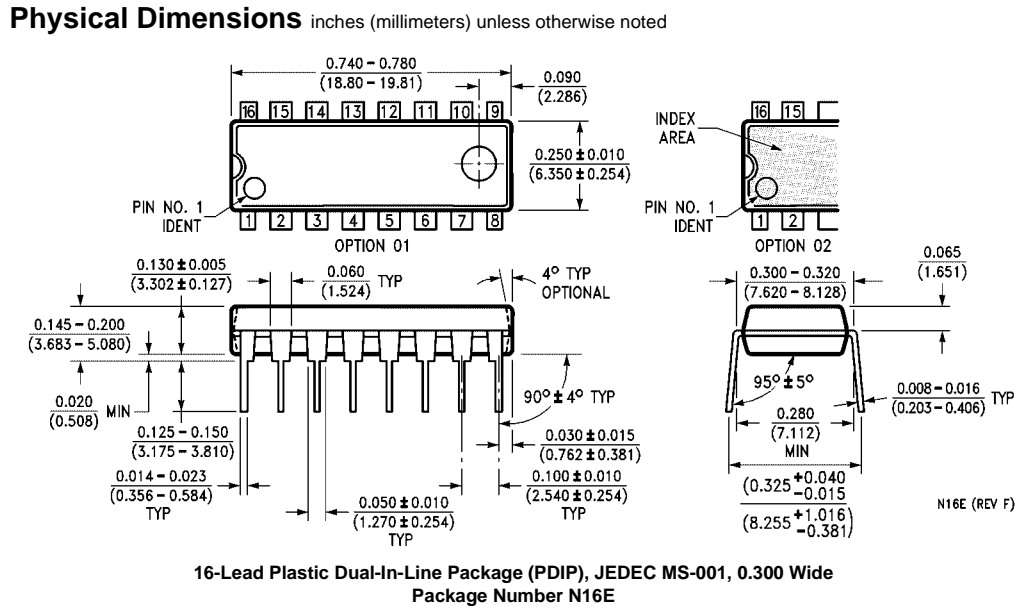
**Note 2:**  $C_L = 15$  pF,  $R_L = 280\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 3:**  $C_L = 50$  pF,  $R_L = 280\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 4:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 5:** The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Electrical Characteristics							
over recommended operating free air temperature (unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units	
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.2	V	
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.7	3.4		V	
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.5	V	
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}$			1	mA	
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$	J, K		50	$\mu\text{A}$	
			Clear		100		
			Preset		100		
			Clock		100		
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.5\text{V}$ (Note 7)	J, K		-1.6	mA	
			Clear		-7		
			Preset		-7		
			Clock		-4		
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 8)	-40		-100	mA	
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 9)		30	50	mA	
<p><b>Note 6:</b> All typicals are at <math>V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}</math>.</p> <p><b>Note 7:</b> Clear is tested with preset HIGH and preset is tested with clear HIGH.</p> <p><b>Note 8:</b> Not more than one output should be shorted at a time, and the duration should not exceed one second.</p> <p><b>Note 9:</b> With all outputs OPEN, <math>I_{CC}</math> is measured with the Q and <math>\bar{Q}</math> outputs HIGH in turn. At the time of measurement, the clock input is grounded.</p>							
Switching Characteristics							
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$							
Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
$f_{\text{MAX}}$	Maximum Clock Frequency		80		60		MHz
$t_{\text{PLH}}$	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		7		9	ns
$t_{\text{PHL}}$	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\bar{Q}$		7		12	ns
$t_{\text{PLH}}$	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		7		9	ns
$t_{\text{PHL}}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		7		12	ns
$t_{\text{PLH}}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		7		9	ns
$t_{\text{PHL}}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		7		12	ns



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**DM74S112**

## Dual Negative-Edge-Triggered J-K Flip-Flop with Preset Clear and Complementary Ou

Generic P/N 74S112

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## General Description

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## Features

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## Datasheet

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[DM74S112 Dual Negative-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs](#) (43 Kbytes; 29-JUL-00)

## Availability, Models, Samples & Pricing

Part Number	Grade	Package		Status	Models		Budgetary Pricing		Std Pack Size	Package Marking
		Type	# pins		SPICE	IBIS	Quantity	\$US ea		
DM74S112N	Comm	<a href="#">MDIP</a>	16	Full Production	N/A	N/A	1-24	\$0.60	N/A	\$Y&Z&4&DM74S1
							25-99	\$0.45		
							100-1000	\$0.36		
DM74S112CW	Comm	wafer		Preliminary	N/A	N/A		N/A	N/A	

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