NEC

MOS INTEGRATED CIRCUIT

# μPD42S18160, 4218160

## 16 M-BIT DYNAMIC RAM
## 1 M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

## Description

The μPD42S18160, 4218160 are 1,048, 576 words by 16 bits CMOS dynamic RAMs. The fast page mode and byte read/write mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the μPD42S18160 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

These are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

## Features

- 1,048,576 words by 16 bits organization
- Single +5.0 V ±10 % power supply
- Fast page mode
- Fast access and cycle time

| Part number | Power consumption Active (MAX.) | Access time (MAX.) | R/W cycle time (MIN.) | Fast page mode cycle time (MIN.) |
|---|---|---|---|---|
| μPD42S18160-60, 4218160-60 | 880 mW | 60 ns | 110 ns | 40 ns |
| μPD42S18160-70, 4218160-70 | 825 mW | 70 ns | 130 ns | 45 ns |

- The μPD42S18160 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

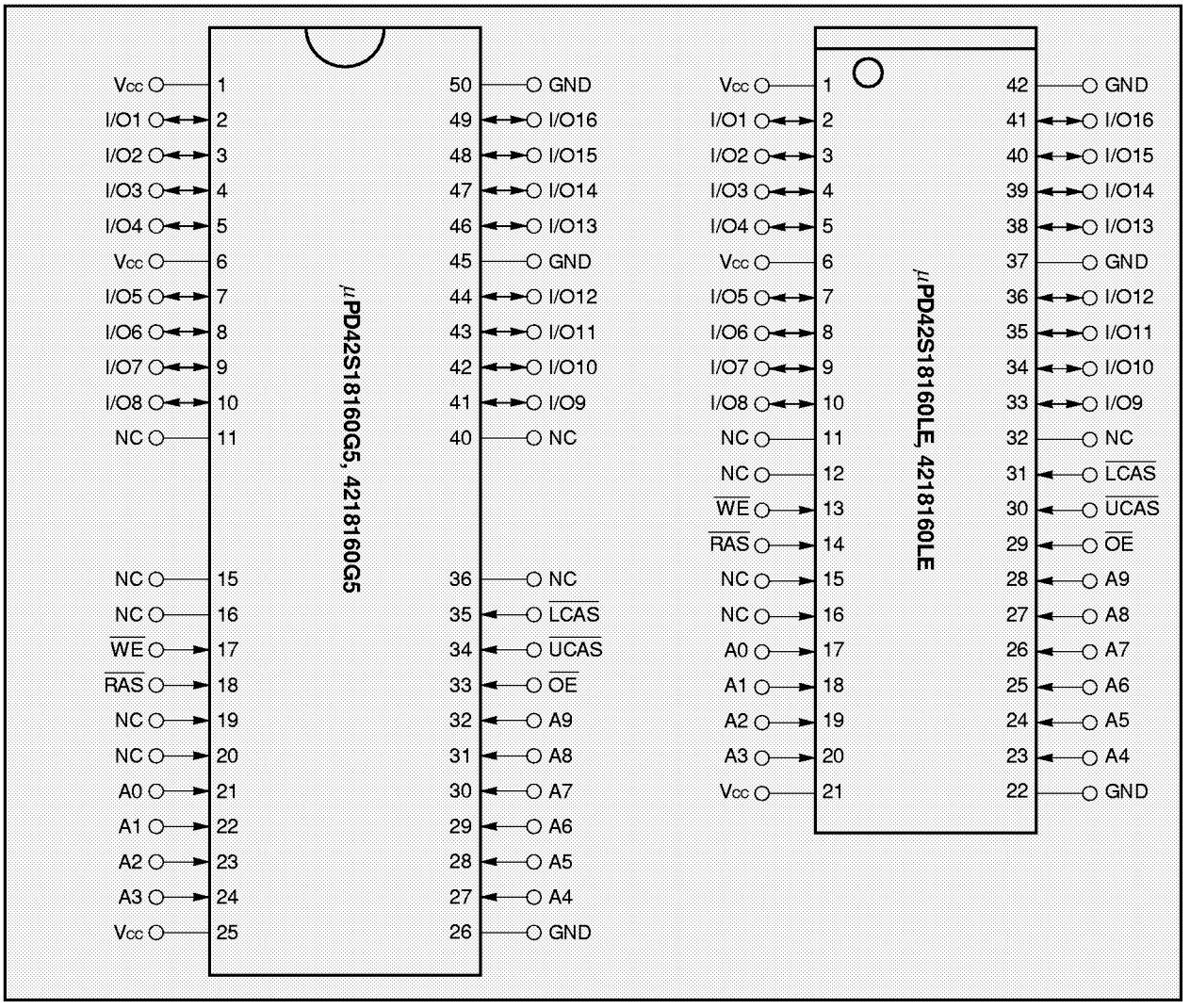
| Part number | Refresh cycle | Refresh | Power consumption at standby (MAX.) |
|---|---|---|---|
| μPD42S18160 | 1,024 cycles/128 ms | $\overline{CAS}$ before $\overline{RAS}$ self refresh,<br>$\overline{CAS}$ before $\overline{RAS}$ refresh,<br>$\overline{RAS}$ only refresh, Hidden refresh | 1.4 mW<br>(CMOS level input) |
| μPD4218160 | 1,024 cycles/16 ms | $\overline{CAS}$ before $\overline{RAS}$ refresh,<br>$\overline{RAS}$ only refresh,<br>Hidden refresh | 5.5 mW<br>(CMOS level input) |

## Ordering Information

| Part number | Access time (MAX.) | Package | Refresh |
|---|---|---|---|
| μPD42S18160G5-60 | 60 ns | 50-pin Plastic TSOP (II) (400 mil) | $\overline{CAS}$ before $\overline{RAS}$ self refresh<br>$\overline{CAS}$ before $\overline{RAS}$ refresh<br>$\overline{RAS}$ only refresh<br>Hidden refresh |
| μPD42S18160G5-70 | 70 ns | | |
| μPD42S18160LE-60 | 60 ns | 42-pin Plastic SOJ (400 mil) | |
| μPD42S18160LE-70 | 70 ns | | |
| μPD4218160G5-60 | 60 ns | 50-pin Plastic TSOP (II) (400 mil) | $\overline{CAS}$ before $\overline{RAS}$ refresh<br>$\overline{RAS}$ only refresh<br>Hidden refresh |
| μPD4218160G5-70 | 70 ns | | |
| μPD4218160LE-60 | 60 ns | 42-pin Plastic SOJ (400 mil) | |
| μPD4218160LE-70 | 70 ns | | |

## Pin Configurations (Marking Side)

50-pin Plastic TSOP (II)(400 mil)

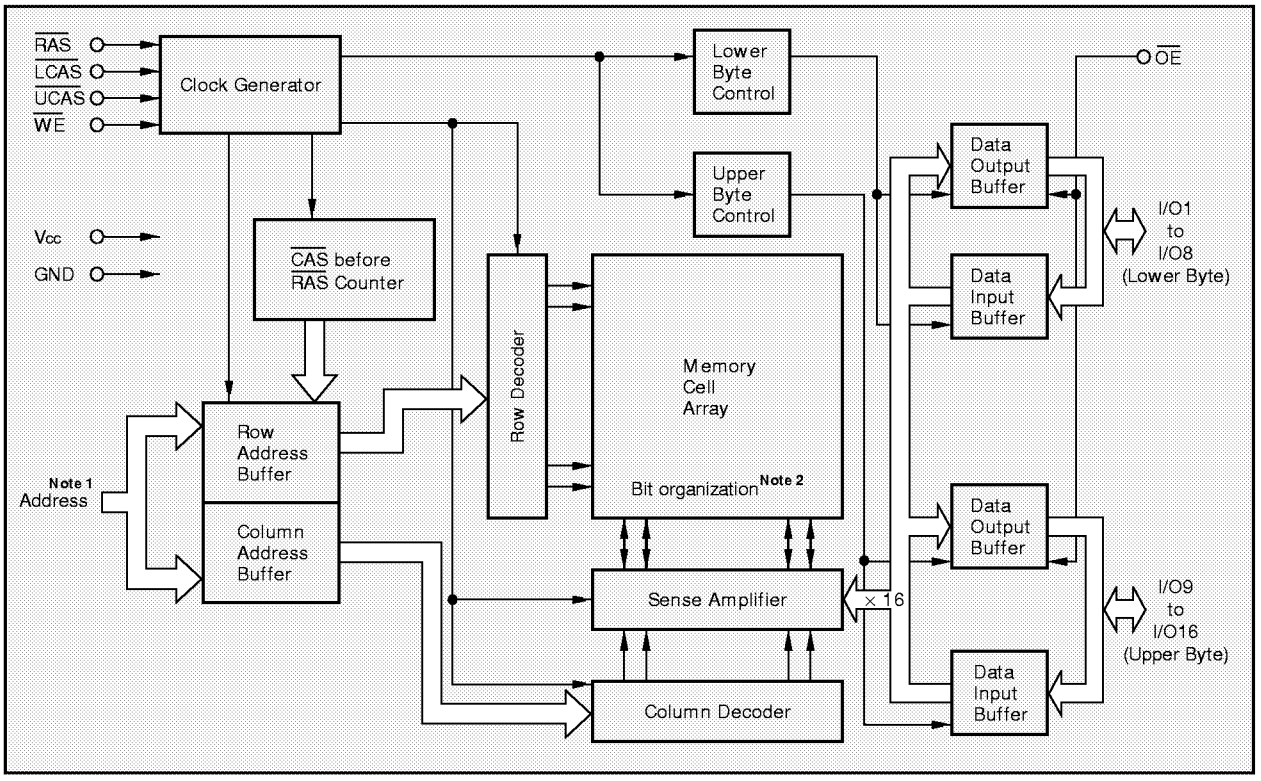



42-pin Plastic SOJ (400 mil)




A0 to A9 : Address Inputs
I/O1 to I/O16 : Data Inputs/Outputs
$\overline{RAS}$ : Row Address Strobe
$\overline{UCAS}$ : Column Address Strobe (upper)
$\overline{LCAS}$ : Column Address Strobe (lower)
$\overline{WE}$ : Write Enable
$\overline{OE}$ : Output Enable
$V_{CC}$ : Power Supply
GND : Ground
NC : No Connection

## Block Diagram




Notes 1.

| Part number | Row address | Column address |
|---|---|---|
| μPD42S18160, 4218160 | A0 - A9 | A0 - A9 |

2. μPD42S18160, 4218160 ··· 1,024 × 1,024 × 16

## Input/Output Pin Functions

The μPD42S18160, 4218160 have input pins $\overline{RAS}$, $\overline{CAS}$[Note 1], $\overline{WE}$, $\overline{OE}$, Address[Note 2] and input/output pins I/O1 to I/O16.

| Pin name | Input/ Output | Function |
|---|---|---|
| $\overline{RAS}$ (Row address strobe) | Input | $\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corre sponding word line.<br>It refreshes memory cell array of one line selected by the row address.<br>It also selects the following function.<br>• $\overline{CAS}$ before $\overline{RAS}$ refresh |
| $\overline{CAS}$ (Column address strobe) | Input | $\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier. |
| A0 to A9[Note 2] (Address input) | Input | Address bus.<br>Input total 20-bit of address signal, upper bits and lower bits[Note 2] in sequence (address multiplex method).<br>Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array.<br>In actual operation, latch row address by specifying row address and activating $\overline{RAS}$.<br>Then, switch the address bus to column address and activate $\overline{CAS}$.<br>Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated.<br>Therefore, the address input setup time ($t_{ASR}$, $t_{ASC}$) and hold time ($t_{RAH}$, $t_{CAH}$) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$. |
| $\overline{WE}$ (Write enable) | Input | Write control signal.<br>Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. |
| $\overline{OE}$ (Output enable) | Input | Read control signal.<br>Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$.<br>If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device.<br>Therefore, read operation cannot be executed. |
| I/O1 to I/O16 (Data input/ output) | Input/ Output | 16-bit data bus.<br>I/O1 to I/O16 are used to input/output data. |

**Notes 1.** $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

2.

| Part number | Address inputs | Upper bits | Lower bits |
|---|---|---|---|
| μPD42S18160, 4218160 | A0 - A9 | 10 bits | 10 bits |

# Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to GND | $V_T$ | | –1.0 to +7.0 | V |
| Supply voltage | $V_{CC}$ | | –1.0 to +7.0 | V |
| Output current | $I_O$ | | 50 | mA |
| Power dissipation | $P_D$ | | 1 | W |
| Operating ambient temperature | $T_A$ | | 0 to +70 | °C |
| Storage temperature | $T_{stg}$ | | –55 to +125 | °C |

**Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended Operating Conditions

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| High level input voltage | $V_{IH}$ | | 2.4 | | $V_{CC}$ +1.0 | V |
| Low level input voltage | $V_{IL}$ | | –1.0 | | +0.8 | V |
| Operating ambient temperature | $T_A$ | | 0 | | 70 | °C |

### Capacitance ($T_A$ = 25 °C, f = 1 MHz)

| Parameter | Symbol | Test Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{I1}$ | Address | | | 5 | pF |
| | $C_{I2}$ | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | | | 7 | pF |
| Data Input/Output capacitance | $C_{I/O}$ | I/O | | | 7 | pF |

## DC Characteristics (Recommended Operating Conditions unless otherwise noted)

| Parameter | | Symbol | Test Condition | | MIN. | MAX. | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Operating current | | $I_{CC1}$ | $\overline{RAS}$, $\overline{CAS}$ Cycling<br>$t_{RC} = t_{RC\ (MIN.)}$<br>$I_O$ = 0 mA | $t_{RAC}$ = 60 ns | | 160 | mA | 1, 2, 3 |
| | | | | $t_{RAC}$ = 70 ns | | 150 | | |
| Standby current | μPD42S18160 | $I_{CC2}$ | $\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, $I_O$ = 0 mA | | | 2.0 | mA | |
| | | | $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_O$ = 0 mA | | | 0.25 | | |
| | μPD4218160 | | $\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, $I_O$ = 0 mA | | | 2.0 | | |
| | | | $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V, $I_O$ = 0 mA | | | 1.0 | | |
| $\overline{RAS}$ only refresh current | | $I_{CC3}$ | $\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$<br>$t_{RC} = t_{RC\ (MIN.)}$, $I_O$ = 0 mA | $t_{RAC}$ = 60 ns | | 160 | mA | 1, 2, 3, 4 |
| | | | | $t_{RAC}$ = 70 ns | | 150 | | |
| Operating current (Fast page mode) | | $I_{CC4}$ | $\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ Cycling<br>$t_{PC} = t_{PC\ (MIN.)}$, $I_O$ = 0 mA | $t_{RAC}$ = 60 ns | | 90 | mA | 1, 2, 5 |
| | | | | $t_{RAC}$ = 70 ns | | 80 | | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh current | | $I_{CC5}$ | $\overline{RAS}$ Cycling<br>$t_{RC} = t_{RC\ (MIN.)}$<br>$I_O$ = 0 mA | $t_{RAC}$ = 60 ns | | 160 | mA | 1, 2 |
| | | | | $t_{RAC}$ = 70 ns | | 150 | | |
| $\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S18160) | | $I_{CC6}$ | $\overline{CAS}$ before $\overline{RAS}$ refresh:<br>$t_{RC}$ = 125.0 μs<br>$\overline{RAS}$, $\overline{CAS}$:<br>$V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$<br>0 V ≤ $V_{IL} \leq$ 0.2 V | $t_{RAS} \leq$ 300 ns | | 350 | μA | 1, 2 |
| | | | Standby:<br>$\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2$ V<br>Address: $V_{IH}$ or $V_{IL}$<br>$\overline{WE}$, $\overline{OE}$: $V_{IH}$<br>$I_O$ = 0 mA | $t_{RAS} \leq$ 1 μs | | 400 | μA | 1, 2 |
| Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for the μPD42S18160) | | $I_{CC7}$ | $\overline{RAS}$, $\overline{CAS}$:<br>$t_{RASS}$ = 5 ms<br>$V_{CC} - 0.2$ V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$<br>0 V ≤ $V_{IL} \leq$ 0.2 V<br>$I_O$ = 0 mA | | | 250 | μA | 2 |
| Input leakage current | | $I_{I\ (L)}$ | $V_I$ = 0 to 5.5 V<br>All other pins not under test = 0 V | | –10 | +10 | μA | |
| Output leakage current | | $I_{O\ (L)}$ | $V_O$ = 0 to 5.5 V<br>Output is disabled (Hi-Z) | | –10 | +10 | μA | |
| High level output voltage | | $V_{OH}$ | $I_O$ = –2.5 mA | | 2.4 | | V | |
| Low level output voltage | | $V_{OL}$ | $I_O$ = +2.1 mA | | | 0.4 | V | |

**Notes 1.** $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC5}$ and $I_{CC6}$ depend on cycle rates ($t_{RC}$ and $t_{PC}$).

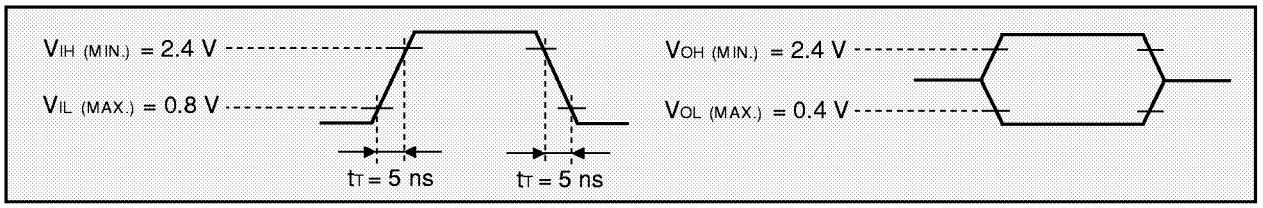
2. Specified values are obtained with outputs unloaded.
3. $I_{CC1}$ and $I_{CC3}$ are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
4. $I_{CC3}$ is measured assuming that all column address inputs are held at either high or low.
5. $I_{CC4}$ is measured assuming that all column address inputs are switched only once during each fast page cycle.

# AC Characteristics (Recommended Operating Conditions unless otherwise noted)

## AC Characteristics Test Conditions

(1) Input timing specification

(2) Output timing specification




(3) Loading conditions are 100 pF + 1 TTL.

## Common to Read, Write, Read Modify Write Cycle

| Parameter | | Symbol | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | | |
| Read / Write Cycle Time | | $t_{RC}$ | 110 | – | 130 | – | ns | |
| $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 40 | – | 50 | – | ns | |
| $\overline{CAS}$ Precharge Time | | $t_{CPN}$ | 10 | – | 10 | – | ns | |
| $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 60 | 10,000 | 70 | 10,000 | ns | |
| $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 15 | 10,000 | 20 | 10,000 | ns | |
| $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 15 | – | 18 | – | ns | |
| $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 60 | – | 70 | – | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | | $t_{RCD}$ | 20 | 45 | 20 | 50 | ns | 1 |
| $\overline{RAS}$ to Column Address Delay Time | | $t_{RAD}$ | 15 | 30 | 15 | 35 | ns | 1 |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | | $t_{CRP}$ | 5 | – | 5 | – | ns | 2 |
| Row Address Setup Time | | $t_{ASR}$ | 0 | – | 0 | – | ns | |
| Row Address Hold Time | | $t_{RAH}$ | 10 | – | 10 | – | ns | |
| Column Address Setup Time | | $t_{ASC}$ | 0 | – | 0 | – | ns | |
| Column Address Hold Time | | $t_{CAH}$ | 15 | – | 15 | – | ns | |
| $\overline{OE}$ Lead Time Referenced to $\overline{RAS}$ | | $t_{OES}$ | 0 | – | 0 | – | ns | |
| $\overline{CAS}$ to Data Setup Time | | $t_{CLZ}$ | 0 | – | 0 | – | ns | |
| $\overline{OE}$ to Data Setup Time | | $t_{OLZ}$ | 0 | – | 0 | – | ns | |
| $\overline{OE}$ to Data Delay Time | | $t_{OED}$ | 13 | – | 15 | – | ns | |
| Masked Byte Write Hold Time Referenced to $\overline{RAS}$ | | $t_{MRH}$ | 0 | – | 0 | – | ns | |
| Transition Time (Rise and Fall) | | $t_T$ | 3 | 50 | 3 | 50 | ns | |
| Refresh Time | μPD42S18160 | $t_{REF}$ | – | 128 | – | 128 | ms | 3 |
| | μPD4218160 | | – | 16 | – | 16 | ms | |

**Notes 1.** For read cycles, access time is defined as follows:

| Input Conditions | Access Time | Access Time from $\overline{RAS}$ |
|---|---|---|
| $t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$ | $t_{RAC\ (MAX.)}$ | $t_{RAC\ (MAX.)}$ |
| $t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$ | $t_{AA\ (MAX.)}$ | $t_{RAD} + t_{AA\ (MAX.)}$ |
| $t_{RCD} > t_{RCD\ (MAX.)}$ | $t_{CAC\ (MAX.)}$ | $t_{RCD} + t_{CAC\ (MAX.)}$ |

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time ($t_{RAC}$, $t_{AA}$ or $t_{CAC}$) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. $t_{CRP\ (MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.

## Read Cycle

| Parameter | Symbol | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | – | 60 | – | 70 | ns | 1 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | – | 15 | – | 20 | ns | 1 |
| Access Time from Column Address | $t_{AA}$ | – | 30 | – | 35 | ns | 1 |
| Access Time from $\overline{OE}$ | $t_{OEA}$ | – | 15 | – | 20 | ns | |
| Column Address Lead Time Referenced to $\overline{RAS}$ | $t_{RAL}$ | 30 | – | 35 | – | ns | |
| Read Command Setup Time | $t_{RCS}$ | 0 | – | 0 | – | ns | |
| Read Command Hold Time Referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | – | 0 | – | ns | 2 |
| Read Command Hold Time Referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | – | 0 | – | ns | 2 |
| Output Buffer Turn-off Delay Time from $\overline{OE}$ | $t_{OEZ}$ | 0 | 13 | 0 | 15 | ns | 3 |
| Output Buffer Turn-off Delay Time from $\overline{CAS}$ | $t_{OFF}$ | 0 | 13 | 0 | 15 | ns | 3 |

**Notes 1.** For read cycles, access time is defined as follows:

| Input Conditions | Access Time | Access Time from $\overline{RAS}$ |
|---|---|---|
| $t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$ | $t_{RAC\ (MAX.)}$ | $t_{RAC\ (MAX.)}$ |
| $t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$ | $t_{AA\ (MAX.)}$ | $t_{RAD} + t_{AA\ (MAX.)}$ |
| $t_{RCD} > t_{RCD\ (MAX.)}$ | $t_{CAC\ (MAX.)}$ | $t_{RCD} + t_{CAC\ (MAX.)}$ |

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ($t_{RAC}$, $t_{AA}$ or $t_{CAC}$) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OFF\ (MAX.)}$ and $t_{OEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to $V_{OH}$ or $V_{OL}$.

### Write Cycle

| Parameter | Symbol | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| $\overline{WE}$ Hold Time Referenced to $\overline{CAS}$ | $t_{WCH}$ | 10 | – | 10 | – | ns | 1 |
| $\overline{WE}$ Pulse Width | $t_{WP}$ | 10 | – | 10 | – | ns | 1 |
| $\overline{WE}$ Lead Time Referenced to $\overline{RAS}$ | $t_{RWL}$ | 20 | – | 20 | – | ns | |
| $\overline{WE}$ Lead Time Referenced to $\overline{CAS}$ | $t_{CWL}$ | 15 | – | 15 | – | ns | |
| $\overline{WE}$ Setup Time | $t_{WCS}$ | 0 | – | 0 | – | ns | 2 |
| $\overline{OE}$ Hold Time | $t_{OEH}$ | 0 | – | 0 | – | ns | |
| Data-in Setup Time | $t_{DS}$ | 0 | – | 0 | – | ns | 3 |
| Data-in Hold Time | $t_{DH}$ | 10 | – | 15 | – | ns | 3 |

**Notes 1.** $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
3. $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

### Read Modify Write Cycle

| Parameter | Symbol | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| Read Modify Write Cycle Time | $t_{RWC}$ | 160 | – | 180 | – | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 83 | – | 95 | – | ns | 1 |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 38 | – | 40 | – | ns | 1 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 53 | – | 60 | – | ns | 1 |

**Note 1.** If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

### Fast Page Mode

| Parameter | Symbol | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| Fast Page Mode Cycle Time | $t_{PC}$ | 40 | – | 45 | – | ns | |
| Access Time from $\overline{CAS}$ Precharge | $t_{ACP}$ | – | 35 | – | 40 | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RASP}$ | 60 | 125,000 | 70 | 125,000 | ns | |
| $\overline{CAS}$ Precharge Time | $t_{CP}$ | 10 | – | 10 | – | ns | |
| $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | $t_{RHCP}$ | 35 | – | 40 | – | ns | |
| Read Modify Write Cycle Time | $t_{PRWC}$ | 85 | – | 90 | – | ns | |
| $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | $t_{CPWD}$ | 60 | – | 65 | – | ns | 1 |

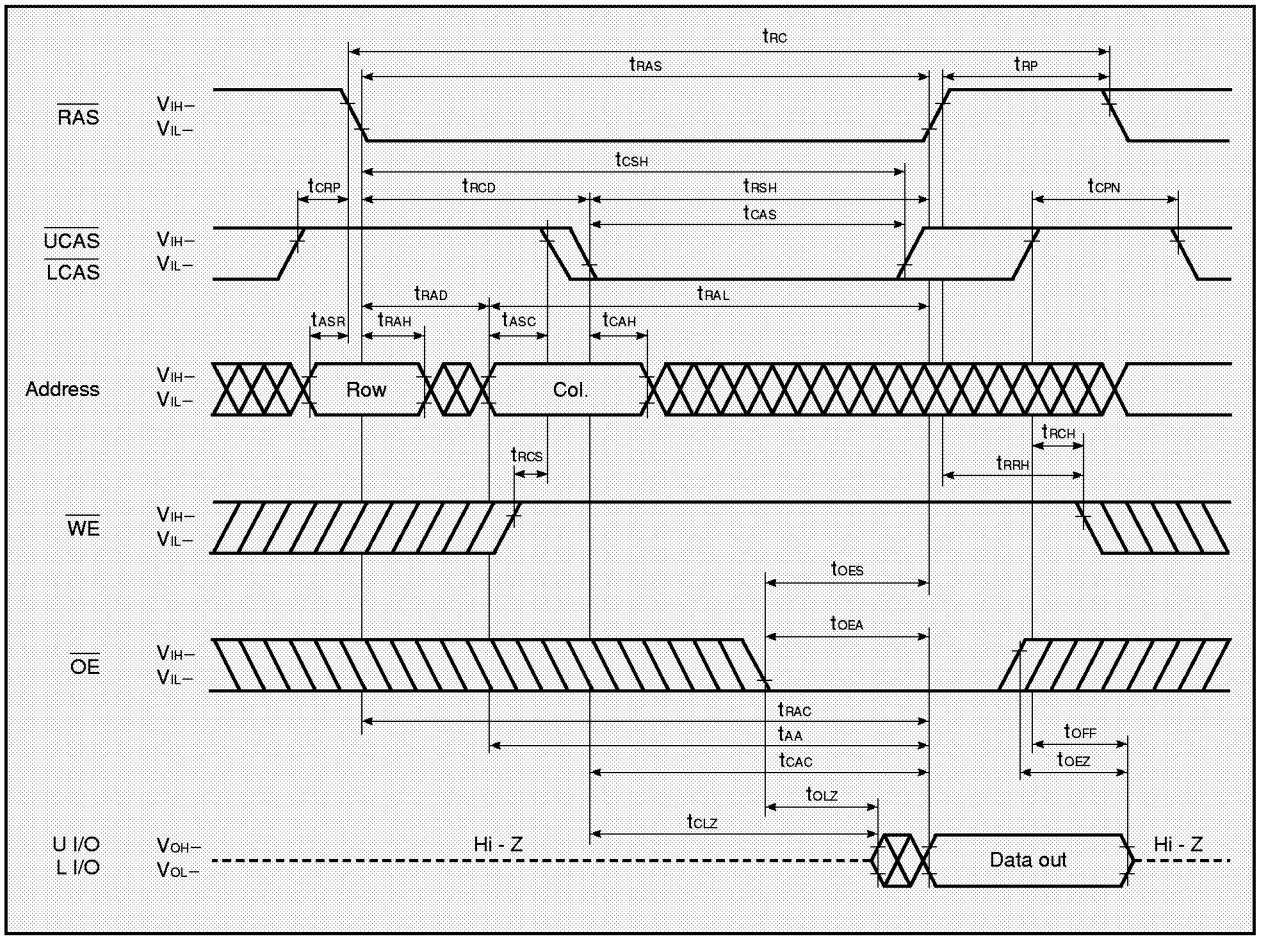
**Note 1.** If $t_{WCS} \geq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\,(MIN.)}$, $t_{CWD} \geq t_{CWD\,(MIN.)}$, $t_{AWD} \geq t_{AWD\,(MIN.)}$ and $t_{CPWD} \geq t_{CPWD\,(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

### Refresh Cycle

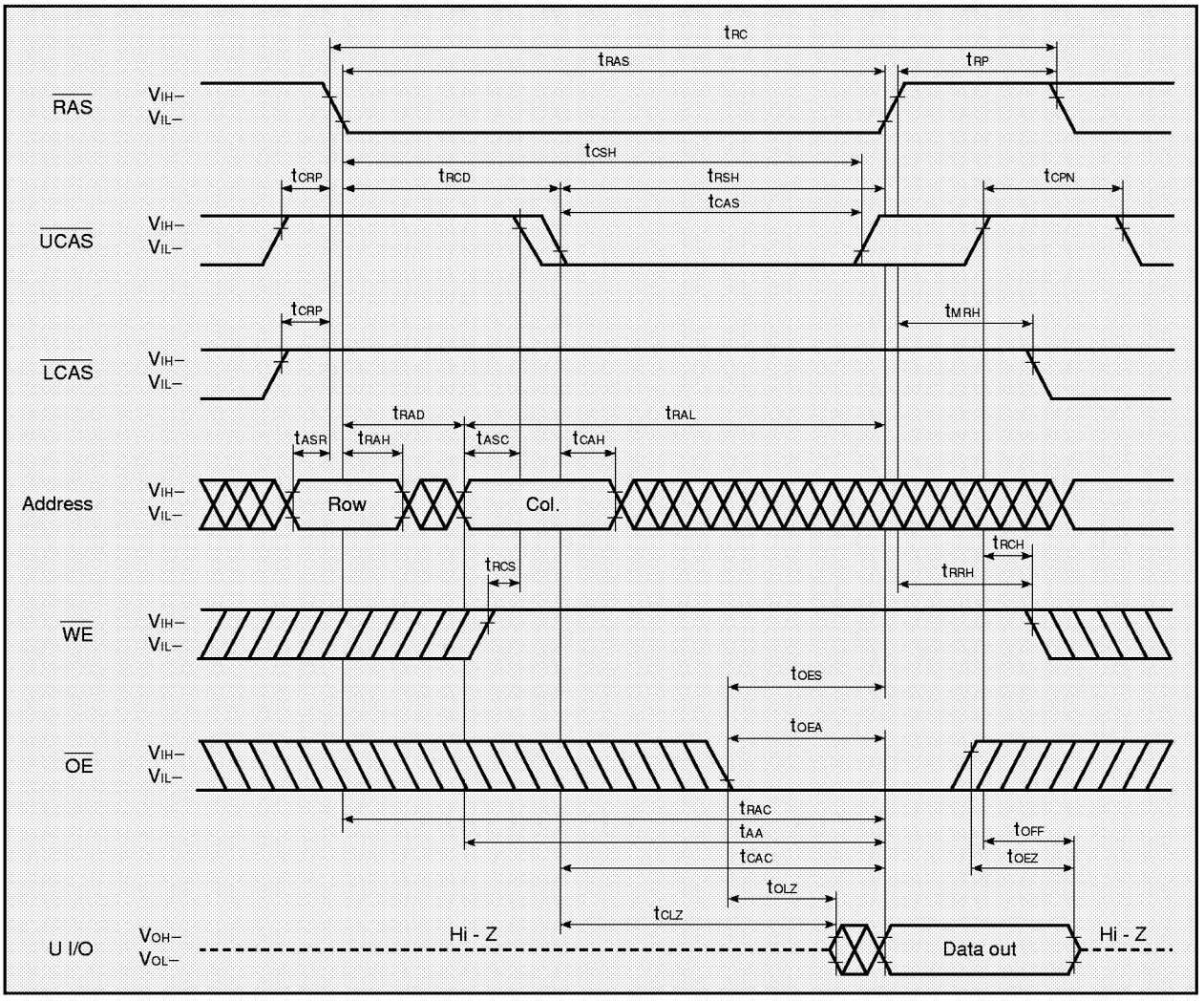
| Parameter | Symbol | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | | |
| $\overline{CAS}$ Setup Time | $t_{CSR}$ | 5 | – | 5 | – | ns | |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh) | $t_{CHR}$ | 10 | – | 10 | – | ns | |
| $\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time | $t_{RPC}$ | 5 | – | 5 | – | ns | |
| $\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh) | $t_{RASS}$ | 100 | – | 100 | – | μs | 1 |
| $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh) | $t_{RPS}$ | 110 | – | 130 | – | ns | 1 |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh) | $t_{CHS}$ | –50 | – | –50 | – | ns | 1 |
| $\overline{WE}$ Hold Time | $t_{WHR}$ | 15 | – | 15 | – | ns | |

**Note 1.** This specification is applied only to the μPD42S18160.

## Read Cycle

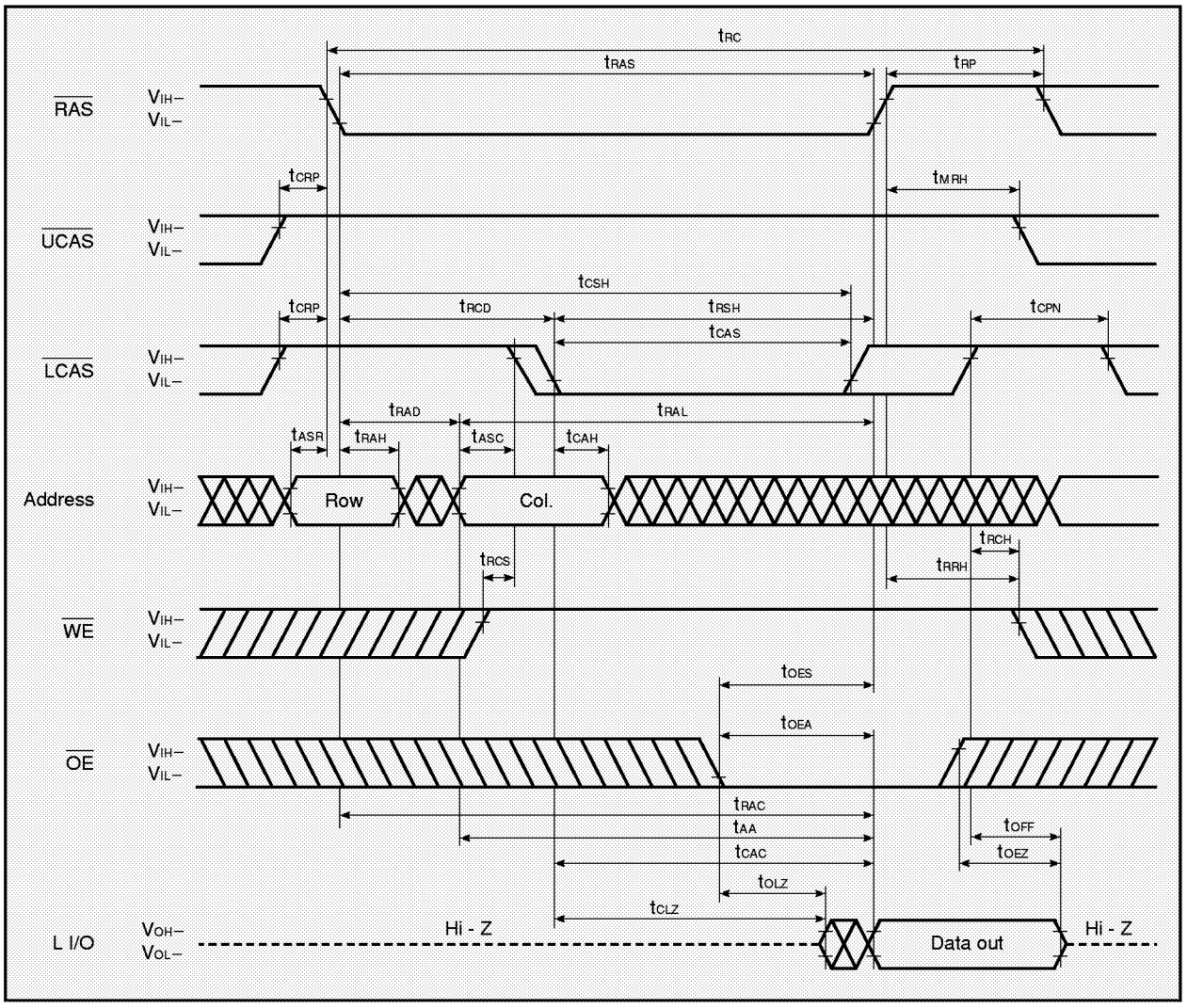

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS
LCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCH
tRCS
tRRH
WE
tOES
tOEA
OE
tRAC
tAA
tCAC
tOFF
tOEZ
tOLZ
tCLZ
U I/O
L I/O
VOH–
VOL–
Hi - Z
Data out
Hi - Z

### Upper Byte Read Cycle



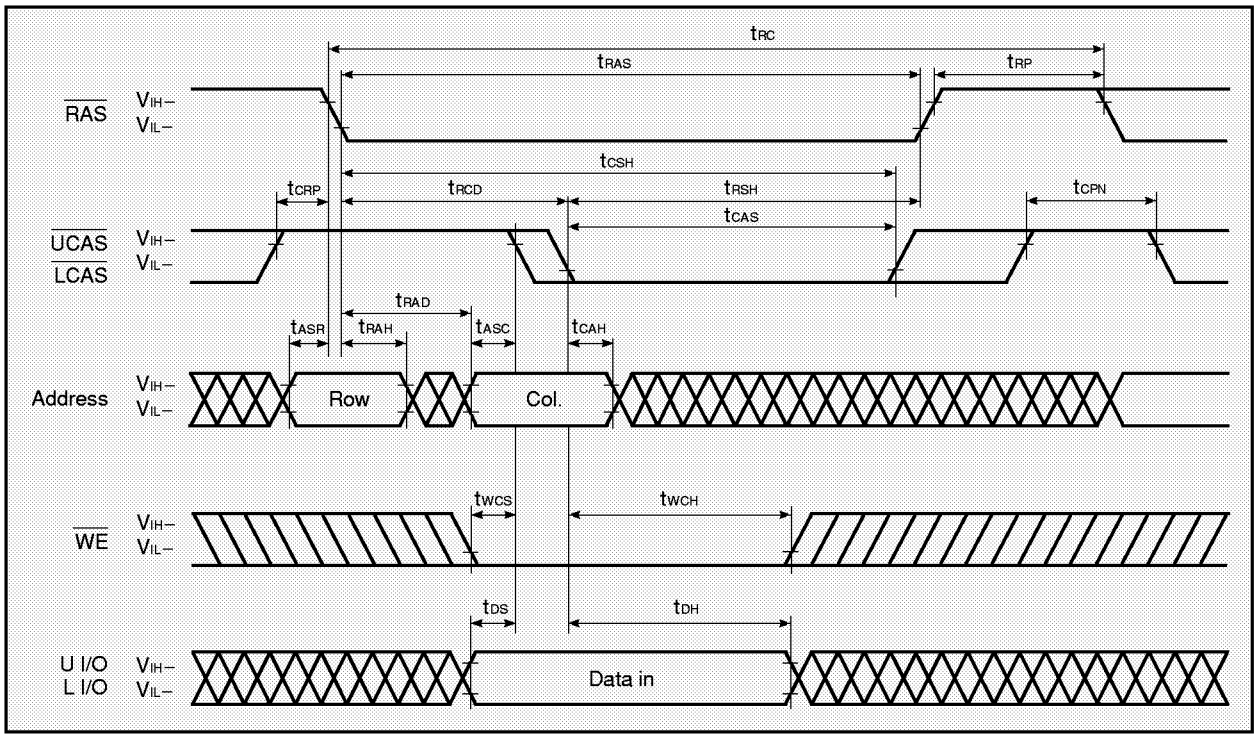

**Remark** L I/O: Hi-Z

### Lower Byte Read Cycle



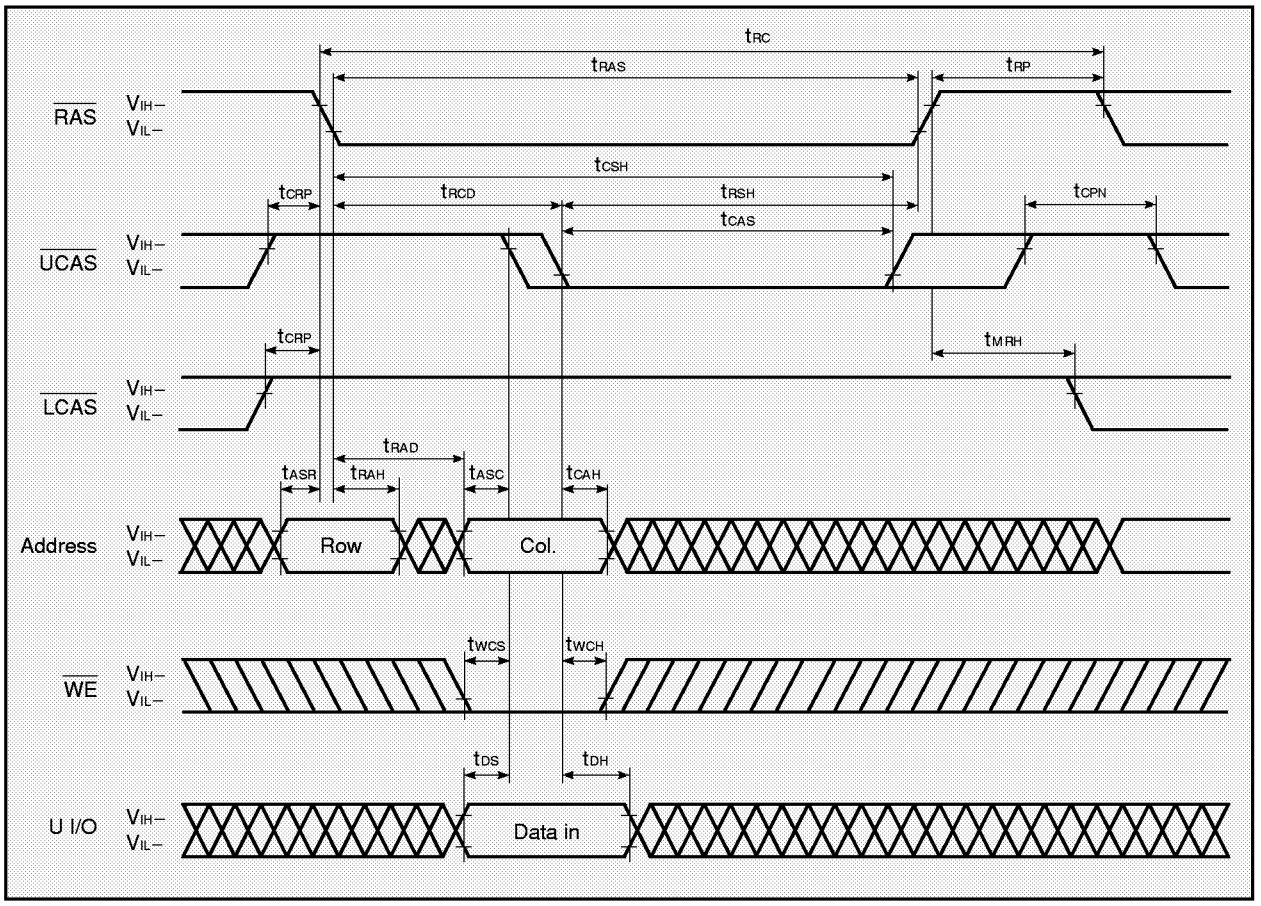

**Remark** U I/O: Hi-Z

Early Write Cycle



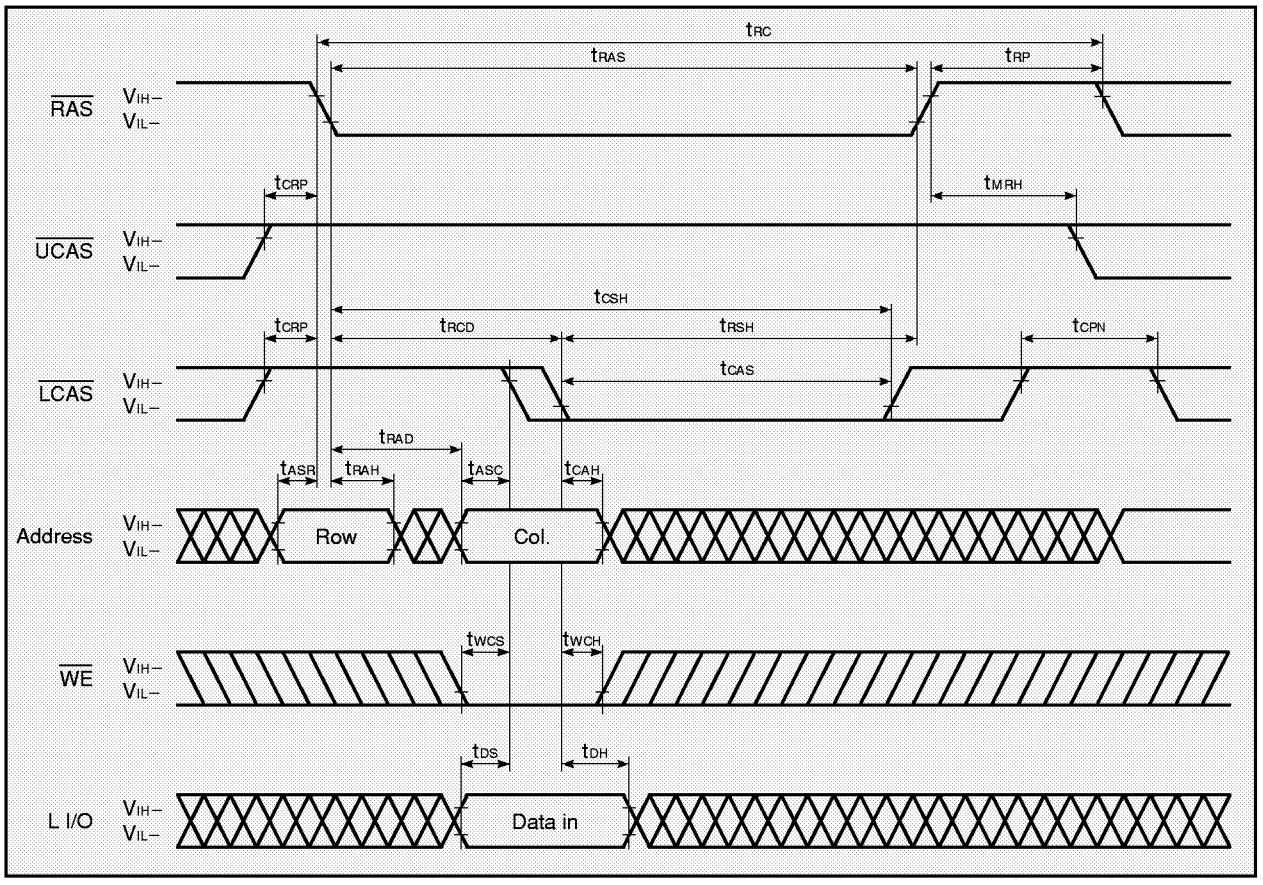

Remark $\overline{OE}$: Don't care

### Upper Byte Early Write Cycle



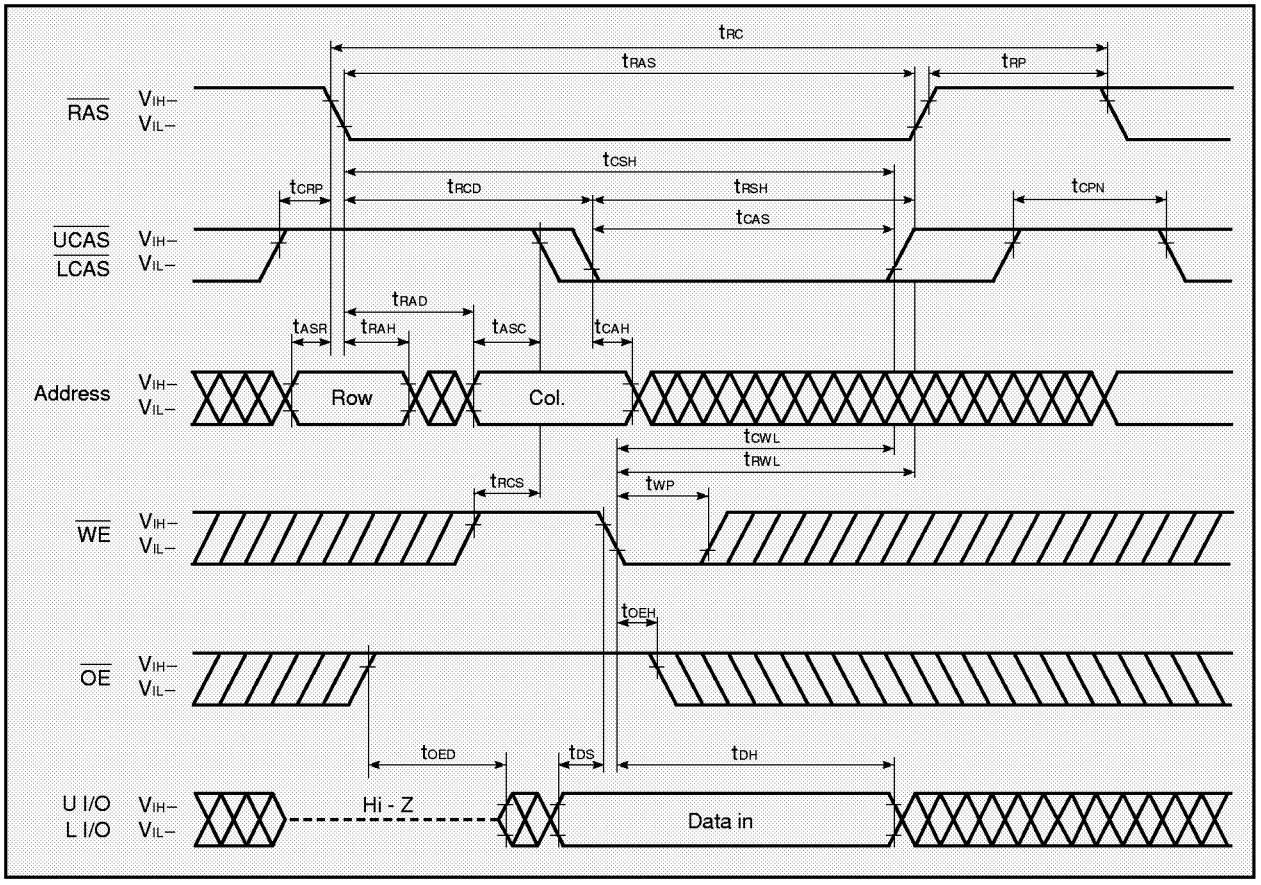

Remark $\overline{OE}$, L I/O: Don't care

## Lower Byte Early Write Cycle

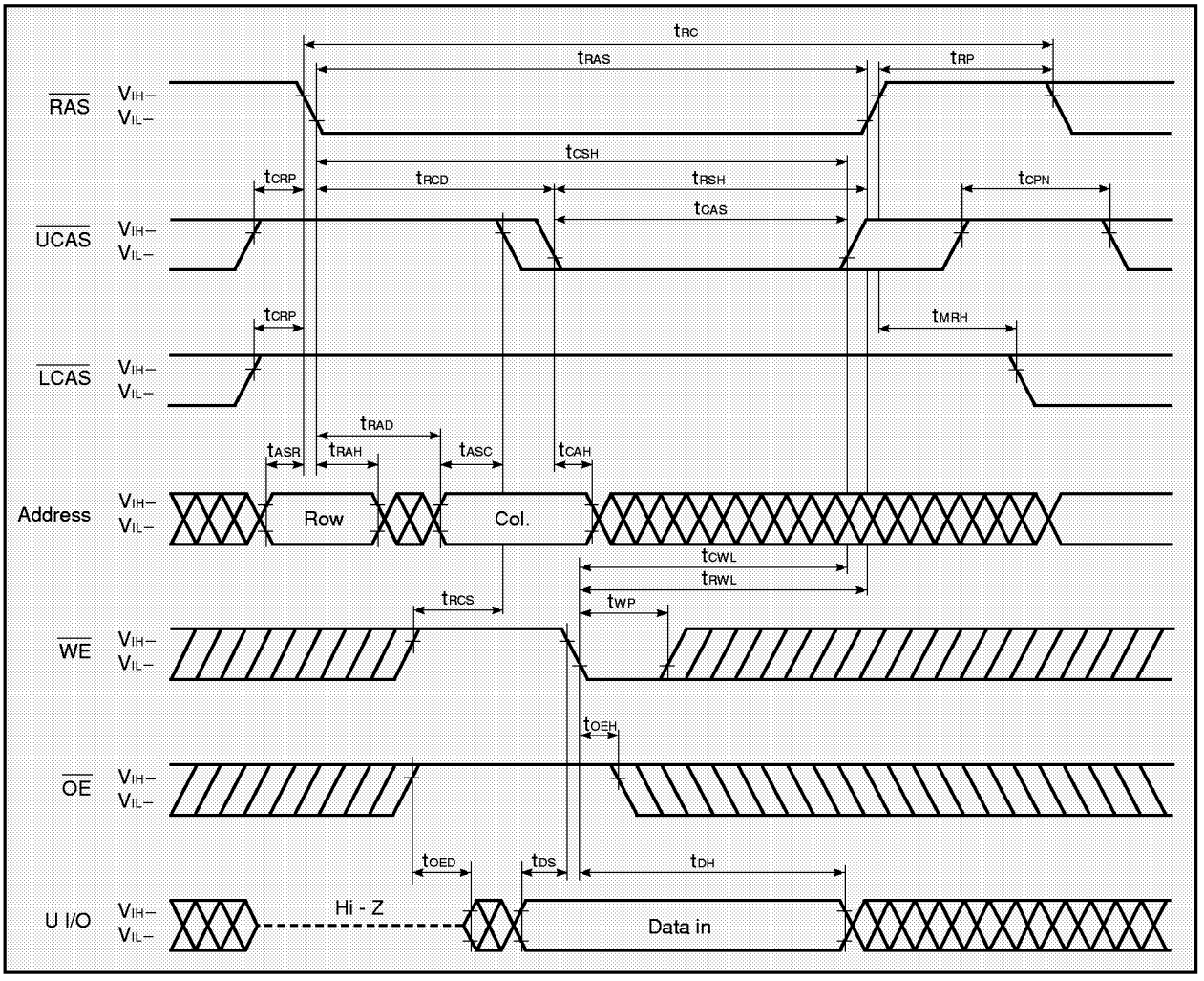



Remark $\overline{OE}$, U I/O: Don't care

Late Write Cycle

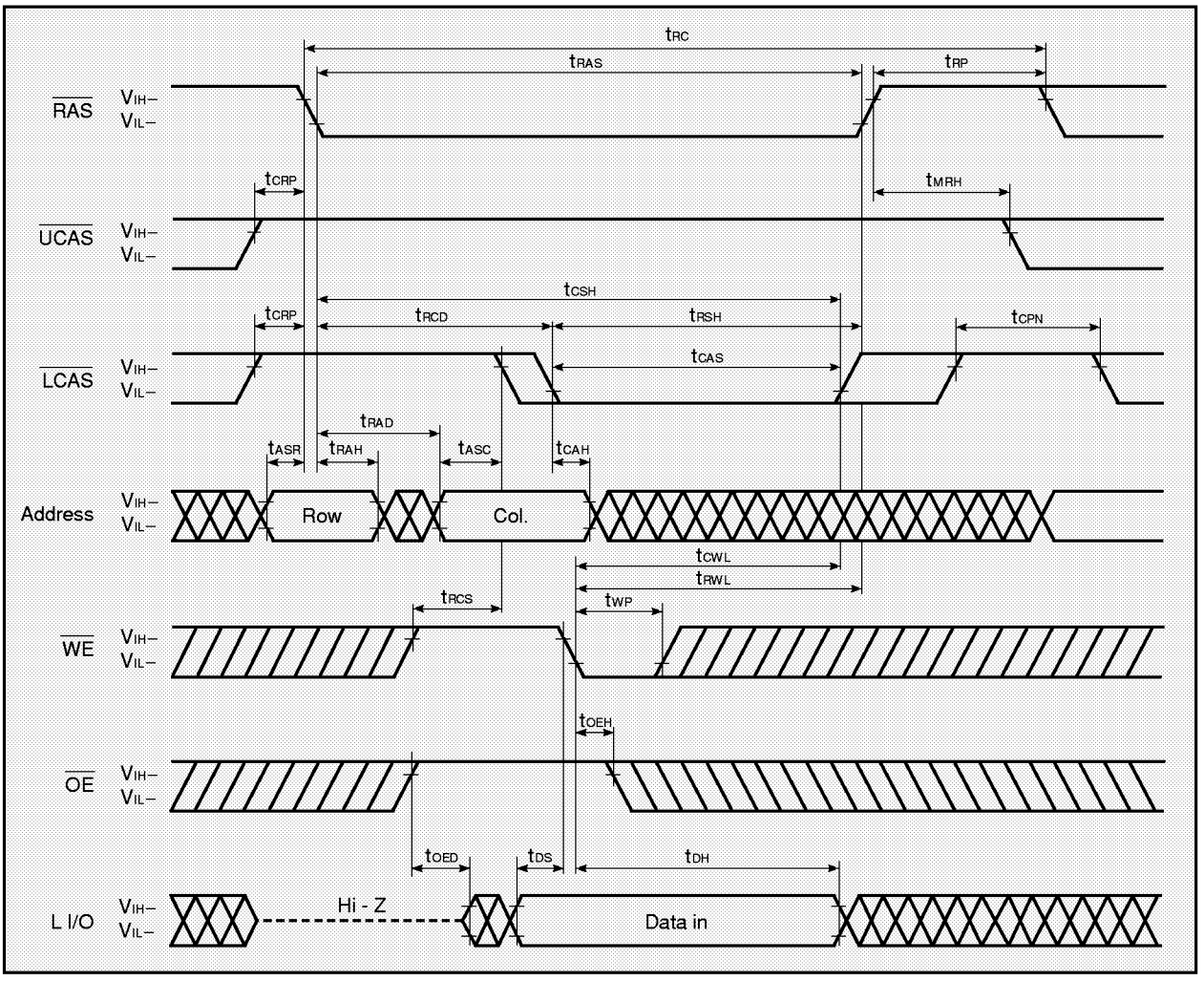


### Upper Byte Late Write Cycle



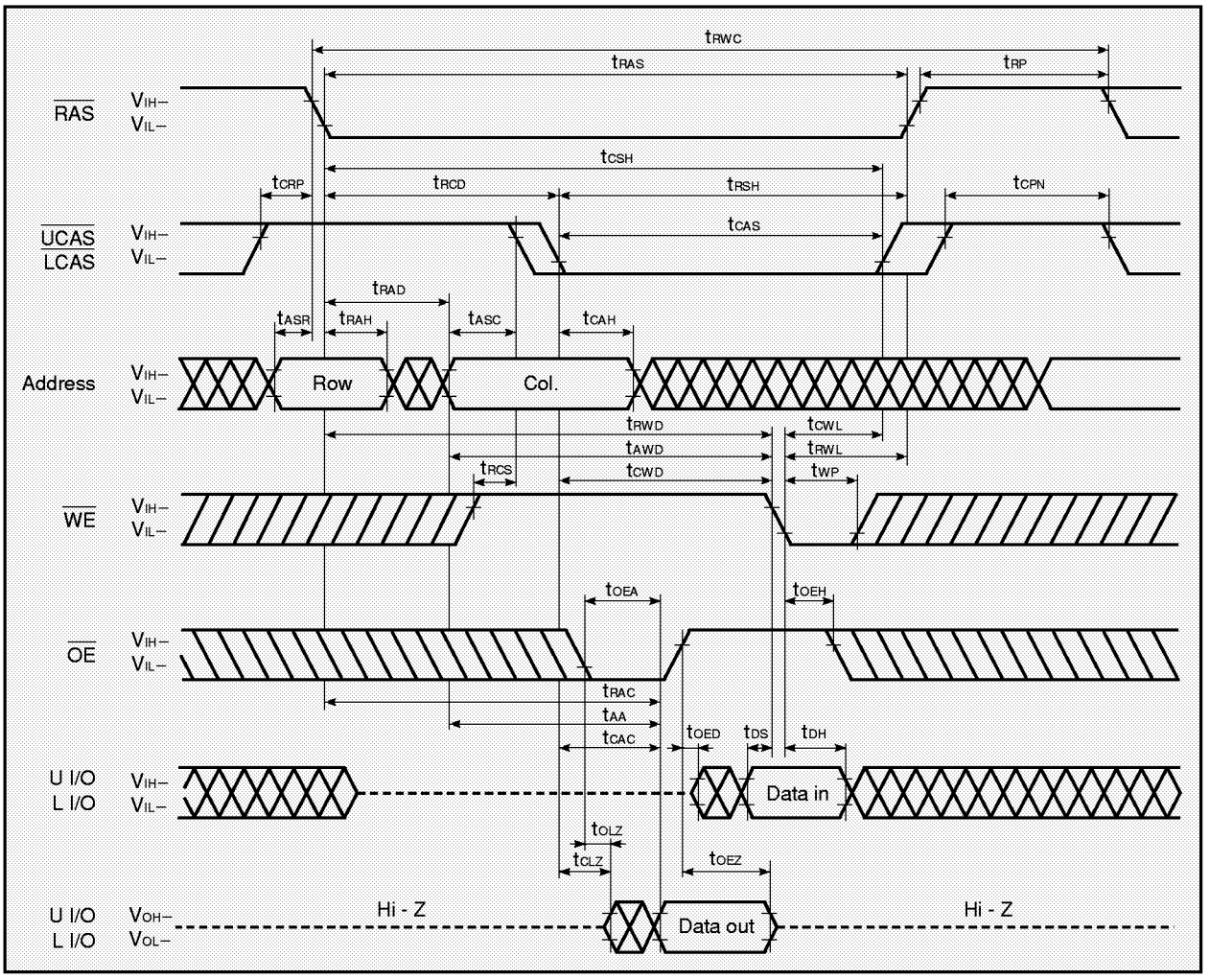

**Remark** L I/O: Don't care

### Lower Byte Late Write Cycle

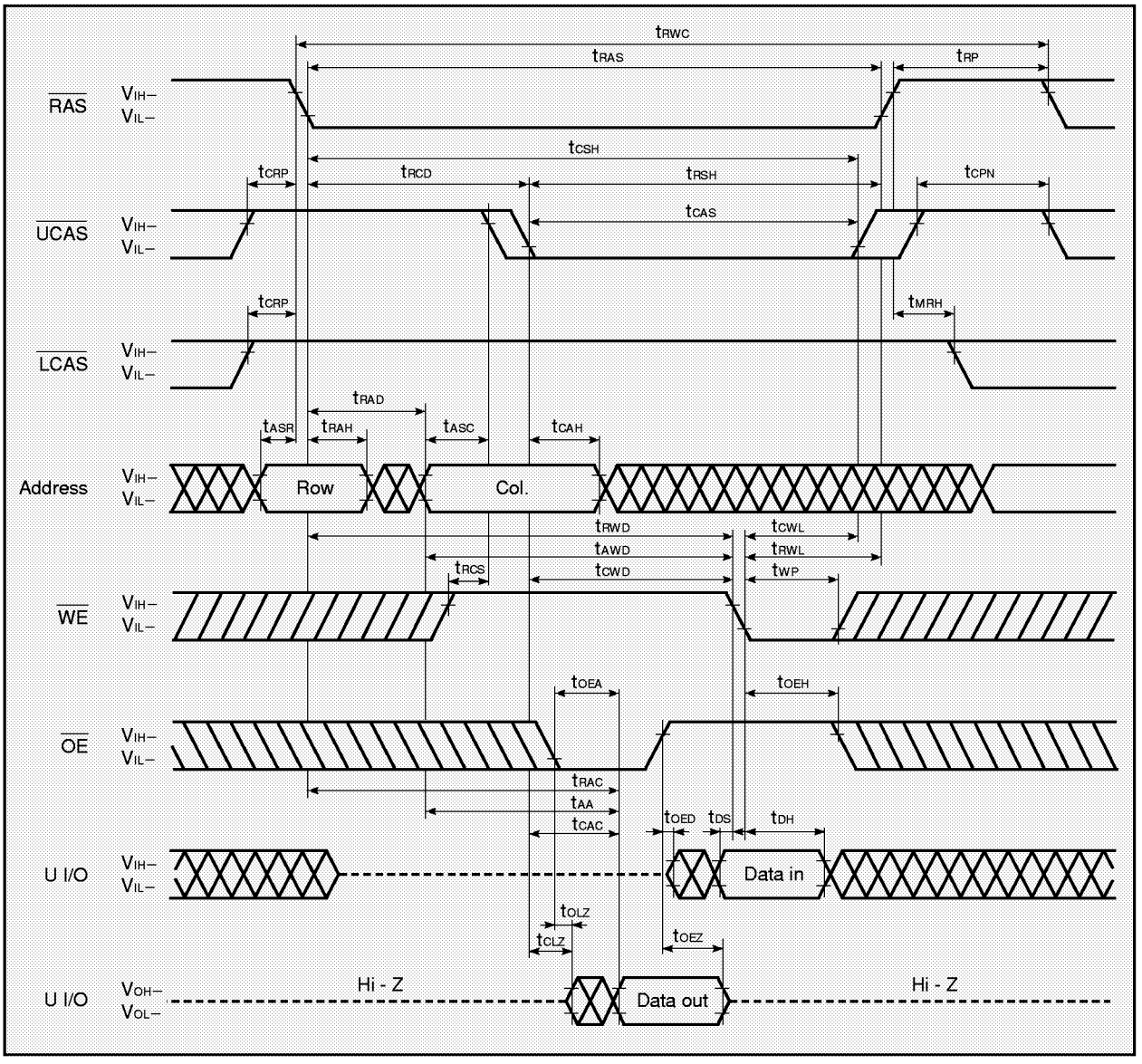



**Remark** U I/O: Don't care

## Read Modify Write Cycle

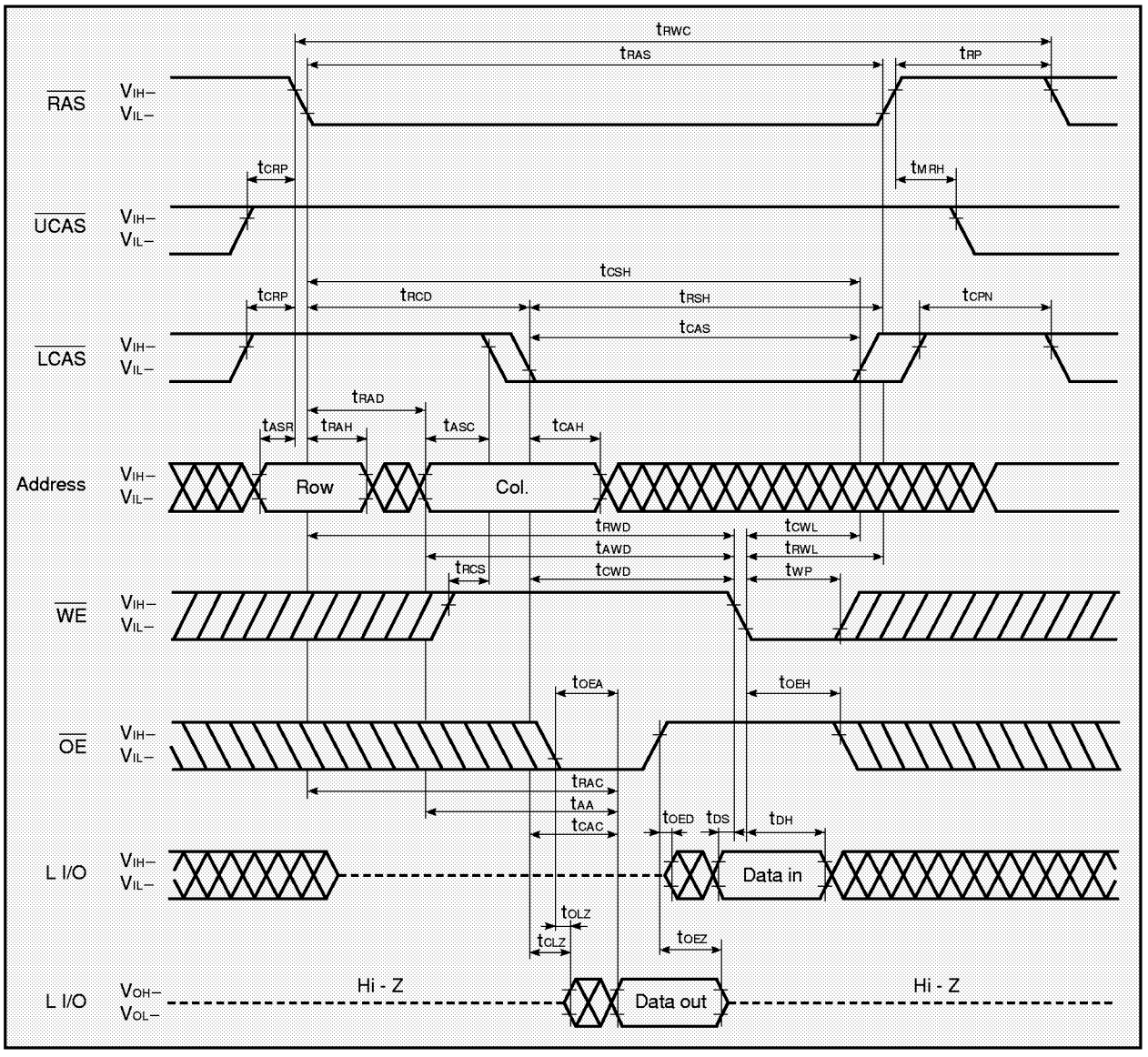


### Upper Byte Read Modify Write Cycle



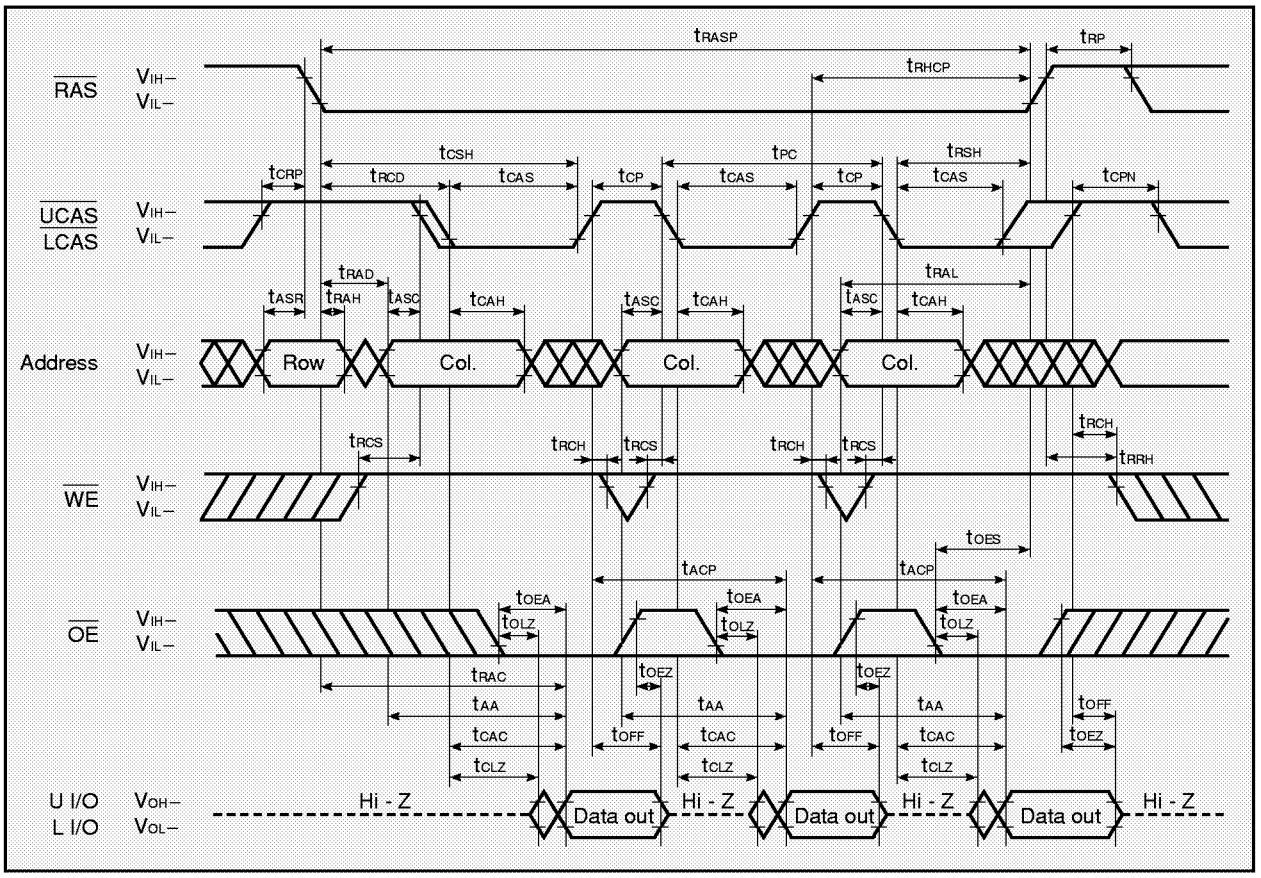

**Remark** In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

### Lower Byte Read Modify Write Cycle



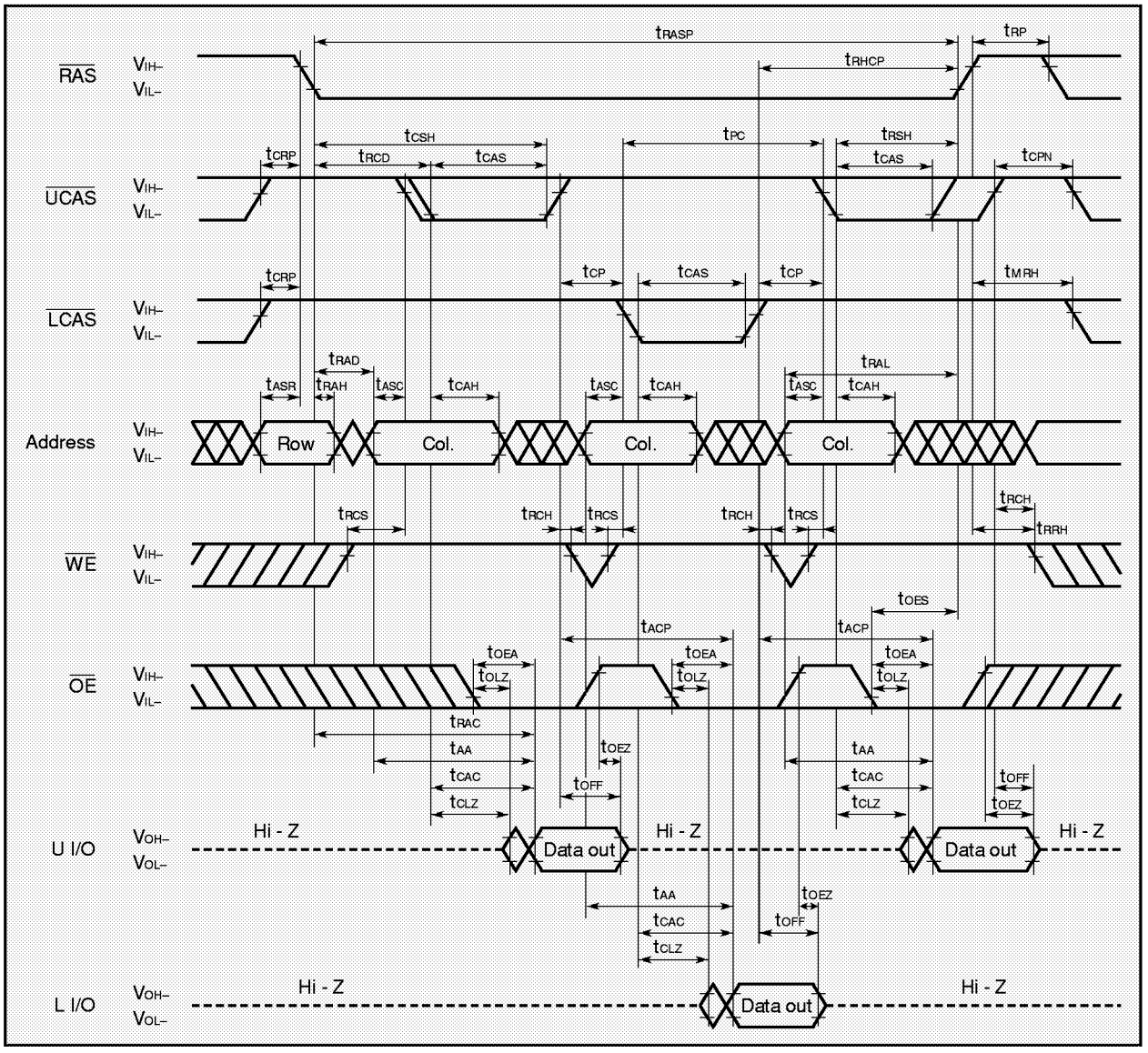

**Remark** In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

## Fast Page Mode Read Cycle




**Remark** In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

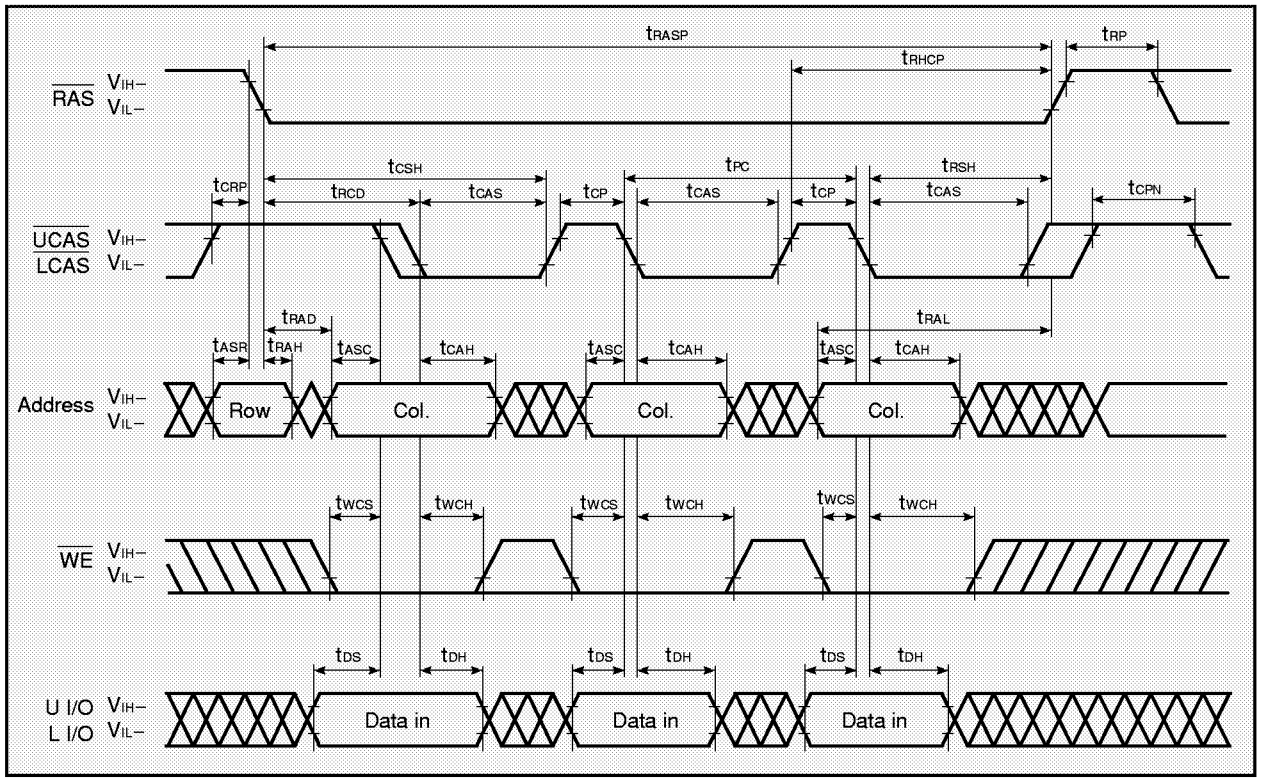
## Fast Page Mode Byte Read Cycle




**Remarks** 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

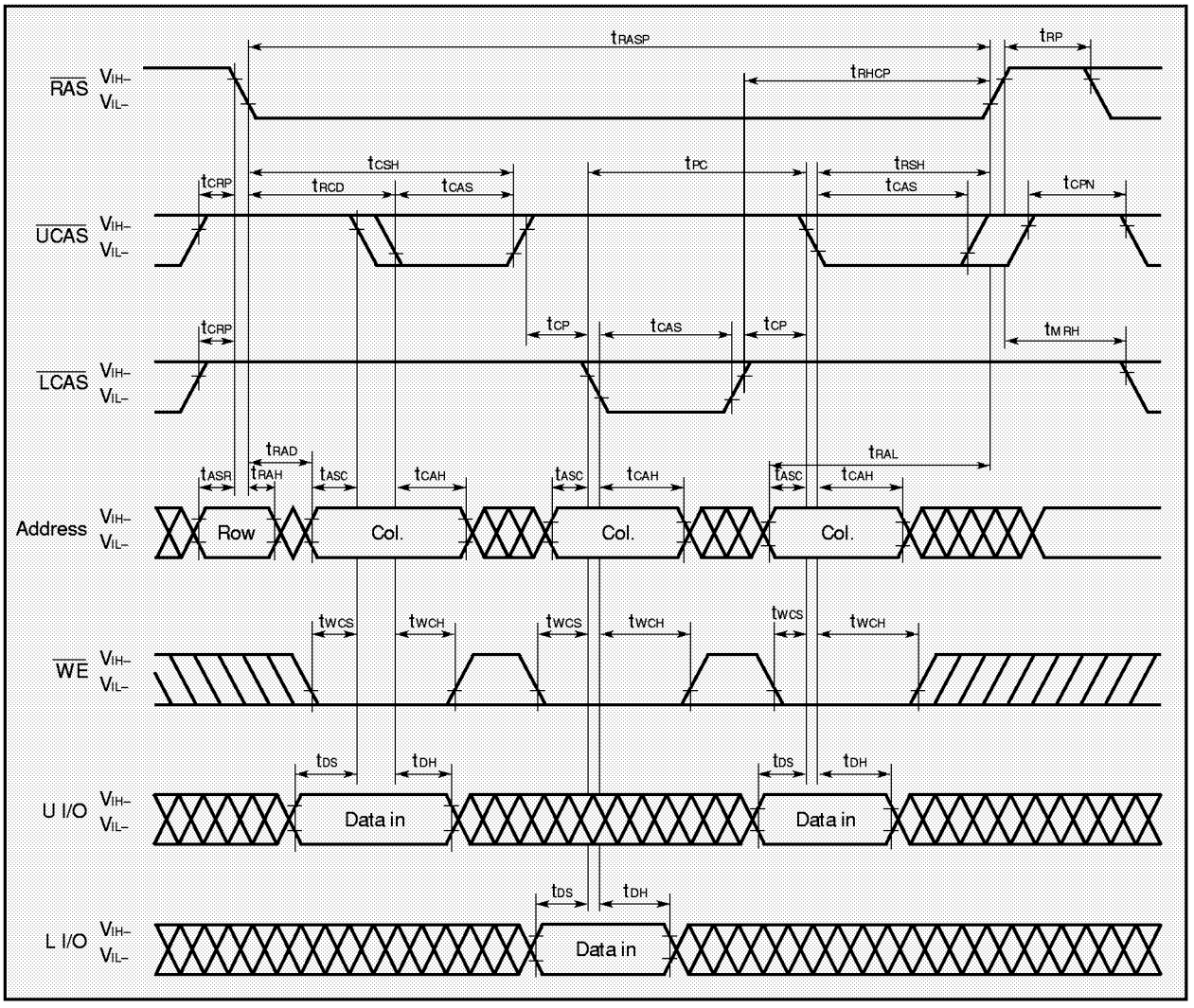
## Fast Page Mode Early Write Cycle




**Remarks** 1. $\overline{OE}$: Don't care

2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

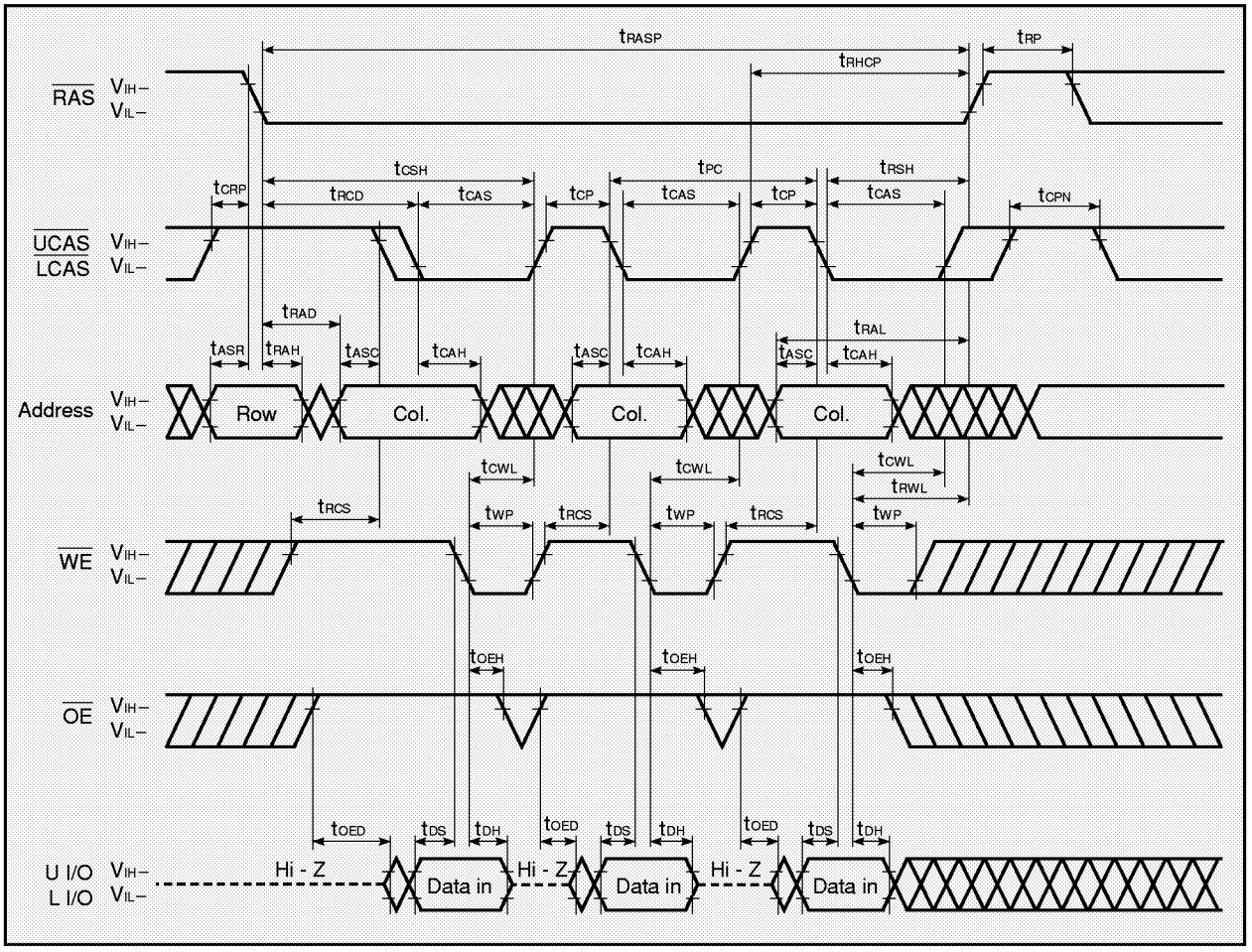
## Fast Page Mode Byte Early Write Cycle




**Remarks** 1. $\overline{OE}$: Don't care

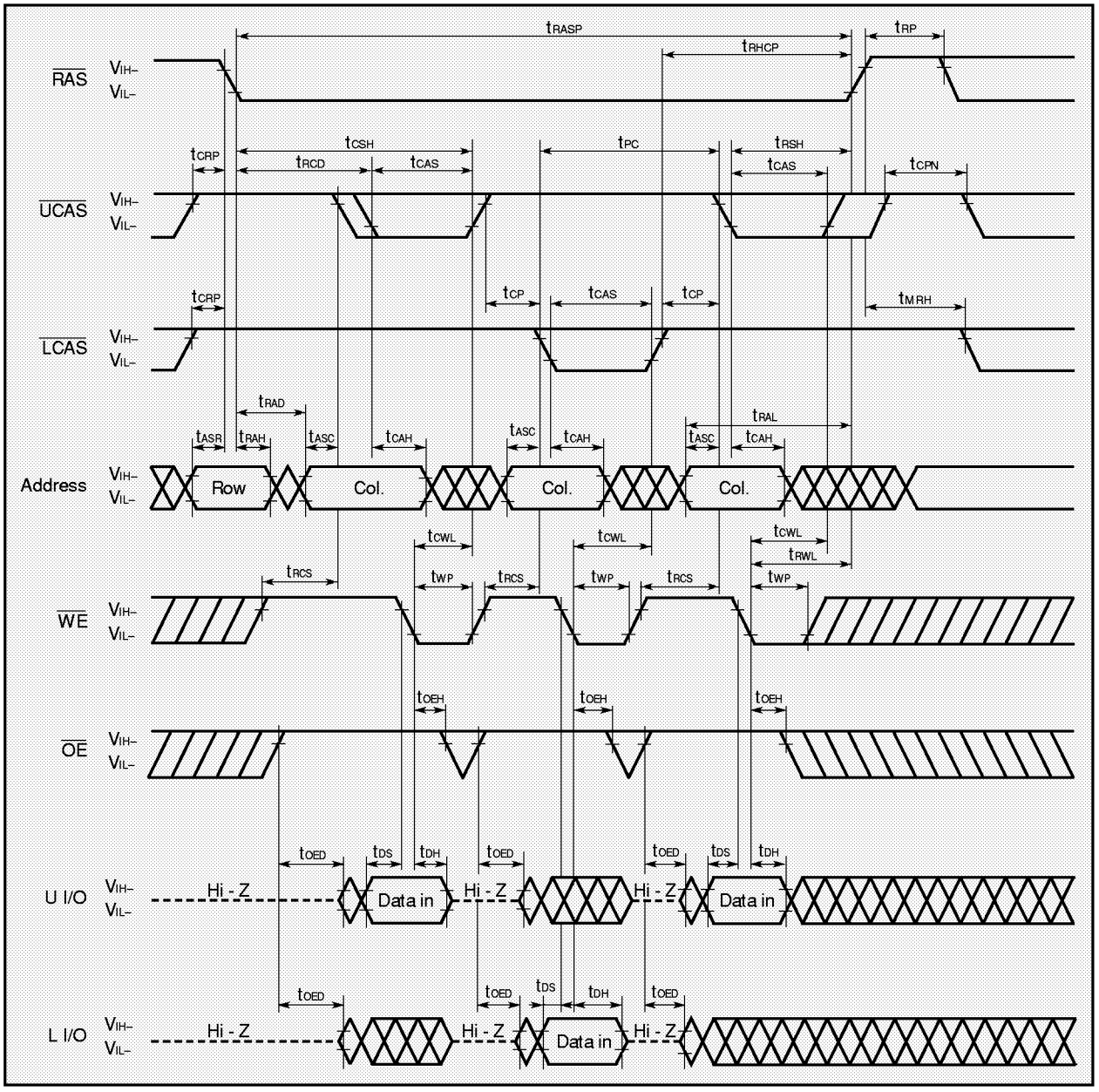
2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

### Fast Page Mode Late Write Cycle




**Remark** In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

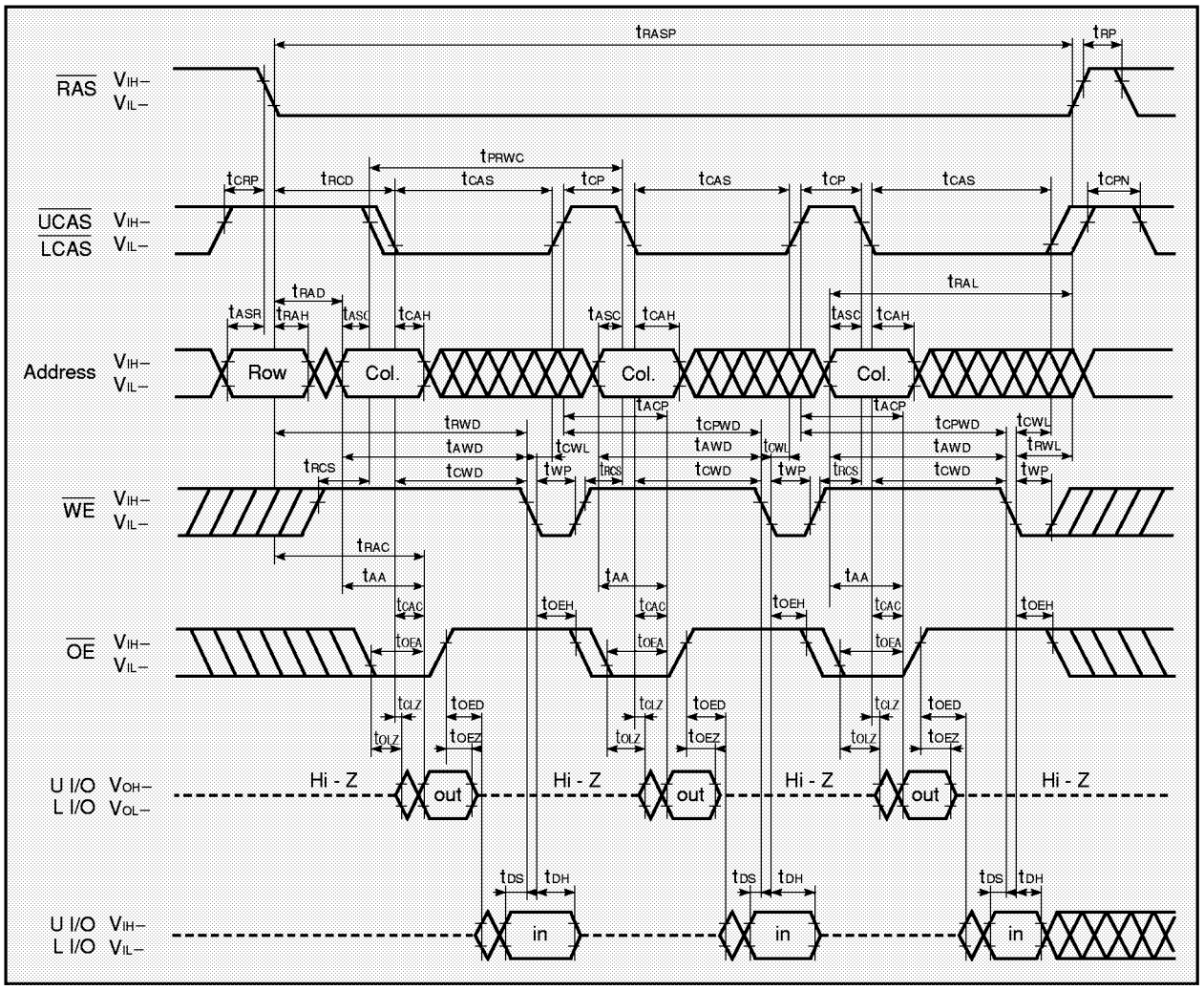
### Fast Page Mode Byte Late Write Cycle




**Remarks** 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

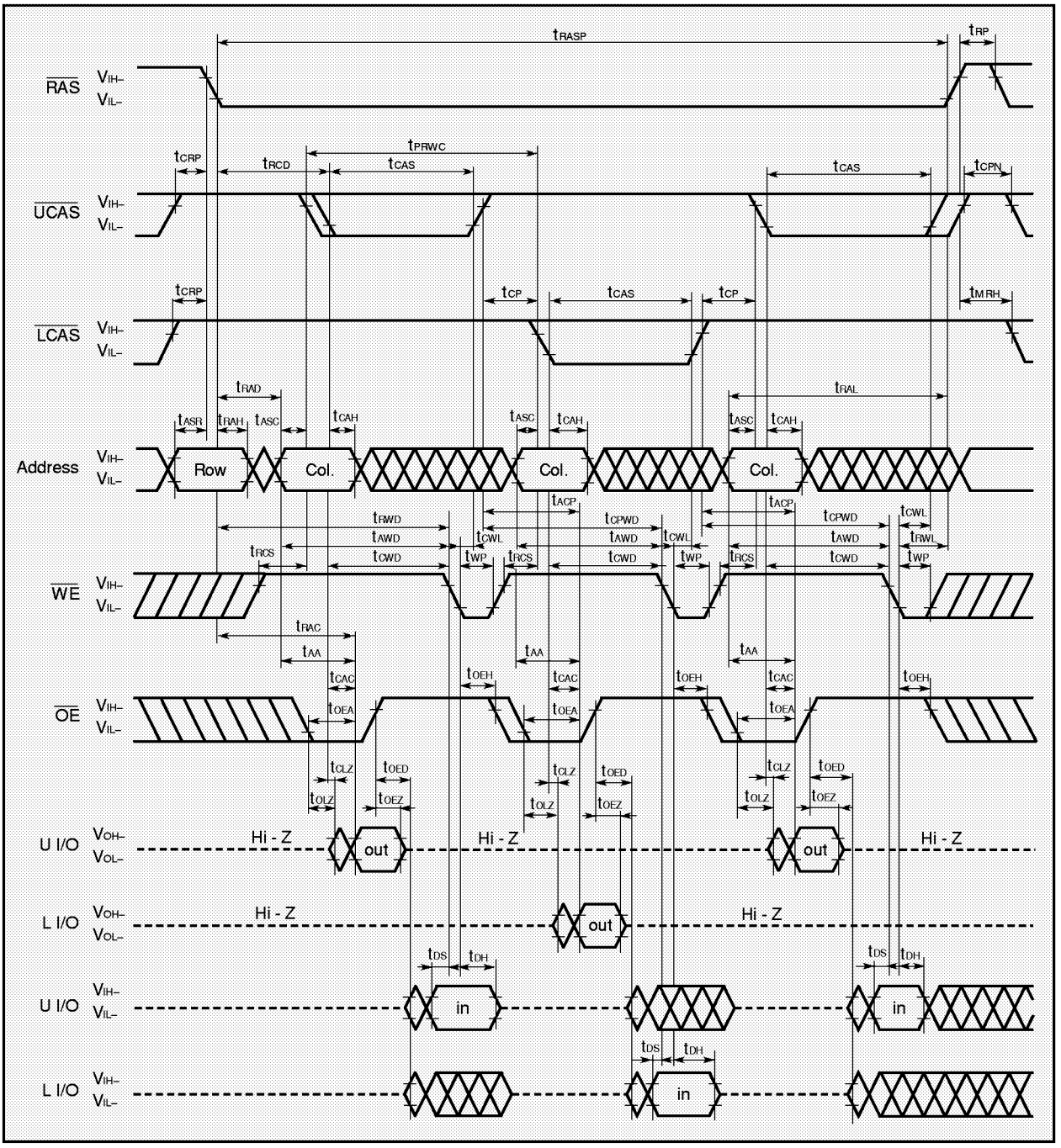
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

### Fast Page Mode Read Modify Write Cycle




**Remark** In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

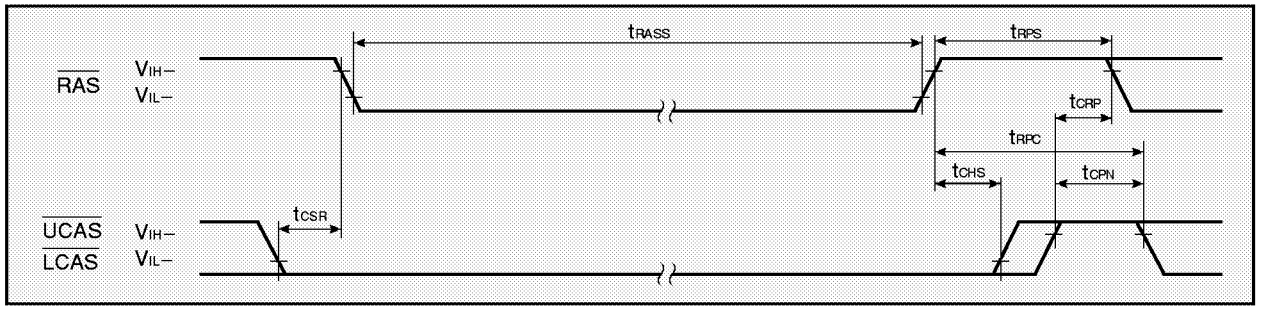
## Fast Page Mode Byte Read Modify Write Cycle




**Remarks** 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

### $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)




**Remark** Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

### Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) **Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh**
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

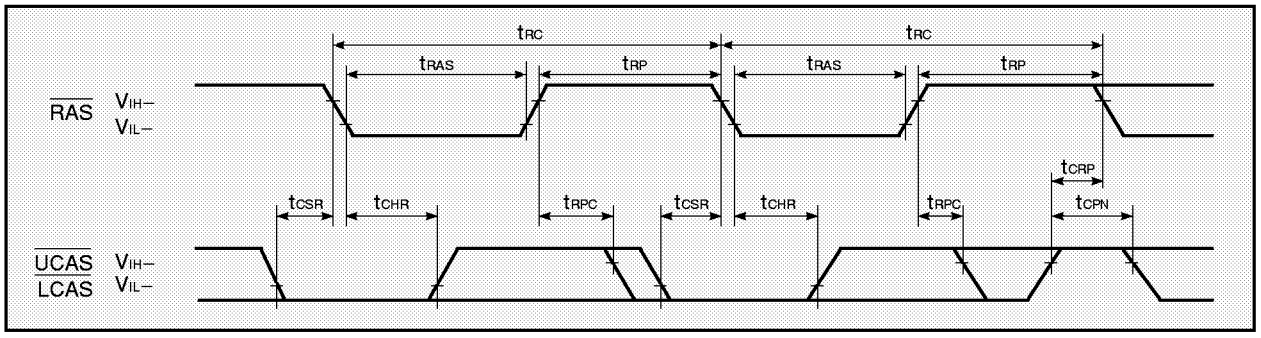
μPD42S18160: 1,024 times within a 16 ms interval

(2) **Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh**
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

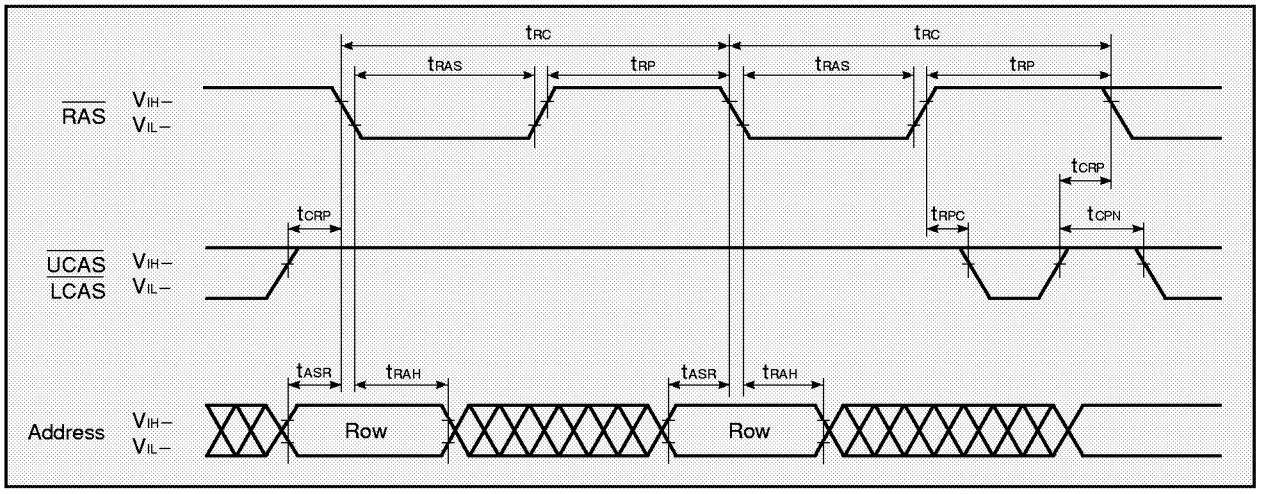
For details, please refer to **How to use DRAM** User's Manual.

### $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



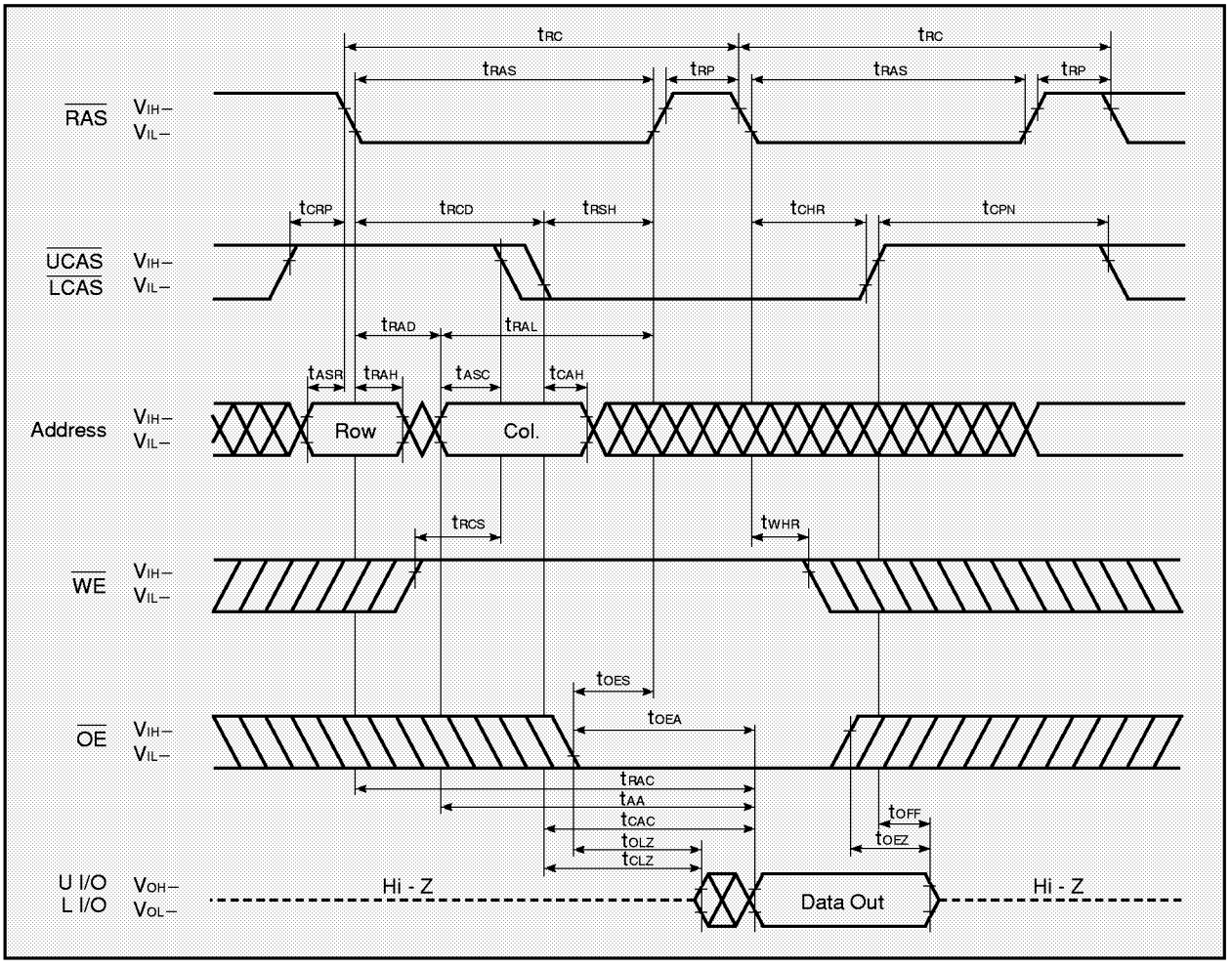

Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

### $\overline{RAS}$ Only Refresh Cycle

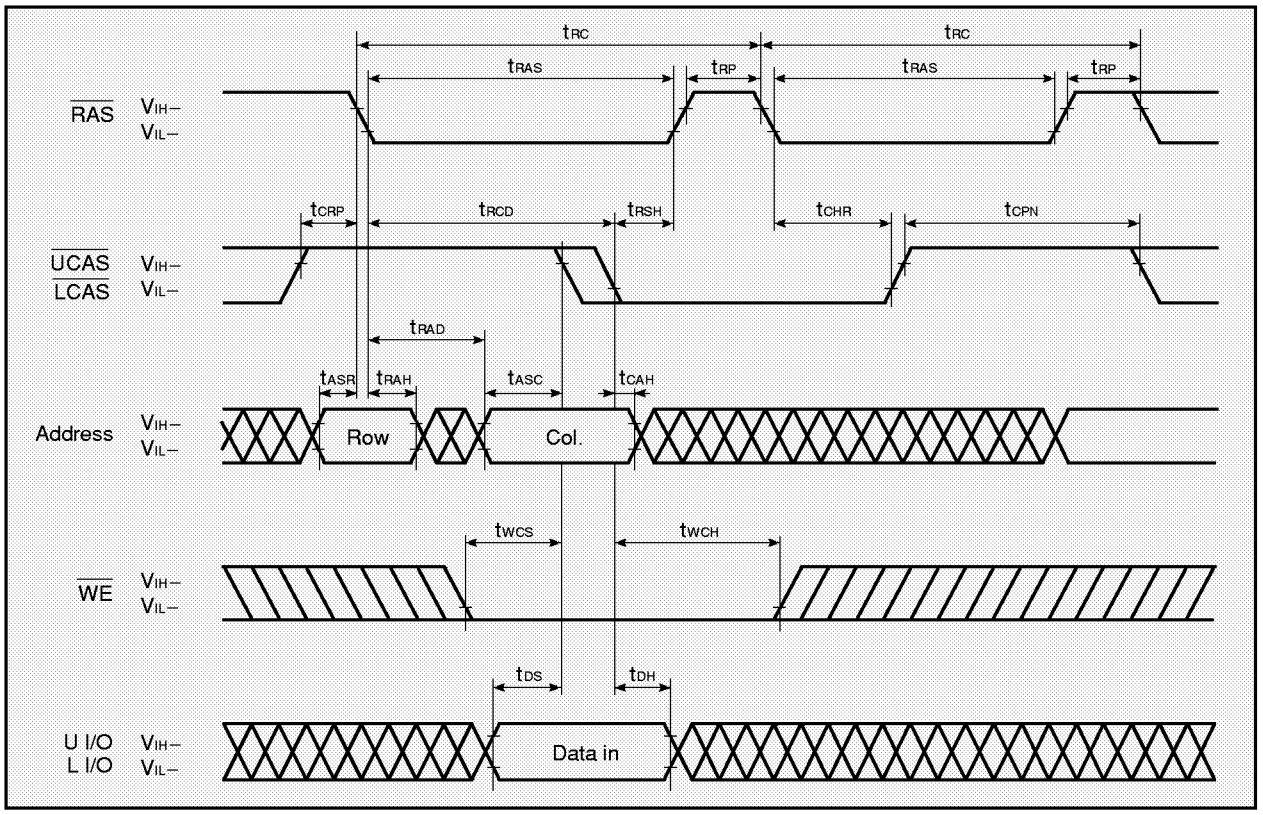



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

## Hidden Refresh Cycle (Read)



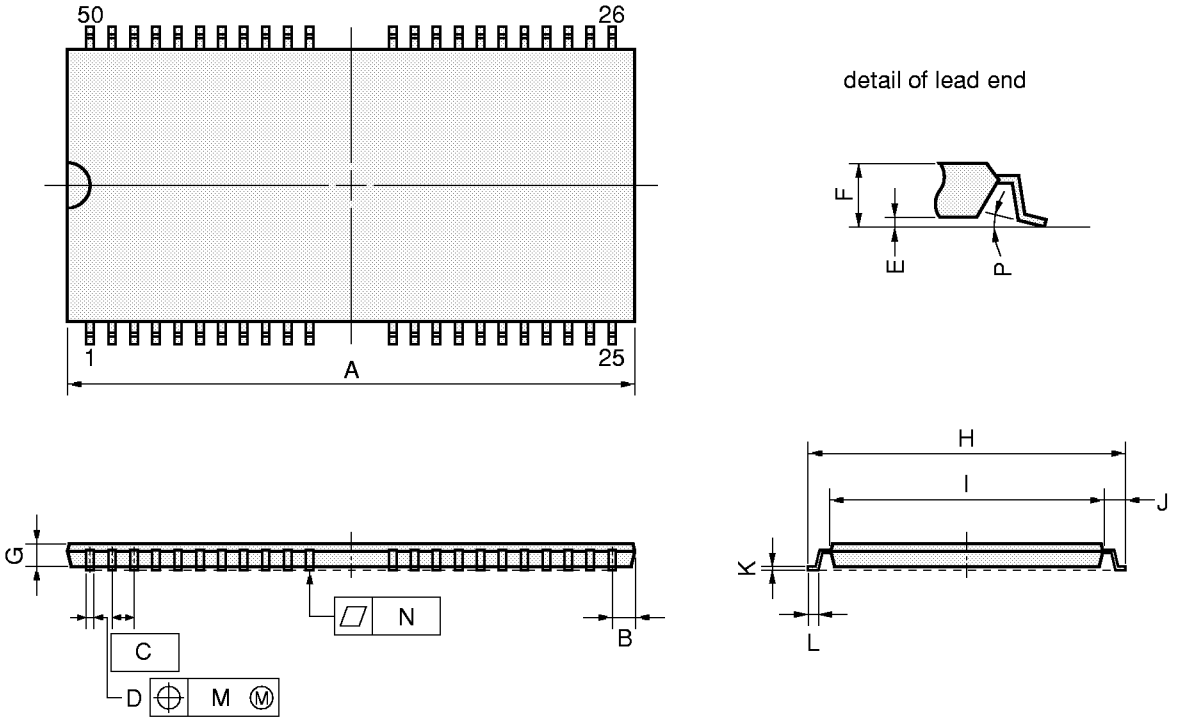
## Hidden Refresh Cycle (Write)




Remark $\overline{OE}$: Don't care

# Package Drawings

## 50PIN PLASTIC TSOP(II) (400 mil)



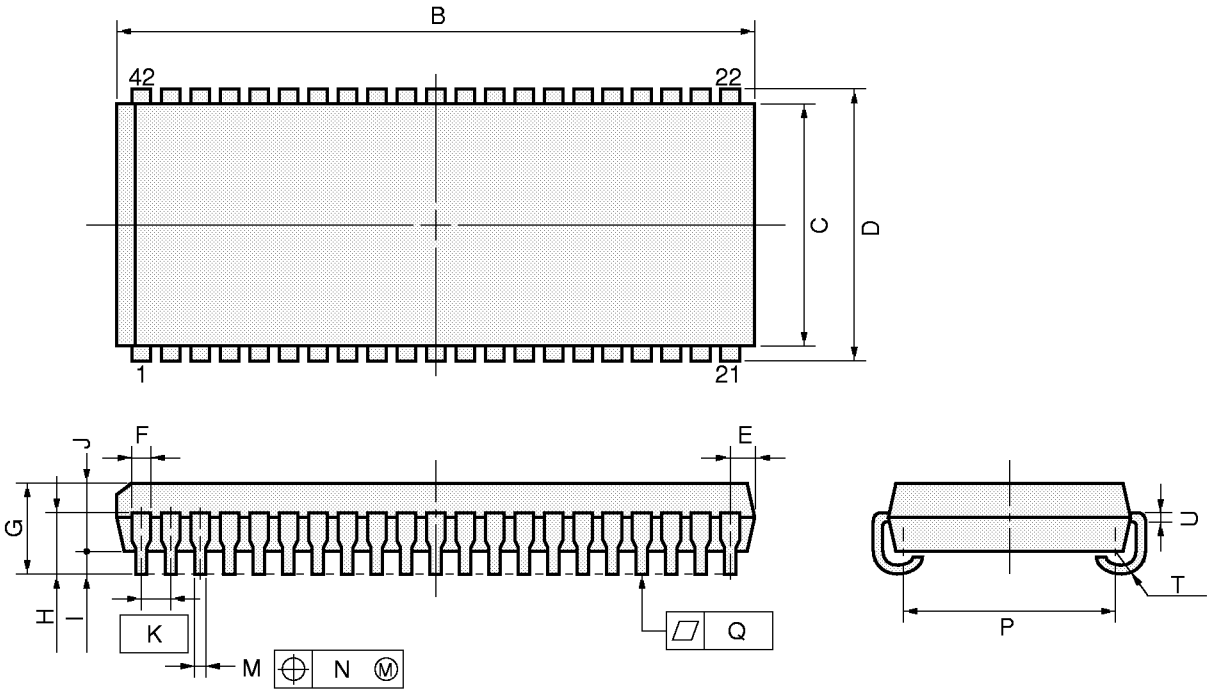

**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 21.17 MAX. | 0.834 MAX. |
| B | 1.0 MAX. | 0.040 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | $0.32^{+0.08}_{-0.07}$ | 0.013±0.003 |
| E | 0.1±0.05 | 0.004±0.002 |
| F | 1.2 MAX. | 0.048 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| K | $0.145^{+0.025}_{-0.015}$ | 0.006±0.001 |
| L | 0.5±0.1 | $0.020^{+0.004}_{-0.005}$ |
| M | 0.13 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

S50G5-80-7JF4

## 42 PIN PLASTIC SOJ (400 mil)




P42LE-400A

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| B | $27.56^{+0.2}_{-0.35}$ | $1.085^{+0.008}_{-0.014}$ |
| C | 10.16 | 0.400 |
| D | 11.18±0.2 | 0.440±0.008 |
| E | 1.08±0.15 | $0.043^{+0.006}_{-0.007}$ |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138±0.008 |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN. | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | $0.016^{+0.004}_{-0.005}$ |
| N | 0.12 | 0.005 |
| P | 9.4±0.20 | 0.370±0.008 |
| Q | 0.10 | 0.004 |
| T | R 0.85 | R 0.033 |
| U | $0.20^{+0.10}_{-0.05}$ | $0.008^{+0.004}_{-0.002}$ |

## Recommended Soldering Conditions

The following conditions (see tables below and next page) must be met when soldering μPD42S18160, 4218160.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

## Types of Surface Mount Device

μPD42S18160G5, 4218160G5: 50-pin plastic TSOP (II) (400 mil)

| Soldering process | Soldering conditions | Symbol |
|---|---|---|
| Infrared ray reflow | Peak temperature of package surface: 235 °C or lower,<br>Reflow time: 30 seconds or less (210 °C or higher),<br>Number of reflow processes: MAX. 2<br>Exposure limit: 7 days[Note]<br>(10 hours pre-baking is required at 125 °C afterwards)<br>Cautions<br>1. **After the first reflow process, cool the package down to room temperature, then start the second reflow process.**<br>2. **After the first reflow process, do not use water to remove residual flux (water can be used in the second process).** | IR35-107-2 |
| VPS | Peak temperature of package: 215 °C or lower,<br>Reflow time: 40 seconds or less (200 °C or higher),<br>Number of reflow processes: MAX. 2<br>Exposure limit: 7 days[Note]<br>(10 hours pre-baking is required at 125 °C afterwards)<br>Cautions<br>1. **After the first reflow process, cool the package down to room temperature, then start the second reflow process.**<br>2. **After the first reflow process, do not use water to remove residual flux (water can be used in the second process).** | VP15-107-2 |
| Partial heating method | Terminal temperature: 300 °C or lower,<br>Time: 3 seconds or less (Per side of the package). | — |

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution **Do not apply more than one soldering method at any one time, except for "Partial heating method".**

μPD42S18160LE, 4218160LE: 42-pin plastic SOJ (400 mil)

| Soldering process | Soldering conditions | Symbol |
|---|---|---|
| Infrared ray reflow | Peak temperature of package surface: 235 °C or lower,<br>Reflow time: 30 seconds or less (210 °C or higher),<br>Number of reflow processes: MAX. 2<br>Exposure limit: 7 days[Note]<br>(20 hours pre-baking is required at 125 °C afterwards)<br>Cautions<br>1. **After the first reflow process, cool the package down to room temperature, then start the second reflow process.**<br>2. **After the first reflow process, do not use water to remove residual flux (water can be used in the second process).** | IR35-207-2 |
| VPS | Peak temperature of package: 215 °C or lower,<br>Reflow time: 40 seconds or less (200 °C or higher),<br>Number of reflow processes: MAX. 2<br>Exposure limit: 7 days[Note]<br>(20 hours pre-baking is required at 125 °C afterwards)<br>Cautions<br>1. **After the first reflow process, cool the package down to room temperature, then start the second reflow process.**<br>2. **After the first reflow process, do not use water to remove residual flux (water can be used in the second process).** | VP15-207-2 |
| Partial heating method | Terminal temperature: 300 °C or lower,<br>Time: 3 seconds or less (Per side of the package) | — |

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution **Do not apply more than one soldering method at any one time, except for "Partial heating method".**