agere systems

Advance Data Sheet
November 2002

LCK4993V/LCK4994V
Low-Voltage PLL Clock Drivers

Features

- 12/100 MHz (LCK4993V), or 24/200 MHz (LCK4994V) output operation
- Matched pair output skew <200 ps
- Zero input-to-output delay
- 18 LVTTL 50% duty-cycle outputs capable of driving 50 Ω terminated lines
- 3.3/2.5 V LVTTL/LV differential (LVPECL), fault tolerant and hot insertable reference inputs
- Phase adjustments in 625/1300 ps steps up to ±10.4 ns
- Multiply/divide ratios of (1–6, 8, 10, 12):(1–6, 8, 10, 12)
- Operation up to 12x input frequency
- Individual output bank disable for aggressive power management and EMI reduction
- Output high-impedance (HI-Z) option for testing purposes
- Fully integrated PLL with lock indicator
- Single 3.3/2.5 V ± 10% supply
- 100-pin TQFP package
- 100-lead FSBGA package
- Pin-for-pin compatible with *CYPRESS*® CY7B993V and CY7B994V

Description

The LCK4993V and LCK4994V low-voltage PLL clock drivers offer user-selectable control over system clock functions. The multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer and communication systems.

Each of the eighteen configurable outputs drive terminated transmission lines with impedances as low as 50 Ω while delivering minimal and specified output skews at LVTTL levels. The outputs are arranged in five banks. Banks 1 to 4 allow a divide function of 1 to 12, while simultaneously allowing phase adjustments in 625 ps—1300 ps increments up to 10.4 ns. One of the output banks also includes an independent clock invert function. The feedback bank consists of two outputs, which allows divide-by functionality from 1 to 12 and limited phase adjustments. Any one of these eighteen outputs can be connected to the feedback input or drive other inputs.

Selectable reference input is a fault tolerance feature which allows smooth change over to the secondary clock source when the primary clock source is not in operation. The reference inputs and feedback inputs are configurable to accommodate both LVTTL or differential (LVPECL) inputs. The completely integrated PLL reduces jitter and simplifies board layout.

Description (continued)

Functional Diagram

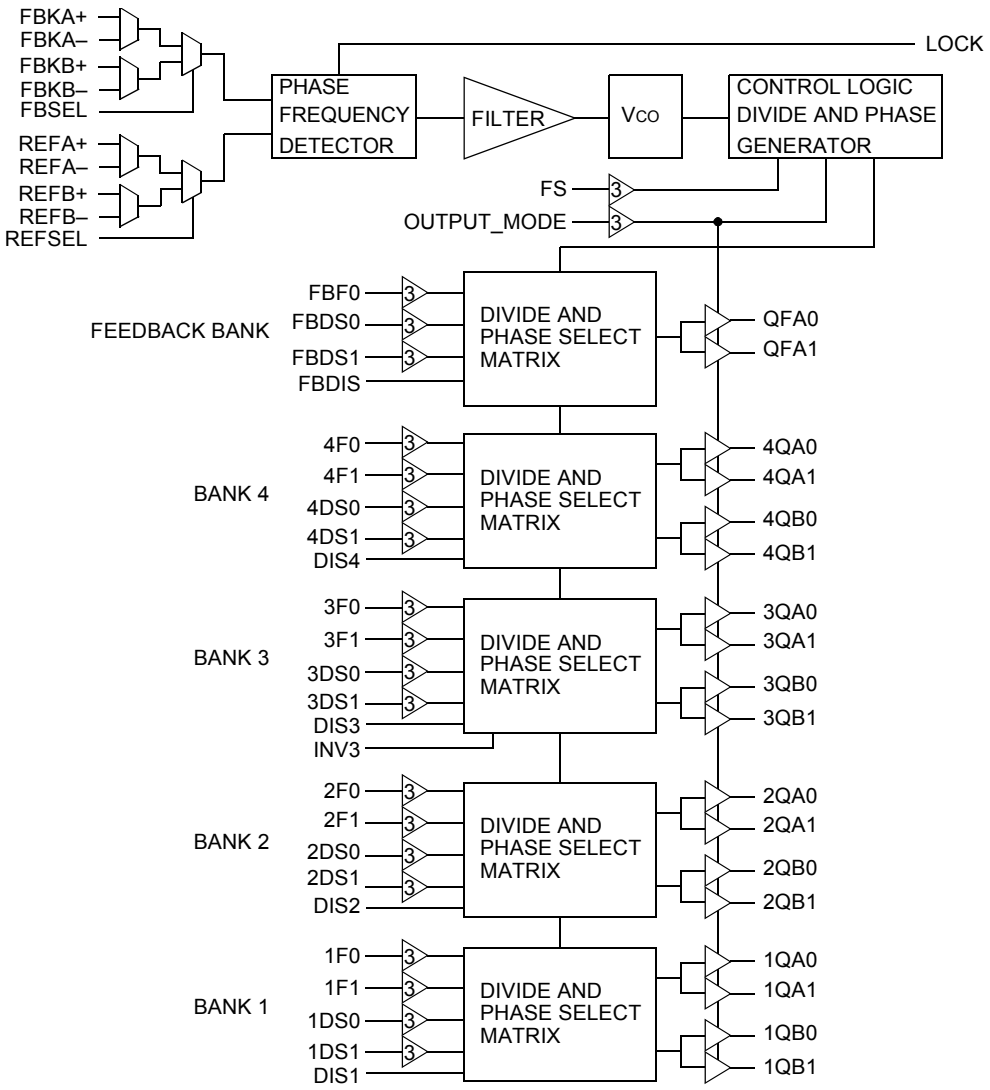


Figure 1. LCK4993V and LCK4994V Functional Diagram

Functional Diagram Description

Phase Frequency Detector and Filter

These two blocks accept signals from the REF inputs (REFA+, REFA–, REFB+, or REFB–) and the FB inputs (FBKA+, FBKA–, FBKB+, or FBKB–). Correction information is then generated to control the frequency of the voltage controlled oscillator (VCO). These two blocks, along with the VCO, form a phase-locked loop (PLL) that tracks the incoming REF signal.

The devices have a flexible REF and FB input scheme. These inputs allow the use of either differential LVPECL or single-ended LVTTL inputs. To configure as single-ended LVTTL inputs, the complementary pin must be left open (internally pulled to 1.5 V), then the other input pin can be used as an LVTTL input. The REF inputs are also tolerant to hot insertion.

Description (continued)

Functional Diagram Description (continued)

The REF inputs can be changed dynamically. When changing from one reference input to the other reference input of the same frequency, the PLL is optimized to ensure that the clock outputs period will not be less than the calculated system budget ($t_{MIN} = t_{REF}$ (nominal reference clock period) – t_{CCJ} (cycle-to-cycle jitter) – t_{PDEV} (maximum period deviation)) while reacquiring lock.

VCO, Control Logic, Divider, and Phase Generator

The VCO accepts analog control inputs from the PLL filter block. The FS control pin setting determines the nominal operational frequency (f_{NOM}) range of the divide-by-one output of the device. f_{NOM} is directly related to the VCO frequency. There are two versions of the device, a low-speed device (LCK4993V) where f_{NOM} ranges from 12 MHz to 100 MHz, and a high-speed device (LCK4994) which ranges from 24 MHz to 200 MHz. The FS setting for each device is shown in Table 1.

The f_{NOM} frequency is seen on divide-by-one outputs. For the LCK4994V, the upper f_{NOM} range extends from 96 MHz to 200 MHz.

Table 1. Frequency Range Select

FS[1]	LCK4993V		LCK4994V	
	f_{NOM} (MHz)		f_{NOM} (MHz)	
	Min	Max	Min	Max
Low	12	26	24	52
Mid	24	52	48	100
High	48	100	96	200

1. The level to be set on FS is determined by the f_{NOM} of the VCO and phase generator. f_{NOM} always appears on an output when the output is operating in the undivided mode. The REF and FB are at f_{NOM} when the output connected to FB is undivided.

Time Unit Definition

Selectable skew is in discrete increments of time unit (t_U). The value of t_U is determined by the FS setting and the maximum nominal output frequency. The equation to be used to determine the t_U is as follows:

$$t_U = \frac{1}{f_{NOM} \times N} \quad \text{(eq. 1)}$$

Where N is a multiplication factor which is determined by the FS setting and is defined in Table 2; and f_{NOM} is the nominal frequency of the device.

Table 2. N Factor Determination

FS	LCK4993V		LCK4994V	
	N	f_{NOM} (MHz) at which t_U = 1.0 ns	N	f_{NOM} (MHz) at which t_U = 1.0 ns
Low	64	15.265	32	31.25
Mid	32	31.25	16	62.5
High	16	62.5	8	125

Description (continued)

Functional Diagram Description (continued)

Divide and Phase Select Matrix

The divide and phase select matrix is comprised of five independent banks: four banks of clock outputs and one bank for feedback. Each clock output bank has two pairs of low-skew, high-fanout output buffers ([1:4]Q[A:B][0:1]), two phase function select inputs ([1:4]F[0:1]), two divider function selects ([1:4]DS[0:1]), and one output disable (DIS[1:4]).

The feedback bank has one pair of low-skew, high-fanout output buffers (QFA[0:1]). One of these outputs may connect to the selected feedback input (FBK[A:B]±). This feedback bank also has one phase function select input (FBF0), two divider function selects FSDS[0:1], and one output disable (FBDIS).

The phase capabilities that are chosen by the phase function select pins are shown in Table 3. The divide capabilities for each bank are shown in Table 4.

Table 3. Output Skew Select Function

Function Selects		Output Skew Function				
[1:4]F1	[1:4]F0 and FBF0	Bank1	Bank2	Bank3	Bank4	Feedback Bank
Low	Low	–4 tu	–4 tu	–8 tu	–8 tu	–4 tu
Low	Mid	–3 tu	–3 tu	–7 tu	–7 tu	NA
Low	High	–2 tu	–2 tu	–6 tu	–6 tu	NA
Mid	Low	– 1tu	–1 tu	BK1[1]	BK1[1]	NA
Mid	Mid	0 tu	0 tu	0 tu	0 tu	0 tu
Mid	High	1 tu	1 tu	BK2[1]	BK2[1]	NA
High	Low	2 tu	2 tu	6 tu	6 tu	NA
High	Mid	3 tu	3 tu	7 tu	7 tu	NA
High	High	4 tu	4 tu	8 tu	8 tu	4 tu

1. BK1 and BK2 denote following the skew of Bank1 and Bank2, respectively.

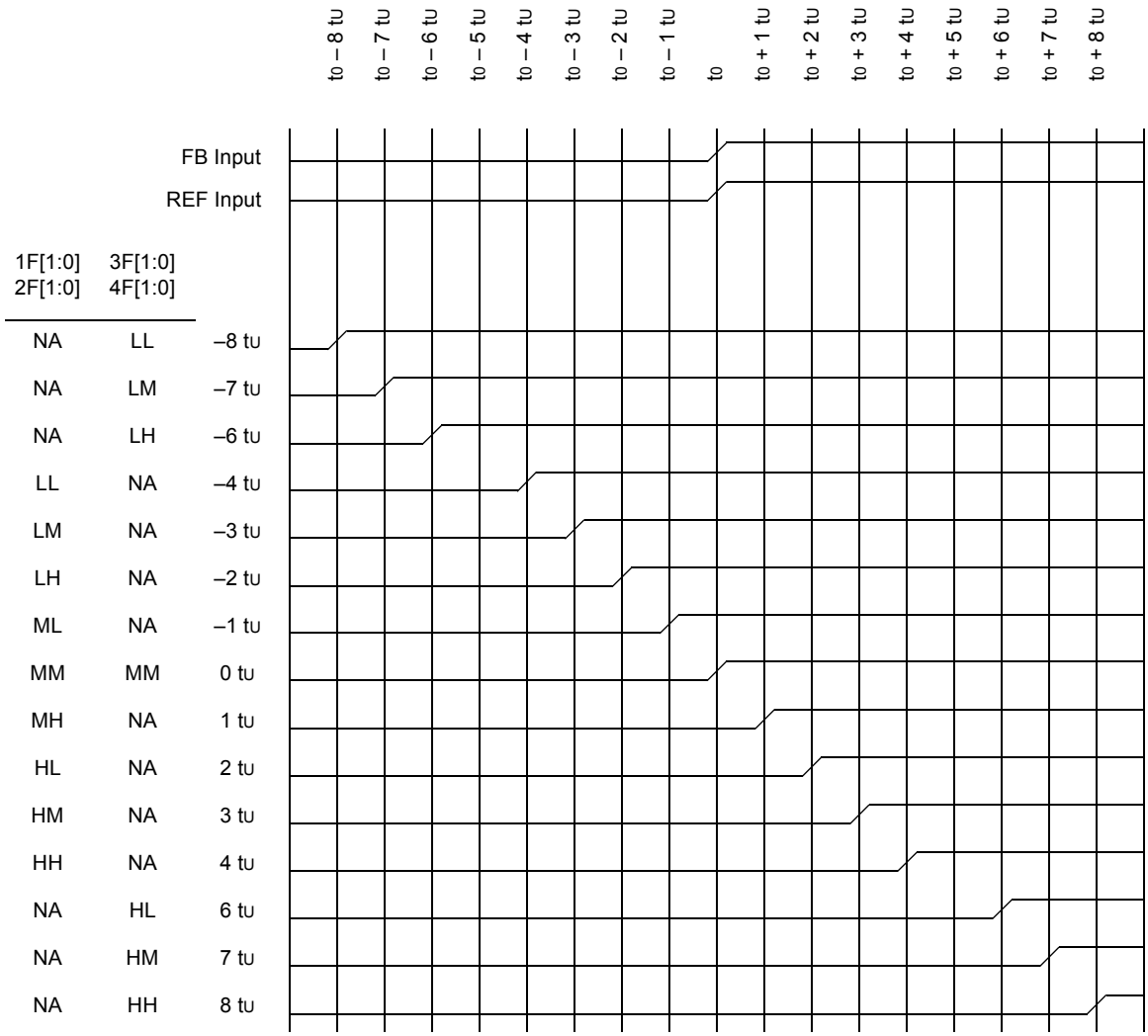
Table 4. Output Divider Function

Function Selects		Output Divider Function				
[1:4]DS1 and FBDS1	[1:4]DS0 and FBDS0	Bank1	Bank2	Bank3	Bank4	Feedback Bank
Low	Low	/1	/1	/1	/1	/1
Low	Mid	/2	/2	/2	/2	/2
Low	High	/3	/3	/3	/3	/3
Mid	Low	/4	/4	/4	/4	/4
Mid	Mid	/5	/5	/5	/5	/5
Mid	High	/6	/6	/6	/6	/6
High	Low	/8	/8	/8	/8	/8
High	Mid	/10	/10	/10	/10	/10
High	High	/12	/12	/12	/12	/12

Description (continued)

Functional Diagram Description (continued)

Figure 2 illustrates the timing relationship of programmable skew outputs. All times are measured with respect to REF with the output used for feedback programed with 0 tU skew. The PLL naturally aligns the rising edge of the FB input and REF input. If the output used for feedback is programmed to another skew position, then the whole tU matrix will shift with respect to REF. For example, it the output used for feedback is programmed to shift –8 tU, then the whole matrix is shifted forward in time by 8 tU. Thus, an output programed with 8 tU of skew will effectively be skewed 16 tU with respect to REF.



Note: FB connected to an output selected for zero skew (i.e., FBF0 = mid or XF[1:0] = mid).

Figure 2. Typical Outputs with FB Connected to a Zero-Skew Output

Description (continued)

Functional Diagram Description (continued)

Output Disable Description

The feedback divide and phase select matrix bank has two outputs, and each of the four divide and phase select matrix banks have four outputs. The outputs of each bank can be independently put into a hold-off or HI-Z state. The combination of the OUTPUT_MODE and DIS[1:4]/FBDIS inputs determines the clock outputs' state for each bank. When the DIS[1:4]/FBDIS is LOW, the outputs of the corresponding bank will be enabled. When the DIS[1:4]/FBDIS is HIGH, the outputs for that bank will be disabled to a HI-Z or hold-off state depending on the OUTPUT_MODE input. Table 5 defines the disabled output functions.

The hold-off state is intended to be a power saving feature. An output bank is disabled to the hold-off state in a maximum of six output clock cycles from the time when the disable input (DIS[1:4]/FBDIS) is high. When disabled to the hold-off state, noninverting outputs are driven to a logic-low state on its falling edge. Inverting outputs are driven to a logic-high state on its rising edge. This ensures the output clocks are stopped without a glitch. When a bank of outputs is disabled to HI-Z state, the respective bank of outputs will go HI-Z immediately.

Table 5. DIS[1:4]/FBDIS Pin Functionality

OUTPUT_MODE	DIS[1:4]/FBDIS	Output Mode
High/Low	Low	Enabled
High	High	HI-Z
Low	High	Hold-off
Mid	X	Factory Test

INV3 Pin Function

Bank3 has signal invert capability. The four outputs of Bank3 will act as two pairs of complementary outputs when the INV3 pin is driven low. In complementary output mode, 3QA0 and 3QB0 are noninverting; 3QA1and 3QB1 are inverting outputs. All four outputs will be inverted when the INV3 pin is driven high. When the INV3 pin is left in mid, the outputs will not invert. Inversion of the outputs are independent of the skew and divide functions. Therefore, clock outputs of Bank3 can be inverted, divided, and skewed at the same time.

Lock Detect Output Description

The LOCK detect output indicates the lock condition of the integrated PLL. Lock detection is accomplished by comparing the phase difference between the reference and feedback inputs. Phase error is declared when the phase difference between the two inputs is greater than the specified device propagation delay limit ($t_{PDFSL, M, H}$).

When in the locked state, after four or more consecutive feedback clock cycles with phase-errors, the LOCK output will be forced low to indicate out-of-lock state.

When in the out-of-lock state, 32 consecutive phase-errorless feedback clock cycles are required to allow the LOCK output to indicate lock condition (LOCK = high).

If the feedback clock is removed after LOCK has gone high, a watchdog circuit is implemented to indicate the out-of-lock condition after a time-out period by deasserting LOCK low. This time-out period is based upon a divided down reference clock.

This assumes that there is activity on the selected REF input. If there is no activity on the selected REF input then the LOCK detect pin may not accurately reflect the state of the internal PLL.

Description (continued)

Functional Diagram Description (continued)

Factory Test Mode Description

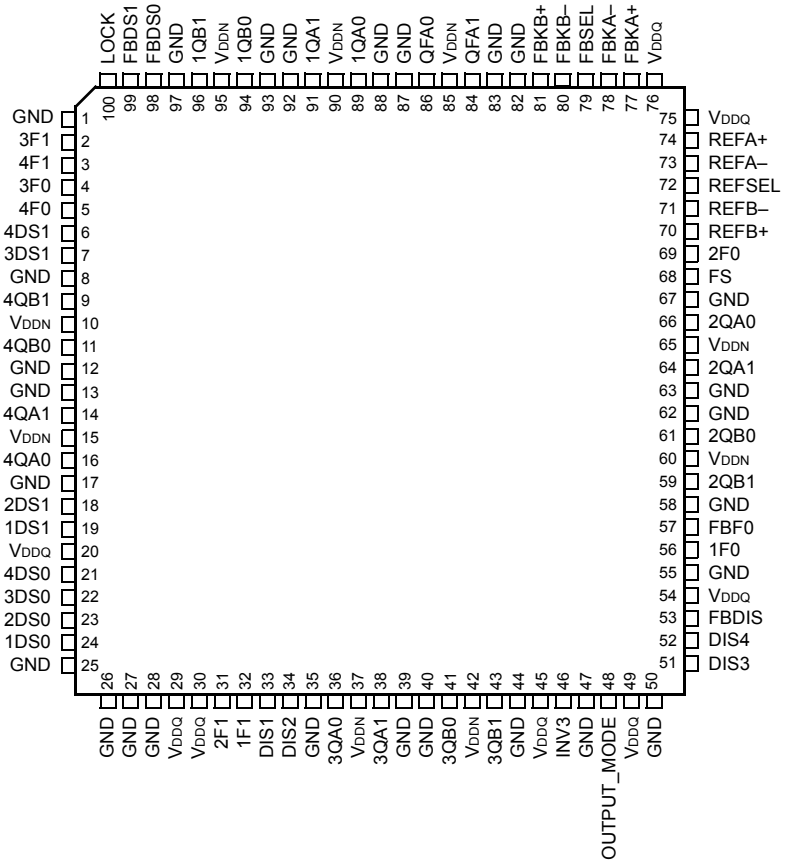
The device will enter factory test mode when the OUTPUT_MODE is driven to mid. In factory test mode, the device will operate with its internal PLL disconnected. The input level supplied to the reference input will be used in place of the PLL output. In TEST mode, the selected FB input(s) must be tied low. All functions of the device are still operational in factory test mode except the internal PLL and output bank disables. The OUTPUT_MODE input is designed to be a static input. Dynamically toggling this input from low to high may temporarily cause the device to go into factory test mode (when passing through the mid state).

Factory Test Reset

When in factory test mode (OUTPUT_MODE = mid), the device can be reset to a deterministic state by driving the DIS4 input high. When the DIS4 input is driven high in factory test mode, all clock outputs will go to HI-Z; after the selected reference clock pin has five positive transitions, all the internal finite state machines (FSM) will be set to a deterministic state. The deterministic state of the state machines will depend on the configurations of the divide selects, skew selects, and frequency select input. All clock outputs will stay in high-impedance mode and all FSMs will stay in the deterministic state until DIS4 is deasserted. When DIS4 is deasserted (with OUTPUT_MODE still at mid), the device will re-enter factory test mode.

Pin Information

Pin Diagram



5-8885 (F) r.1

Figure 3. 100-Pin TQFP Package (Top View)

Pin Information (continued)

Pin Descriptions

Table 6. Pin Descriptions

For all 3-state inputs, low indicates a connection to GND, mid indicates an open connection, and high indicates a connection to V_{DD}. Internal termination circuitry holds an unconnected input to $V_{DD}/2$

Pin	Symbol	Type	I/O	Description
1, 8, 12, 13, 17, 25—28, 35, 39, 40, 44, 47, 50, 55, 58, 62, 63, 67, 82, 83, 87, 88, 92, 93, 97	GND	Power	—	**Ground.**
2—5, 31, 32, 56, 69	[1:4]F[0:1]	3-Level Input	I	**Output Phase Function Select.** Each pair controls the phase function of the respective bank of outputs. See Table 3.
6, 7, 18, 19, 21—24,	[1:4]DS[0:1]	3-Level Input	I	**Output Divider Function Select.** Each pair controls the phase function of the respective bank of outputs. See Table 4.
9, 11, 14, 16, 36, 38, 41, 43, 59, 61, 64, 66, 89, 91, 94, 96	[1:4]Q[A:B][0:1]	LVTTL	I	**Clock Output.** These outputs provide numerous divide and phase select functions determined by the [1:4]DS[0:1] and [1:4]F[0:1] inputs.
10, 15, 37, 42, 60, 65, 85, 90, 95	V_{DDN}	Power	—	**Output Buffer Power.** Power supply for each output pair.
20, 29, 30, 45, 49, 54, 75, 76	V_{DDQ}	Power	—	**Internal Power.** Power supply for the internal circuitry.
33, 34, 51, 52	DIS[1:4]	LVTTL	I	**Output Disable.** Each input controls the state of the respective output bank. Low = The [1:4]Q[A:B][0:1] is enabled. See Table 5. High = The output bank is disabled to the hold-off or HI-Z state; the disable state is determined by OUTPUT_MODE. These inputs each have an internal pull-down resistor.
46	INV3	3-Level Input	I	**Invert Mode.** This input only affects Bank3. Low = Each matched output pair will become complementary (3QA0+, 3QA1–, 3QB0+, 3QB1–). Mid = All four outputs will be noninverting. High = All four outputs in the same bank will be inverted.
48	OUTPUT_MODE	3-Level Input	I	**Output Mode.** This pin determines the clock outputs' disable state. Low = The clock outputs will disable to HOLD-OFF mode. Mid = The device enters factory test mode. High = The clock outputs will disable to HI-Z.
53	FBDIS	LVTTL	I	**Feedback Disable.** This input controls the state of QFA[0:1]. Low = The QFA[0:1] is enabled. See Table 5. High = The QFA[0:1] is disabled to the HOLD-OFF or HI-Z state; the disable state is determined by OUTPUT_MODE. This input each have an internal pull-down resistor.

Pin Information (continued)

Pin Descriptions (continued)

Table 6. Pin Descriptions (continued)

Pin	Symbol	Type	I/O	Description
57	FBF0	3-Level Input	I	**Feedback Output Phase Function Select.** This input determines the phase function of the feedback banks QFA[0:1] outputs. See Table 3.
70, 71, 73, 74	REFB+, REFB–, REFA–, REFA+	LVTTL/ LVDIFF	I	**Reference Inputs.** These inputs can operate as differential PECL or single-ended TTL reference inputs to the PLL. When operating as a single-ended LVTTL input, the complementary input must be left open.
72	REFSEL	LVTTL	I	**Reference Input Select.** The REFSEL input controls how the reference input is configured. Low = REFSEL uses the REFA pair as the reference input. High = REFSEL uses the REFB pair as the reference input. This input each have an internal pull-down resistor.
77, 78, 80, 81	FBKA+, FBKA–, FBKB–, FBKB+	LVTTL/ LVDIFF	I	**Feedback Inputs.** One pair of inputs selected by the FBSEL is used to feedback the clock output xQn to the phase detector. The PLL will operate such that the rising edges of the reference and feedback signals are aligned in both phase and frequency. These inputs can operate as differential PECL or single-ended TTL inputs. When operating as a single-ended LVTTL input, the complementary input must be left open.
79	FBSEL	LVTTL	I	**Feedback Input Select.** Low = FBKA inputs are selected. High = FBKB inputs are selected. This input each have an internal pull-down resistor.
84, 86	QFA[0:1]	LVTTL	O	**Clock Feedback Output.** This pair of clock outputs is intended to be connected to the FB input. These outputs have numerous divide options and three choices of phase adjustments. The function is determined by the setting of the FBDS[0:1] pins and FBF0.
98, 99	FBDS[0:1]	3-Level Input	I	**Feedback Divider Function Select.** These inputs determine the function of the QFA0 and QFA1 outputs. See Table 4.
100	LOCK	LVTTL	O	**PLL Lock Indicator.** Low = The PLL is attempting to acquire lock. High = This output indicates the internal PLL is locked to the reference signal.

Pin Information (continued)

Pin Assignments

Table 7. 100-Pin FSBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10
A	1QB1	1QB0	1QA1	1QA0	QFA0	QFA1	FBKB+	V_{DDQ}	FBKA–	FBKA+
B	V_{DDN}	V_{DDN}	V_{DDN}	V_{DDN}	V_{DDN}	V_{DDN}	V_{DDQ}	FBKB–	FBSEL	REFA+
C	GND	GND	GND	GND	GND	GND	V_{DDQ}	GND	GND	REFA–
D	LOCK	4F0	3F1	GND	FBDS1	FBDS0	2F0	V_{DDQ}	REFSEL	REFB–
E	4QB1	V_{DDN}	4DS1	GND	3F0	4F1	GND	FS	V_{DDN}	REFB+
F	4QB0	V_{DDN}	3DS1	GND	GND	GND	GND	FBF0	V_{DDN}	2QA0
G	4QA1	2DS1	V_{DDQ}	GND	GND	GND	GND	V_{DDQ}	1F0	2QA1
H	4QA0	1DS1	1DS0	V_{DDQ}	GND	GND	V_{DDQ}	OUTPUT_MODE	FBDIS	2QB0
J	4DS0	3DS0	2DS0	DIS1	V_{DDN}	V_{DDN}	GND	INV3	DIS3	2QB1
K	2F1	1F1	DIS2	V_{DDN}	3QA0	3QA1	GND	3QB0	3QB1	DIS4

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–40	125	°C
Supply Voltage	V_{DD}	–0.5	4.6	V
dc Input Voltage	V_{DC}	–0.3	V_{DD} + 0.5	V
Output Current into Outputs (low)	I_{OUT}	—	40	mA
Latch-Up Current	I_L	—	±200	mA

Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 9. Handling Precautions

Device	Minimum Threshold	
	HBM	CDM
LCK4993V	2000 V	500 V
LCK4994V	2000 V	500 V

CAUTION: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Recommended Operating Conditions

Table 10. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Commercial Ambient Temperature V_{DD} = 3.3/2.5 V ± 10%	T_{AC}	0	70	°C
Industrial Ambient Temperature V_{DD} = 3.3/2.5 V ± 10%	T_{AI}	–40	85	°C
Ambient Temperature (with power applied)	T_A	–40	125	°C

Electrical Characteristics

Table 11. Electrical Characteristics

Parameter	Symbol	Description	Test Conditions	Min	Max	Unit
LVTTL Compatible Output Pins (QFA[0:1], [1:4]Q[A:B], LOCK						
High-Voltage Output (LVTTL)	V_{OH}	QFA[0:1], [1:4]Q[A:B][0:1]	V_{DD} = Min, I_{OH} = –30 mA	2.4	—	V
		LOCK	V_{DD} = Min, I_{OH} = –2 mA	2.4	—	V
Low-Voltage Output (LVTTL)	V_{OL}	QFA[0:1], [1:4]Q[A:B][0:1]	V_{DD} = Min, I_{OH} = 30 mA	—	0.5	V
		LOCK	V_{DD} = Min, I_{OH} = 2 mA	—	0.5	V
High-Impedance State Leakage Current	I_{OZ}	—	—	–100	100	µA
LVTTL Compatible Pins (FBKA±, FBKB±, REFA±, REFB±, FBSEL, REFSEL, FBDIS, DIS[1:4])						
High-Voltage Input (LVTTL)	V_{IH}	FBK[A:B]±, REF[A:B]±	Min ≤ V_{DD} ≤ Max	2.0	V_{DD} + 0.3	V
		REFSEL, FBSEL, FBDIS, DIS[1:4]	—	2.0	V_{DD} + 0.3	V
Low-Voltage Input (LVTTL)	V_{IL}	FBK[A:B]±, REF[A:B]±	Min ≤ V_{DD} ≤ Max	–0.3	0.8	V
		REFSEL, FBSEL, FBDIS, DIS[1:4]	—	–0.3	0.8	V
Input Current V_{IN} > V_{DD} (LVTTL)	I_{IN}	FBK[A:B]±, REF[A:B]±	V_{DD} = GND, V_{IN} = 3.63 V	—	100	µA
High-Input Current (LVTTL)	I_{IH}	FBK[A:B]±, REF[A:B]±	V_{DD} = Max, V_{IN} = V_{DD}	—	500	µA
		REFSEL, FBSEL, FBDIS, DIS[1:4]	V_{IN} = V_{DD}	—	500	µA
Low-Input Current (LVTTL)	I_{IL}	FBK[A:B]±, REF[A:B]±	V_{DD} = Max, V_{IN} = GND	—	500	µA
		REFSEL, FBSEL, FBDIS, DIS[1:4]	—	–500	—	µA
3-Level Input Pins (FBF0, FBDS[0:1], [1:4]F[0:1], [1:4]DS[0:1], FS, OUTPUT_MODE(TEST)						
Low-Voltage 3-Level Input[1]	V_{ILL}	—	Min ≤ V_{DD} ≤ Max	—	0.13 x V_{DD}	V
Mid-Voltage 3-Level Input[1]	V_{IMM}	—	Min ≤ V_{DD} ≤ Max	0.47 x V_{DD}	0.53 x V_{DD}	V
High-Voltage 3-Level Input[1]	V_{IHH}	—	Min ≤ V_{DD} ≤ Max	0.87 x V_{DD}	—	V
Low-Current 3-Level Input	I_{ILL}	3-level input pins excluding FBF0	V_{IN} = GND	–200	—	µA
		FBF0	V_{IN} = GND	–400	—	µA
Mid-Current 3-Level Input	I_{IMM}	3-level input pins excluding FBF0	V_{IN} = V_{DD}/2	–50	50	µA
		FBF0	V_{IN} = V_{DD}/2	–100	100	µA
High-Current 3-Level Input	I_{IHH}	3-level input pins excluding FBF0	V_{IN} = V_{DD}	—	200	µA
		FBF0	V_{IN} = V_{DD}	—	400	µA

1. These inputs are normally wired to V_{DD}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{DD}). Internal termination resistors hold the unconnected inputs at V_{DD}/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.

Electrical Characteristics (continued)

Table 11. Electrical Characteristics (continued)

Parameter	Symbol	Description	Test Conditions	Min	Max	Unit
LVDIFF Input Pins (FBK[A:B]±, REF[A:B]±						
Input Differential Voltage	V_{DIFF}	—	—	400	V_{DD}	mV
Lowest Input Low Voltage	V_{ILLP}	—	—	GND	V_{DD} – 0.4	V
Highest Input High Voltage	V_{IHHP}	—	—	1.0	V_{DD}	V
Common-mode Range (crossing voltage)	V_{COM}	—	—	0.8	V_{DD}	V
Operating Current						
Internal Operating Current	I_{CCI}	LCK4993V	V_{DD} = Max, f_{MAX}	—	250	mA
		LCK4994V	V_{DD} = Max, f_{MAX}[2]	—	250	mA
Output Current Dissipation/Pair[3]	I_{CCN}	LCK4993V	V_{DD} = Max, C_{LOAD} = 25 pF, R_{LOAD} = 50 Ω at V_{DD}/2, f_{MAX}	—	40	mA
		LCK4994V	V_{DD} = Max, C_{LOAD} = 25 pF, R_{LOAD} = 50 Ω at V_{DD}/2, f_{MAX}	—	50	mA
Capacitance						
Input Capacitance	C_{IN}	—	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3/2.5 V	—	5	pF

1. These inputs are normally wired to V_{DD}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{DD}). Internal termination resistors hold the unconnected inputs at V_{DD}/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.
2. I_{CCI} measurements is performed with Bank1 and FB Bank configured to run at maximum frequency (f_{NOM} = 100 MHz for LCK4993V, f_{NOM} = 200 MHz for LCK4994V), and all other clock output banks to run at half the maximum frequency. FS and OUTPUT_MODE are asserted to the high state.
3. This is dependent upon frequency and number of outputs of a bank being loaded. The value indicates maximum I_{CCN} at maximum frequency and maximum load of 25 pF terminated to 50 Ω at V_{DD}/2.

Switching Characteristics

The following switching characteristics are over the operating range for non-3-level inputs, and the following assumptions apply:

- A 25 pF maximum load capacitance is used for up to 185 MHz. At 200 MHz, the maximum load is 10 pF.
- Both outputs of the pair must be terminated, even if only one is being used.
- Each package must be properly decoupled.
- ac parameters are measured at 1.5 V, unless otherwise indicated.

Table 12. Switching Characteristics

Parameter	Symbol	Description	LCK4993/4V-2		LCK4993/4V-5		Unit
			Min	Max	Min	Max	
Clock Output Frequency	f_{OUT}	LCK4993V	—	100	—	100	MHz
		LCK4994V	—	200	—	200	MHz
Matched-Pair Skew[1, 2]	t_{SKEWPR}	—	—	200	—	200	ps
Intrabank Skew	$t_{SKEWBNK}$	—	—	200	—	250	ps
Output-Output Skew	t_{SKEW0}	Same frequency and phase, rise-to-rise and fall-to-fall.[1, 2]	—	250	—	550	ps
	t_{SKEW1}	Same frequency and phase, other banks at different frequency, rise-to-rise and fall-to-fall.[1, 2]	—	250	—	650	ps
	t_{SKEW2}	Invert to nominal of different banks, compared banks at same frequency, rising edge to falling edge aligned, other banks at same frequency.[1, 2]	—	250	—	700	ps
	t_{SKEW3}	All output configurations outside t_{SKEW1} and t_{SKEW2}.[1, 2]	—	500	—	800	ps
Complementary Outputs Skew	$t_{SKEWCPR}$	Crossing to crossing, complementary outputs of the same bank.[1, 2, 3, 4]	—	200	—	300	ps
Cycle-to-Cycle Jitter	$t_{CCJ1—3}$	Divide by 1 output frequency, FB = divide by 1, 2, 3.	—	TBD	—	TBD	ps p-p
	$t_{CCJ4—12}$	Divide by 1 output frequency, FB = divide by 4, 5, 6, 8, 10, 12.	—	TBD	—	TBD	ps p-p
Propagation Delay	t_{PD}	REF to FB rise.	–250	250	–500	500	ps
	$t_{PDDELTA}$	Difference between two devices.[4]	—	200	—	200	ps
REF Input	t_{REFpwl}	Pulse width low.[5]	2.0	—	2.0	—	ns
	t_{REFpwh}	Pulse width high.[5]	2.0	—	2.0	—	ns
Output Rise/Fall Time[6]	t_R/t_F	—	0.15	2.0	0.15	2.0	ns

1. Test load C_L = 25 pF, terminated to $V_{DD}/2$ with 50 Ω up to 185 MHz and 10 pF load to 200 MHz.
2. SKEW is defined as the time between the earliest and latest output transition among all outputs for which the same phase delay has been selected when all outputs are loaded with 25 pF and properly terminated up to 185 MHz. At 200 MHz the maximum load is 10 pF.
3. Complementary output skews are measured at complementary signal pair intersections.
4. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Rise and fall times are measured between 2.0 V and 0.8 V.

Switching Characteristics (continued)

Table 12. Switching Characteristics (continued)

Parameter	Symbol	Description	LCK4993/4V-2		LCK4993/4V-5		Unit
			Min	Max	Min	Max	
PLL Lock Time from Power-Up	t_{LOCK}	—	—	10	—	10	ms
PLL Relock Time	$t_{RELOCK1}$	From same frequency, different phase, and with stable power supply.	—	500	—	500	µs
	$t_{RELOCK2}$	From different frequency, different phase, and with stable power supply.[7]	—	1000	—	1000	µs
Output Duty Cycle Deviation from 50%[8]	t_{ODCV}	—	–1.0	1.0	–1.0	1.0	ns
Output Low Time Deviation from 50%[9]	t_{PWL}	—	—	2.0	—	2.0	ns
Output High Time Deviation from 50%[9]	t_{PWH}	—	—	1.5	—	1.5	ns
Period Deviation	t_{PDEV}	When changing from reference to reference.	—	0.025	—	0.025	UI[10]
Output Disable Time	t_{OZA}	DIS[1:4]/FBDIS low to output ACTIVE from output is high-impedance.[11, 12]	0.5	14	0.5	14	ns
Output Enable Time	t_{OAZ}	DIS[1:4]/FBDIS high to output high-impedance from ACTIVE.[1, 11]	1.0	10	1.0	10	ns

1. Test load C_L = 25 pF, terminated to $V_{DD}/2$ with 50 Ω up to 185 MHz and 10 pF load to 200 MHz.
2. SKEW is defined as the time between the earliest and latest output transition among all outputs for which the same phase delay has been selected when all outputs are loaded with 25 pF and properly terminated up to 185 MHz. At 200 MHz the maximum load is 10 pF.
3. Complementary output skews are measured at complementary signal pair intersections.
4. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Rise and fall times are measured between 2.0 V and 0.8 V.
7. f_{NOM} must be within the frequency range defined by the same FS state.
8. ac parameters are measured at 1.5 V, unless otherwise indicated.
9. t_{PWL} is measured at 0.8 V. t_{PWH} is measured at 2.0 V.
10. UI = unit interval. Examples: 1 UI is a full period. 0.1 UI is 10% of a period.
11. Measured at 0.5 V deviation from starting voltage.
12. For t_{OZA} minimum, C_L = 0 pF. For t_{OZA} maximum, C_L = 25 pF to 185 MHz or 10 pF to 200 MHz.

ac Test Loads and Waveform

Note: Figure 4 and Figure 5 are for illustrations only. The actual ATE loads may vary.

For LOCK output only:	For all other outputs:
R1 = 910 Ω	R1 = 100 Ω
R2 = 910 Ω	R2 = 100 Ω
C_L < 30 pF	C_L < 25 pF to 185 MHz or 10 pF at 200 MHz
(Includes fixture and probe capacitance)	

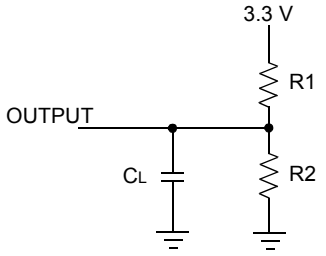


Figure 4. LVTTL ac Test Load

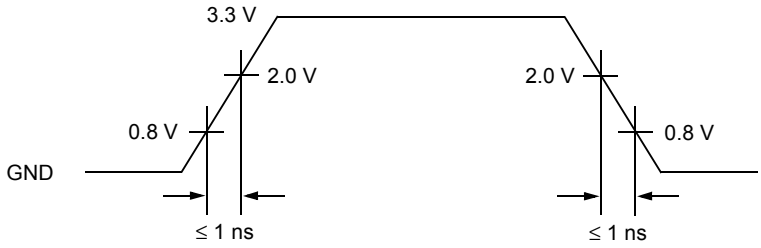


Figure 5. TTL Input Test Waveform

ac Timing Diagrams

ac parameters are measured at 1.5 V, unless otherwise indicated.

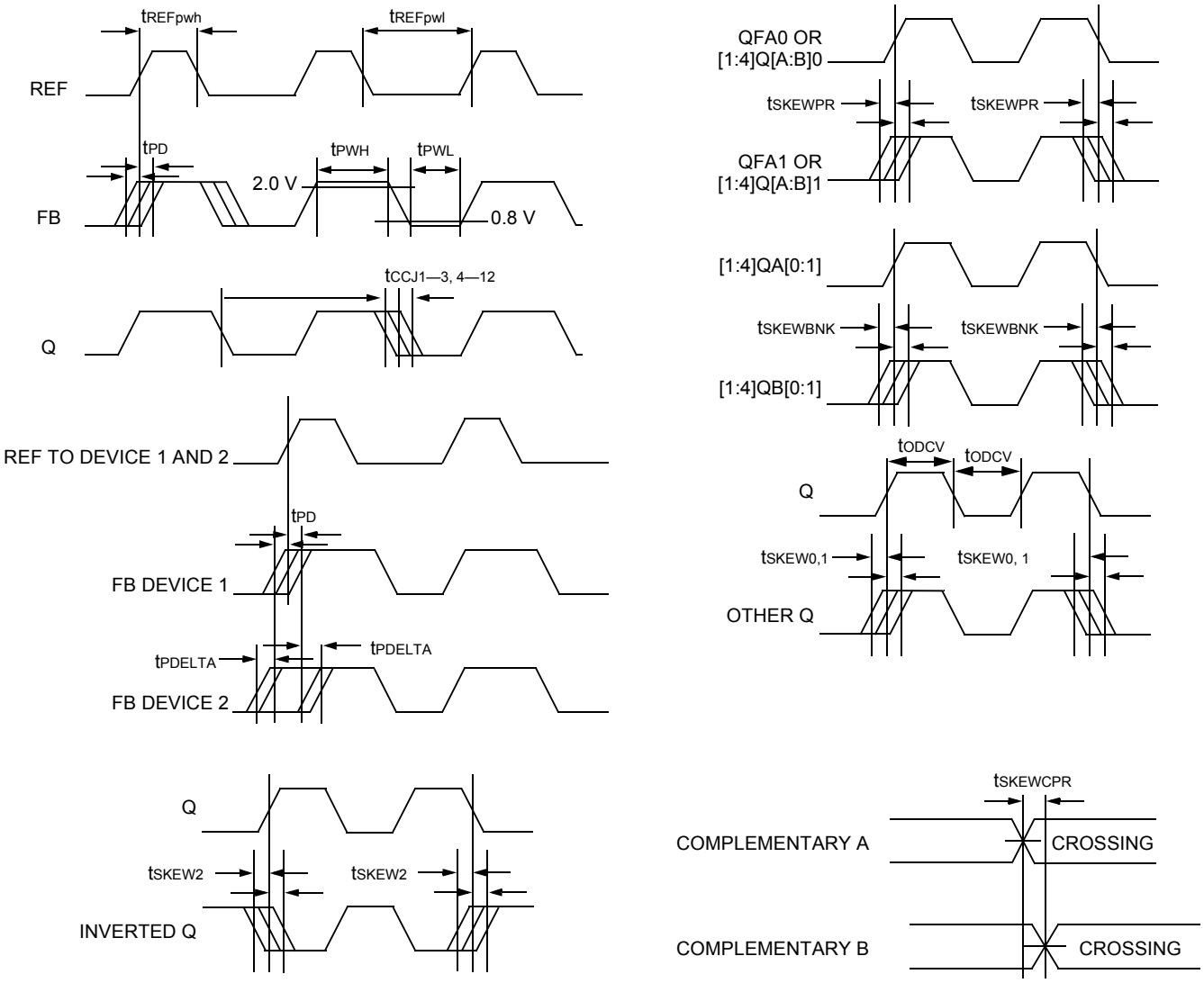
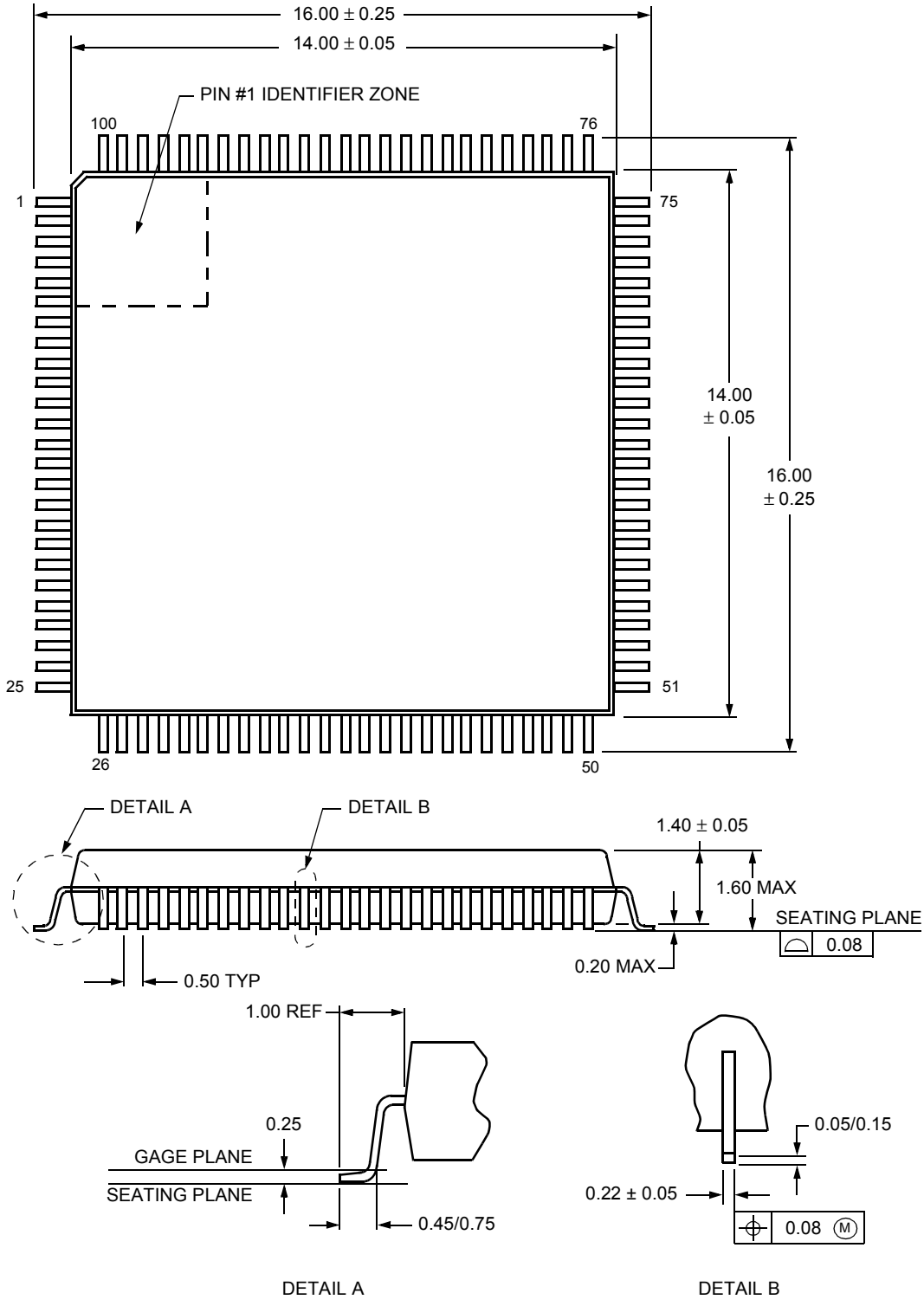


Figure 6. ac Timing Diagrams

Outline Diagrams

100-Pin TQFP

Controlling dimensions are in millimeters.

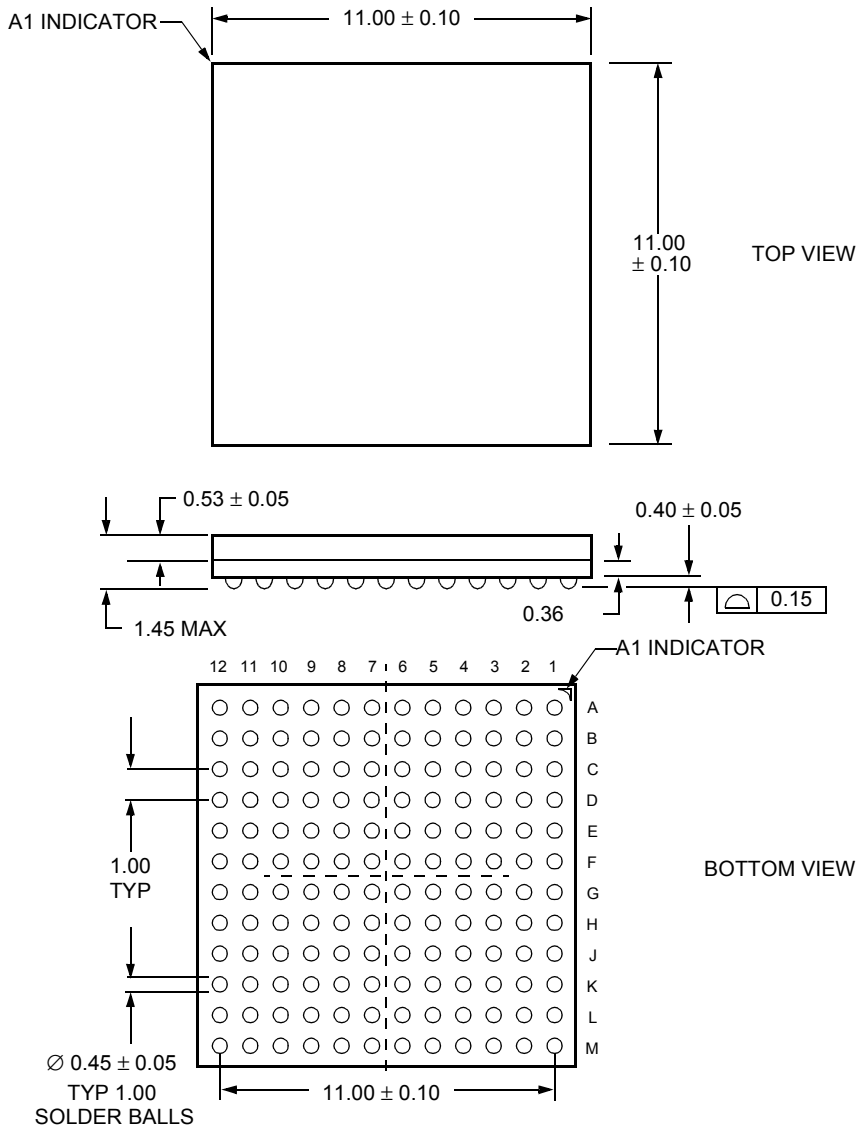


5-2146 (F) r.1

Outline Diagrams (continued)

100-Ball FSBGA

Controlling dimensions are in millimeters.



5-8159.a (F) r.1

Note: The ball diameter, ball pitch, and stand-off and package thicknesses are different from JEDEC spec M0192 (low-profile BGA family).

Ordering Information

Device	Type	Comcode
LCK4993V	FSBGA	TBD
LCK4994V	FSBGA	TBD
LCK4993V	TQFP	TBD
LCK4994V	TQFP	TBD

CYPRESS is a registered trademark of Cypress Semiconductor Corporation.

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@agere.com**
N. AMERICA: Agere Systems Inc., Lehigh Valley Central Campus, Room 10A-301C, 1110 American Parkway NE, Allentown, PA 18109-9138
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA: Agere Systems Hong Kong Ltd., Suites 3201 & 3210-12, 32/F, Tower 2, The Gateway, Harbour City, Kowloon
Tel. (852) 3129-2000, FAX (852) 3129-2020
CHINA: **(86) 21-5047-1212** (Shanghai), **(86) 755-25881122** (Shenzhen)
JAPAN: **(81) 3-5421-1600** (Tokyo), KOREA: **(82) 2-767-1850** (Seoul), SINGAPORE: **(65) 778-8833**, TAIWAN: **(886) 2-2725-5858** (Taipei)
EUROPE: **Tel. (44) 1344 296 400**

November 2002
DS02-346LCK