FAIRCHILD
A Schlumberger Company

F100151
Hex D Flip-Flop

F100K ECL Product

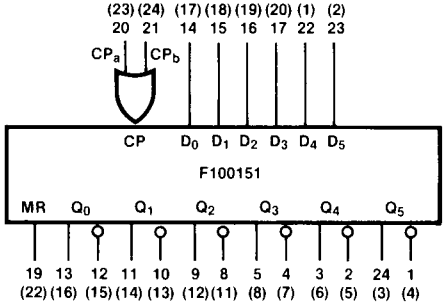
Description

The F100151 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of Common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50K Ω pull-down resistors.

Pin Names

D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

Logic Symbol



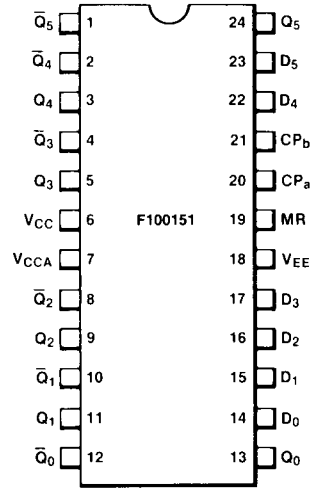
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information

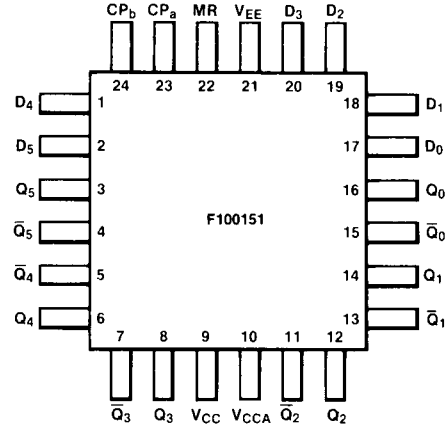
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

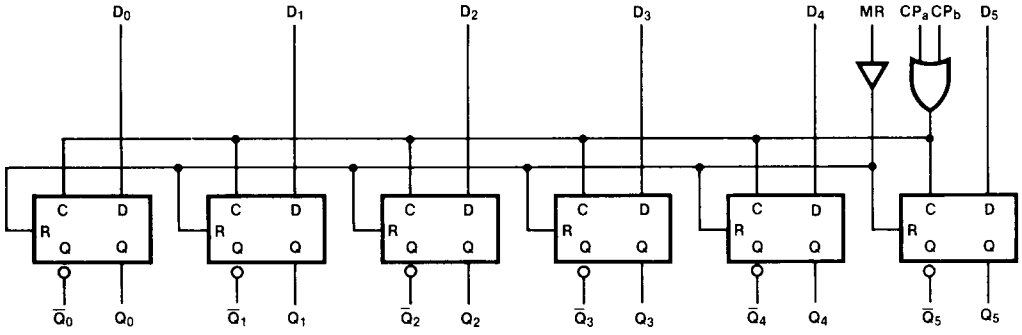
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Tables (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	⌐	L	L	L
H	⌐	L	L	H
L	L	⌐	L	L
H	L	⌐	L	H
X	H	⌐	L	$Q_n(t)$
X	⌐	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before CP positive transition
t+1 = Time after CP positive transition
⌐ = LOW-to-HIGH transition

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current MR D_0-D_5 CP_a, CP_b			 450 225 520	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−210	−155	−98	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.20	0.80	2.20	0.90	2.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.90	1.30	3.00	1.20	3.10	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time D_0-D_5 MR (Release Time)	 0.70 2.30		 0.70 2.30		 0.70 2.60		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0-D_5	0.70		0.70		0.70		ns	*Figure 5*
t_{pw}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

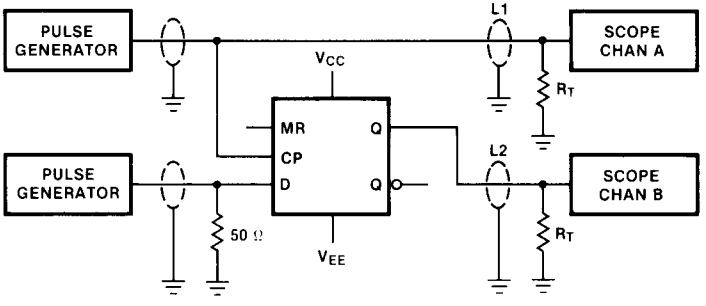
*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.00	0.90	2.20	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.70	1.30	2.80	1.20	2.90	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_0-D_5 MR (Release Time)	0.60 2.20		0.60 2.20		0.60 2.50		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0-D_5	0.60		0.60		0.60		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

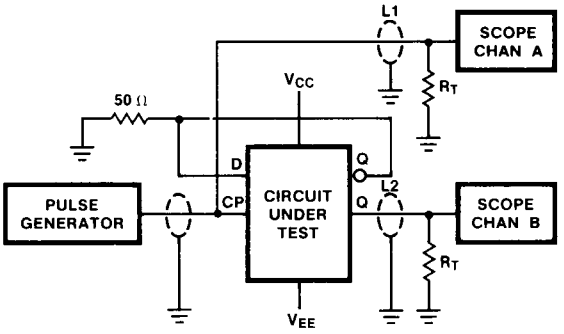
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Toggle Frequency Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

Fig. 3 Propagation Delay (Clock) and Transition Times

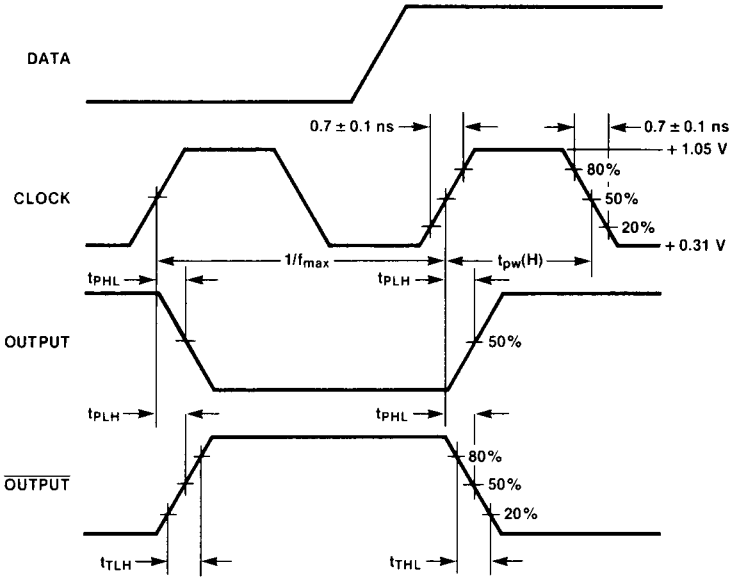


Fig. 4 Propagation Delay (Reset)

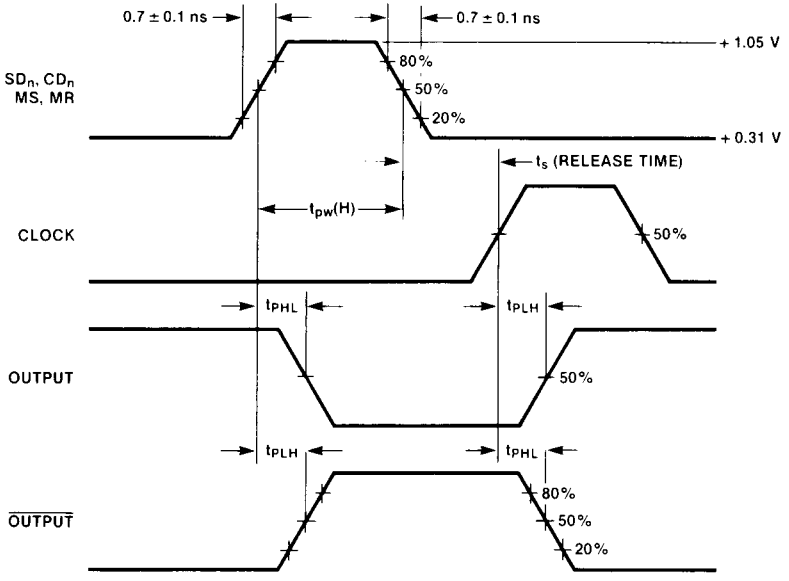
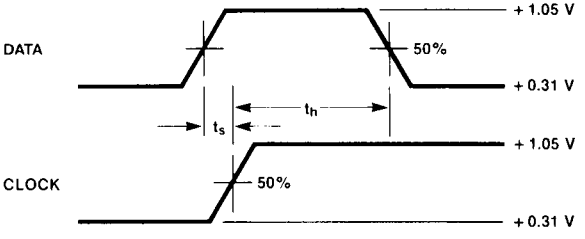


Fig. 5 Setup and Hold Time



Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input