



# *High Speed Super Low Power SRAM*

32K Word x 8 Bit

**CS18LV02563**

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## Revision History

| <u>Rev. No.</u> | <u>History</u>                     | <u>Issue Date</u> | <u>Remark</u> |
|-----------------|------------------------------------|-------------------|---------------|
| 2.0             | Initial issue with new naming rule | Dec.27,2004       |               |



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32K Word x 8 Bit

**CS18LV02563**

## ■ GENERAL DESCRIPTION

The CS18LV02563 is a high performance, high speed and super low power CMOS Static Random Access Memory organized as 32,768 words by 8bits and operates from a wide range of 1.8 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE).

The CS18LV02563 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV02563 is available in JEDEC standard 28-pin TSOP I (8x13.4 mm), SOP (330 mil) and PDIP (600 mil) packages.

## ■ FEATURES

- Wide operation voltage : 1.8 ~ 3.6V
- Ultra low power consumption : 2mA@1MHz (Max.) , Vcc=3.0V.  
0.10 uA (Typ.) CMOS standby current
- High speed access time : 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.

## ■ PRODUCT FAMILY

| Product Family | Operating Temp. | Vcc Range | Speed (ns) | Standby Current(Typ.)<br>I <sub>CCSB1</sub> | Package Type |
|----------------|-----------------|-----------|------------|---|--------------|
| CS18LV02563    | 0~70°C          | 1.8~3.6V  | 55/70      | 0.10 uA<br>(Vcc = 3.0V)                     | 28 SOP       |
|                |                 |           |            |   | 28 TSOP I    |
|                |                 |           |            |   | 28 PDIP      |
|                |                 |           |            |   | Dice         |
|                | -40~85°C        |           | 55/70      | 0.15 uA<br>(Vcc= 3.0V)                      | 28 SOP       |
|                |                 |           |            |   | 28 TSOP I    |
|                |                 |           |            |   | 28 PDIP      |
|                |                 |           |            |   | Dice         |

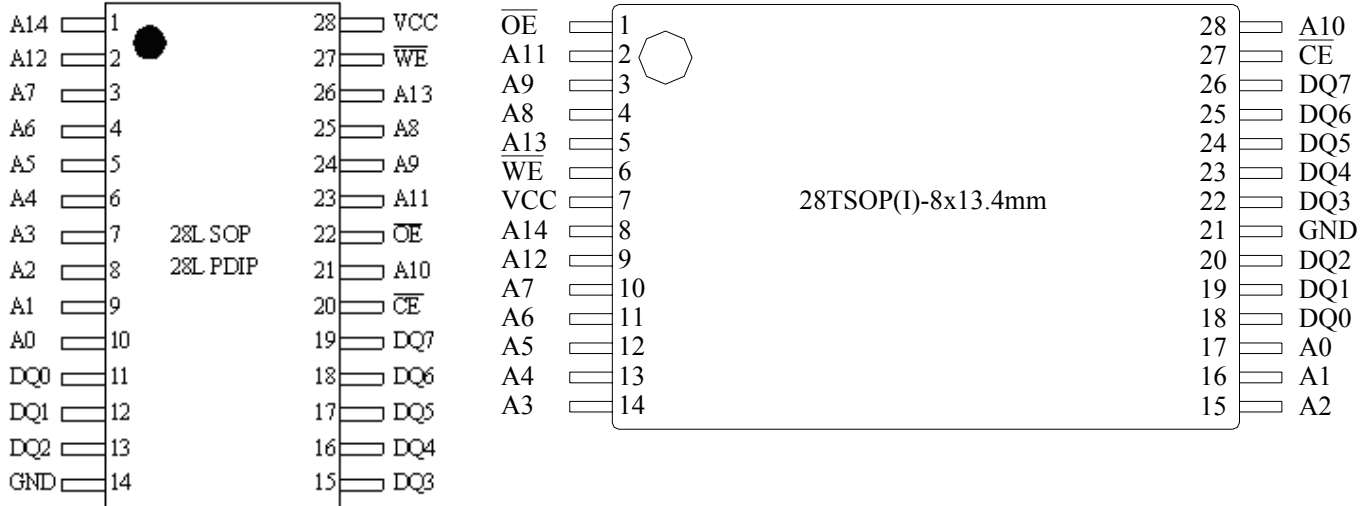


# High Speed Super Low Power SRAM

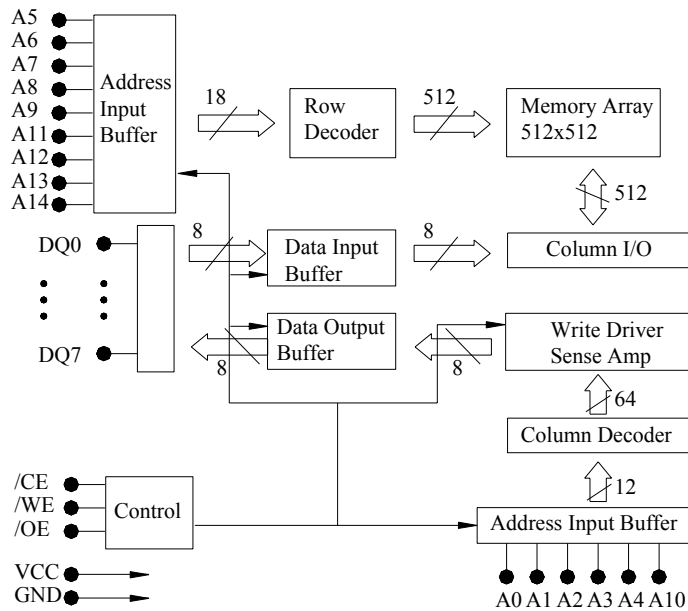
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## PIN CONFIGURATIONS



## FUNCTIONAL BLOCK DIAGRAM





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## ■ PIN DESCRIPTIONS

| Name     | Type  | Function  |
|----------|-------|---|
| A0 – A14 | Input | Address inputs for selecting one of the 32,768 x 8 bit words in the RAM   |
| /CE      | Input | /CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.                              |
| /WE      | Input | The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location. |
| /OE      | Input | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.                |
| DQ0~DQ7  | I/O   | These 8 bi-directional ports are used to read data from or write data into the RAM.   |
| Vcc      | Power | Power Supply  |
| Gnd      | Power | Ground  |

## ■ TRUTH TABLE

| Mode            | /CE | /WE | /OE | DQ0~7            | Vcc Current                            |
|-----------------|-----|-----|-----|------------------|--|
| Standby         | H   | X   | X   | High Z           | I <sub>CCSB</sub> , I <sub>CCSB1</sub> |
| Output Disabled | L   | H   | H   | High Z           | I <sub>CC</sub>                        |
| Read            | L   | H   | L   | D <sub>OUT</sub> | I <sub>CC</sub>                        |
| Write           | L   | L   | X   | D <sub>IN</sub>  | I <sub>CC</sub>                        |



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## ■ ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol            | Parameter                            | Rating                       | Unit |
|-------------------|--------------------------------------|------------------------------|------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | -0.5 to V <sub>CC</sub> +0.5 | V    |
| T <sub>BIAS</sub> | Temperature Under Bias               | -40 to +125                  | °C   |
| T <sub>STG</sub>  | Storage Temperature                  | -60 to +150                  | °C   |
| P <sub>T</sub>    | Power Dissipation                    | 1.0                          | W    |
| I <sub>OUT</sub>  | DC Output Current                    | 20                           | mA   |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ■ OPERATING RANGE

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Commercial | 0~70°C              | 1.8 ~3.6V       |
| Industrial | -40~85°C            | 1.8 ~ 3.6V      |

## ■ CAPACITANCE<sup>(1)</sup>(T<sub>A</sub>=25°C, f=1.0MHz)

| Symbol          | Parameter                | Conduction           | MAX. | Unit |
|-----------------|--------------------------|----------------------|------|------|
| C <sub>IN</sub> | Input Capacitance        | V <sub>IN</sub> =0V  | 6    | pF   |
| C <sub>DQ</sub> | Input/Output Capacitance | V <sub>I/O</sub> =0V | 8    | pF   |

1. This parameter is guaranteed, and not 100% tested.



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## ■ DC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, VCC = 3.0V)

| Name               | Parameter                                    | Test Condition  | MIN  | TYP <sup>(1)</sup> | MAX                  | Unit |
|--------------------|--|---|------|--------------------|----------------------|------|
| V <sub>IL</sub>    | Guaranteed Input Low Voltage <sup>(2)</sup>  | V <sub>CC</sub> =1.8V   | -0.5 |                    | 0.8                  | V    |
| V <sub>IH</sub>    | Guaranteed Input High Voltage <sup>(2)</sup> | V <sub>CC</sub> =3.6V   | 2.0  |                    | V <sub>CC</sub> +0.2 | V    |
| I <sub>IL</sub>    | Input Leakage Current                        | V <sub>CC</sub> =MAX, V <sub>IN</sub> =0 to V <sub>CC</sub>   | -1   |                    | 1                    | uA   |
| I <sub>OL</sub>    | Output Leakage Current                       | V <sub>CC</sub> =MAX, /CE=V <sub>IN</sub> , or /OE=V <sub>IN</sub> , V <sub>IO</sub> =0V to V <sub>CC</sub> | -1   |                    | 1                    | uA   |
| V <sub>OL</sub>    | Output Low Voltage                           | V <sub>CC</sub> =MAX, I <sub>OL</sub> = 1mA   |      |                    | 0.4                  | V    |
| V <sub>OH</sub>    | Output High Voltage                          | V <sub>CC</sub> =MIN, I <sub>OH</sub> = -1mA  | 2.2  |                    |                      | V    |
| I <sub>CC</sub>    | Operating Power Supply Current               | /CE=V <sub>IL</sub> , I <sub>DQ</sub> =0mA, F=F <sub>MAX</sub> = 1/ t <sub>RC</sub>                         |      |                    | 20                   | mA   |
| I <sub>CCSB</sub>  | TTL Standby Supply                           | /CE=V <sub>IH</sub> , I <sub>DQ</sub> =0mA,   |      |                    | 1                    | mA   |
| I <sub>CCSB1</sub> | CMOS Standby Current                         | /CE ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V,             |      | 0.1                | 3                    | uA   |

1. Typical characteristics are at TA = 25°C.

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

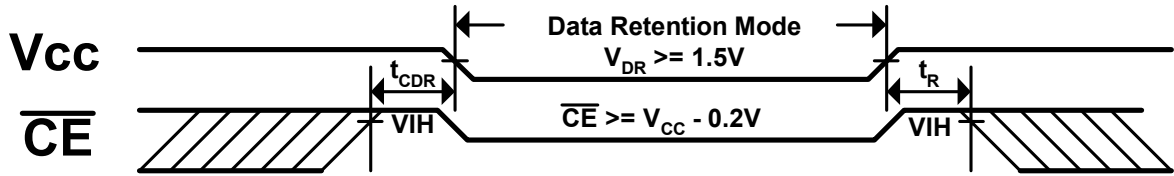
## ■ DATA RETENTION CHARACTERISTICS (TA = 0° ~70°C)

| Name              | Parameter                            | Test Condition  | MIN                 | TYP <sup>(1)</sup> | MAX | Unit |
|-------------------|--------------------------------------|---|---------------------|--------------------|-----|------|
| V <sub>DR</sub>   | V <sub>CC</sub> for Data Retention   | /CE ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V                          | 1.5                 |                    |     | V    |
| I <sub>CCDR</sub> | Data Retention Current               | /CE ≥ V <sub>CC</sub> -0.2V, V <sub>CC</sub> =1.5V<br>V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V |                     | 0.1                | 2   | uA   |
| T <sub>CDR</sub>  | Chip Deselect to Data Retention Time | Refer to Retention Waveform   | 0                   |                    |     | ns   |
| t <sub>R</sub>    | Operation Recovery Time              |   | t <sub>RC</sub> (2) |                    |     | ns   |

1. TA = 25°C.

2. t<sub>RC</sub> = Read Cycle Time.

■ **LOW V<sub>CC</sub> DATA RETENTION WAVEFORM ( /CE Controlled )**



■ **AC TEST CONDITIONS**

|                           |                     |
|---------------------------|---------------------|
| Input Pulse Levels        | V <sub>CC</sub> /0V |
| Input Rise and Fall Times | 5ns                 |
| Input and Output Timing   | 0.5V <sub>CC</sub>  |
| Reference Level           |                     |

■ **KEY TO SWITCHING WAVEFORMS**

| WAVEFORMS | INPUTS                          | OUTPUTS                                 |
|-----------|---------------------------------|---|
|           | MUST BE STEADY                  | MUST BE STEADY                          |
|           | MAY CHANGE FROM H TO L          | WILL BE CHANGE FROM H TO L              |
|           | MAY CHANGE FROM L TO H          | WILL BE CHANGE FROM L TO H              |
|           | DON'T CARE ANY CHANGE PERMITTED | CHANGE STATE UNKNOWN                    |
|           | DOES NOT APPLY                  | CENTER LINE IS HIGH IMPEDANCE OFF STATE |

■ **AC TEST LOADS AND WAVEFORMS**

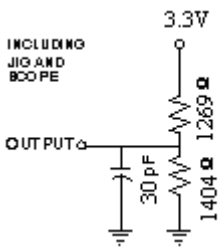


FIGURE 1A

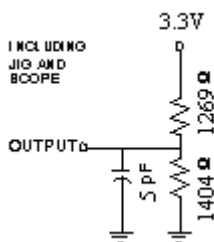


FIGURE 1B

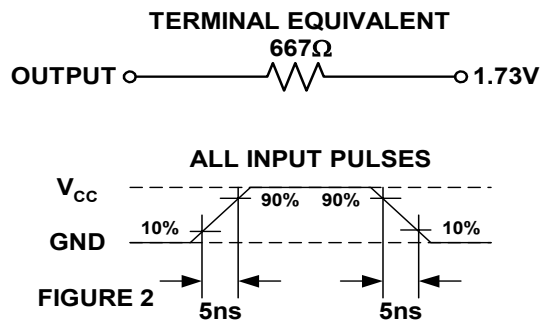


FIGURE 2



# High Speed Super Low Power SRAM

32K Word x 8 Bit

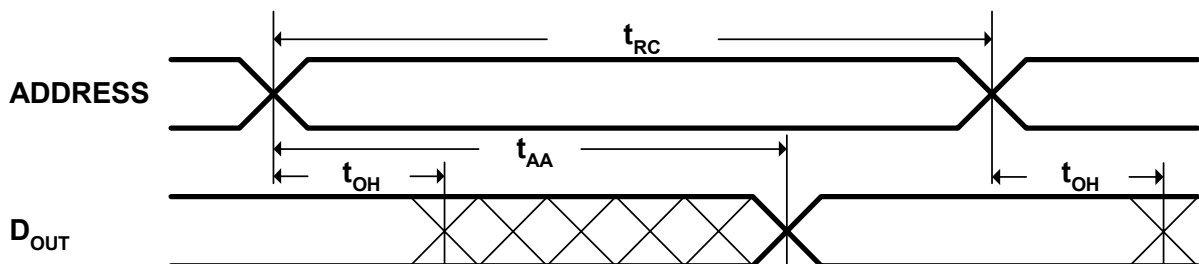
CS18LV02563

■ **AC ELECTRICAL CHARACTERISTICS** (  $T_A = 0^\circ \sim 70^\circ\text{C}$ ,  $V_{CC} = 3.0\text{V}$  )  
**< READ CYCLE >**

| JEDEC Name | Symbol    | Description                        | -55 |     | -70 |     | Unit |
|------------|-----------|------------------------------------|-----|-----|-----|-----|------|
|            |           |                                    | MIN | MAX | MIN | MAX |      |
| $t_{AVAX}$ | $t_{RC}$  | Read Cycle Time                    | 55  |     | 70  |     | ns   |
| $t_{AVQV}$ | $t_{AA}$  | Address Access Time                |     | 55  |     | 70  | ns   |
| $t_{ELQV}$ | $t_{ACE}$ | Chip Select Access Time            |     | 55  |     | 70  | ns   |
| $t_{GLQV}$ | $t_{OE}$  | Output Enable to Output Valid      |     | 30  |     | 50  | ns   |
| $t_{ELQX}$ | $t_{CLZ}$ | Chip Select to Output Low Z        | 10  |     | 10  |     | ns   |
| $t_{GLQX}$ | $t_{OLZ}$ | Output Enable to Output in Low Z   | 5   |     | 5   |     | ns   |
| $t_{EHQZ}$ | $t_{CHZ}$ | Chip Deselect to Output in High Z  | 0   | 35  | 0   | 35  | ns   |
| $t_{GHQZ}$ | $t_{OHZ}$ | Output Disable to Output in High Z | 0   | 30  | 0   | 30  | ns   |
| $t_{AXOX}$ | $t_{OH}$  | Address Change to Out Disable      | 10  |     | 10  |     | ns   |

■ **SWITCHING WAVEFORMS (READ CYCLE)**

**READ CYCLE1** <sup>(1,2,4)</sup>

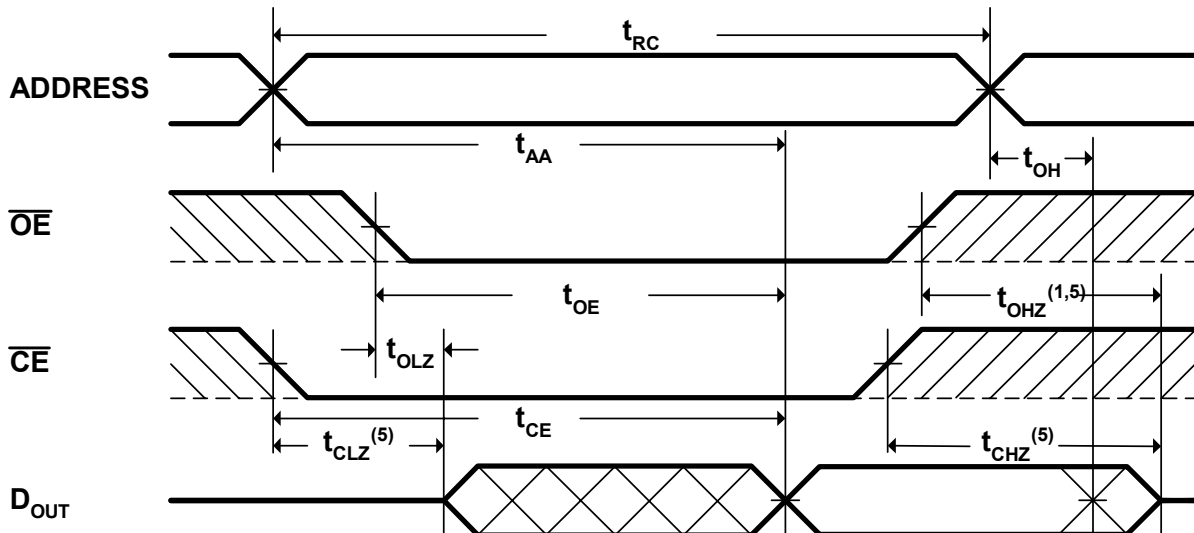




**READ CYCLE2** <sup>(1,3,4)</sup>



**READ CYCLE3** <sup>(1,4)</sup>



**NOTES:**

1. /WE is high in read Cycle.
2. Device is continuously selected when /CE =  $V_{IL}$ .
3. Address valid prior to or coincident with CE transition low.
4. /OE =  $V_{IL}$ .
5. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5VCC, input pulse levels of 0V to VCC and output loading specified in Figure 1A.
6. Transition is measured  $\pm 500mV$  from steady state with  $C_L = 5pF$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.



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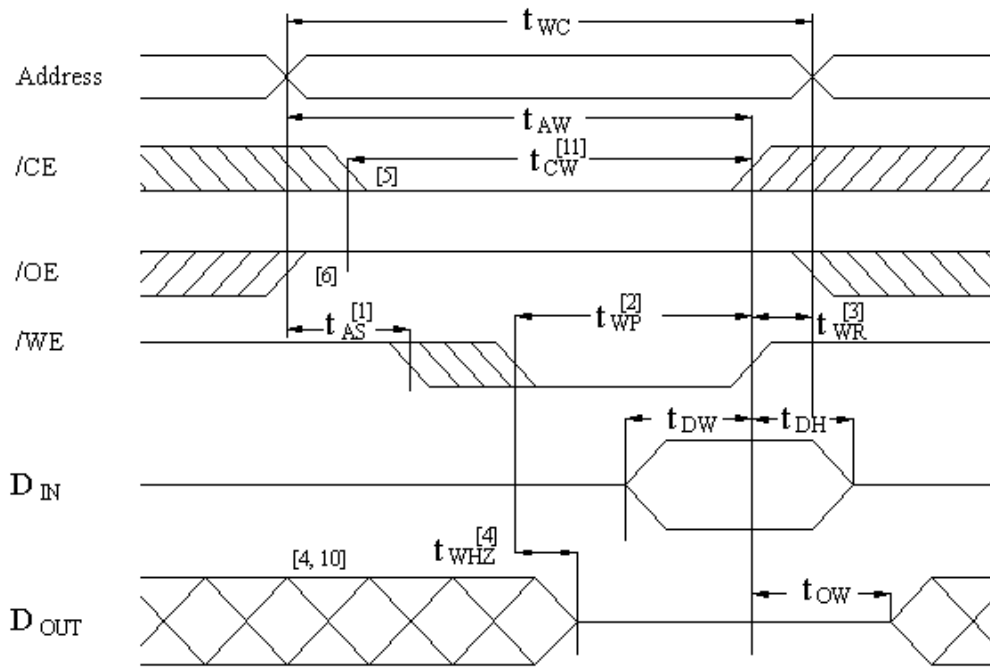
## ■ AC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 3.0V)

### < WRITE CYCLE >

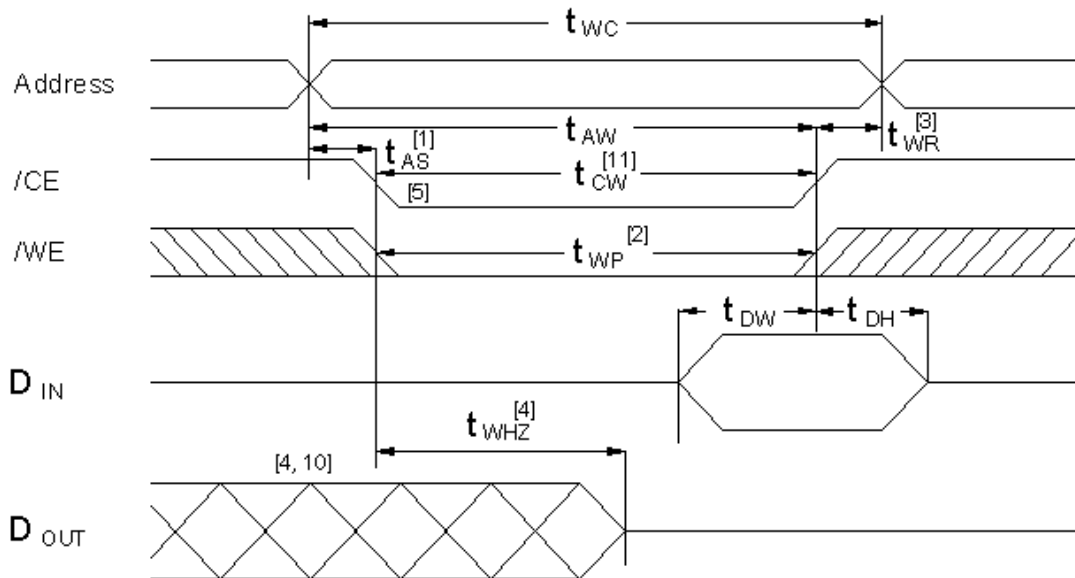
| JEDEC Name | Symbol | Description                        | -55 |     | -70 |     | Unit |
|------------|--------|------------------------------------|-----|-----|-----|-----|------|
|            |        |                                    | MIN | MAX | MIN | MAX |      |
| tAVAX      | tWC    | Write Cycle Time                   | 55  |     | 70  |     | ns   |
| tE1LWH     | tCW    | Chip Select to End of Write        | 55  |     | 70  |     | ns   |
| tAVWL      | tAS    | Address Setup Time                 | 0   |     | 0   |     | ns   |
| tAVWH      | tAW    | Address Valid to End of Write      | 55  |     | 70  |     | ns   |
| tWLWH      | tWP    | Write Pulse Width                  | 40  |     | 50  |     | ns   |
| tWHAX      | tWR    | Write Recovery Time                | 0   |     | 0   |     | ns   |
| tWLQZ      | tWHZ   | Write to Output in High Z          |     | 25  |     | 35  | ns   |
| tDVWH      | tDW    | Data to Write Time Overlap         | 20  |     | 30  |     | ns   |
| tWHDX      | tDH    | Data Hold for Write End            | 0   |     | 0   |     | ns   |
| tGHQZ      | tOHZ   | Output Disable to Output in High Z | 0   | 30  | 0   | 30  | ns   |
| tWHOX      | tOW    | End of Write to Output Active      | 5   |     | 5   |     | ns   |

## SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



WRITE CYCLE2 (Chip Enable Controlled)





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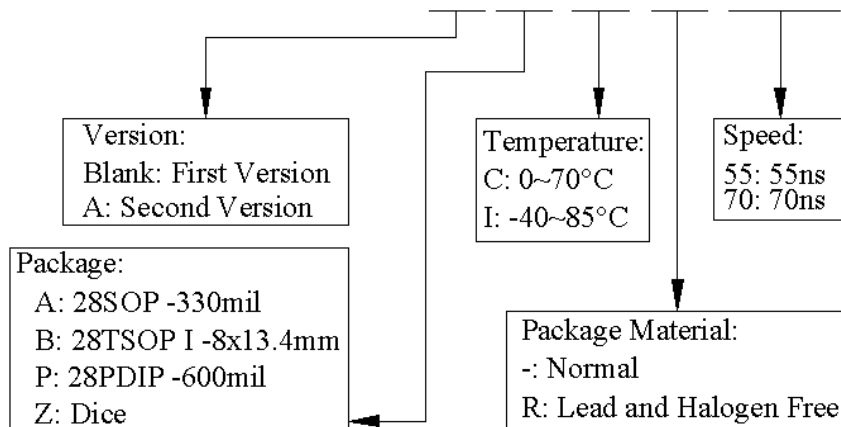
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## NOTES:

1. /WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3.  $T_{WR}$  is measured from the earlier of /CE or /WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.
6. /OE is continuously low ( $/OE = V_{IL}$ ).  $D_{OUT}$  is the same phase of write data of this write cycle.
7.  $D_{OUT}$  is the read data of next address.
8. If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5VCC, input pulse levels of 0V to VCC and output loading specified in Figure 1A.
10. Transition is measured  $\pm 500mV$  from steady state with  $C_L = 5pF$  as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11.  $T_{CW}$  is measured from the later of /CE going low to the end of write.

## ■ ORDER INFORMATION

CS18LV02563 X X X X XX



Note: Package material code "R" meets ROHS

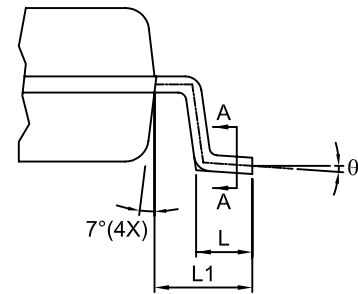
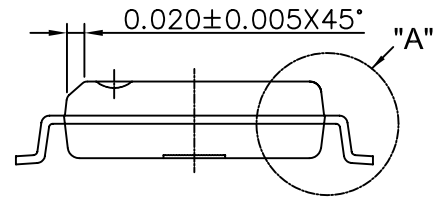
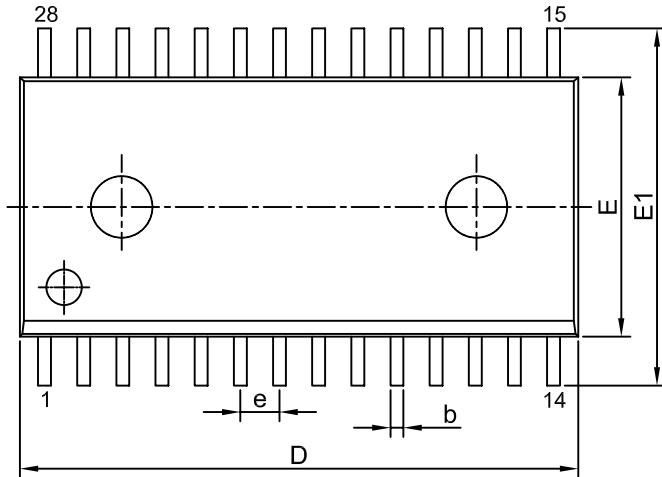


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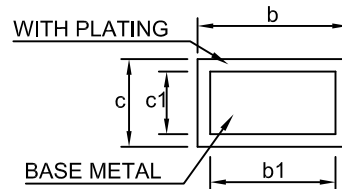
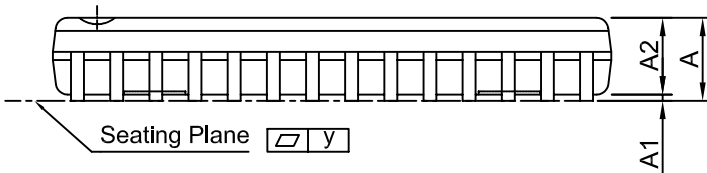
32k Word x 8 bit

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## PACKAGE DIMENSIONS - 28L SOP 330 mil



DETAIL "A" (2:1)



SECTION A-A

| SYMBOL |      | A     | A1    | A2    | b     | b1    | c     | c1    | D      | E     | E1     | e     | L      | L1     | y     | $\theta$ |
|--------|------|-------|-------|-------|-------|-------|-------|-------|--------|-------|--------|-------|--------|--------|-------|----------|
| UNIT   |      |       |       |       |       |       |       |       |        |       |        |       |        |        |       |          |
| mm     | Min. | 2.540 | 0.102 | 2.362 | 0.35  | 0.35  | 0.20  | 0.20  | 17.983 | 8.280 | 11.506 | 1.118 | 0.700  | 1.520  | -     | 0°       |
|        | Nom. | 2.692 | 0.226 | 2.489 | -     | -     | -     | -     | 18.110 | 8.407 | 11.811 | 1.270 | 0.964  | 1.720  | -     | -        |
|        | Max. | 2.844 | 0.350 | 2.616 | 0.50  | 0.45  | 0.32  | 0.28  | 18.237 | 8.534 | 12.116 | 1.422 | 1.228  | 1.920  | 0.1   | 10°      |
| inch   | Min. | 0.100 | 0.004 | 0.093 | 0.014 | 0.014 | 0.008 | 0.008 | 0.708  | 0.326 | 0.453  | 0.044 | 0.0276 | 0.0598 | -     | 0°       |
|        | Nom. | 0.106 | 0.009 | 0.098 | -     | -     | -     | -     | 0.713  | 0.331 | 0.465  | 0.050 | 0.0380 | 0.0677 | -     | -        |
|        | Max. | 0.112 | 0.014 | 0.103 | 0.020 | 0.018 | 0.012 | 0.011 | 0.718  | 0.336 | 0.477  | 0.056 | 0.0484 | 0.0756 | 0.004 | 10°      |

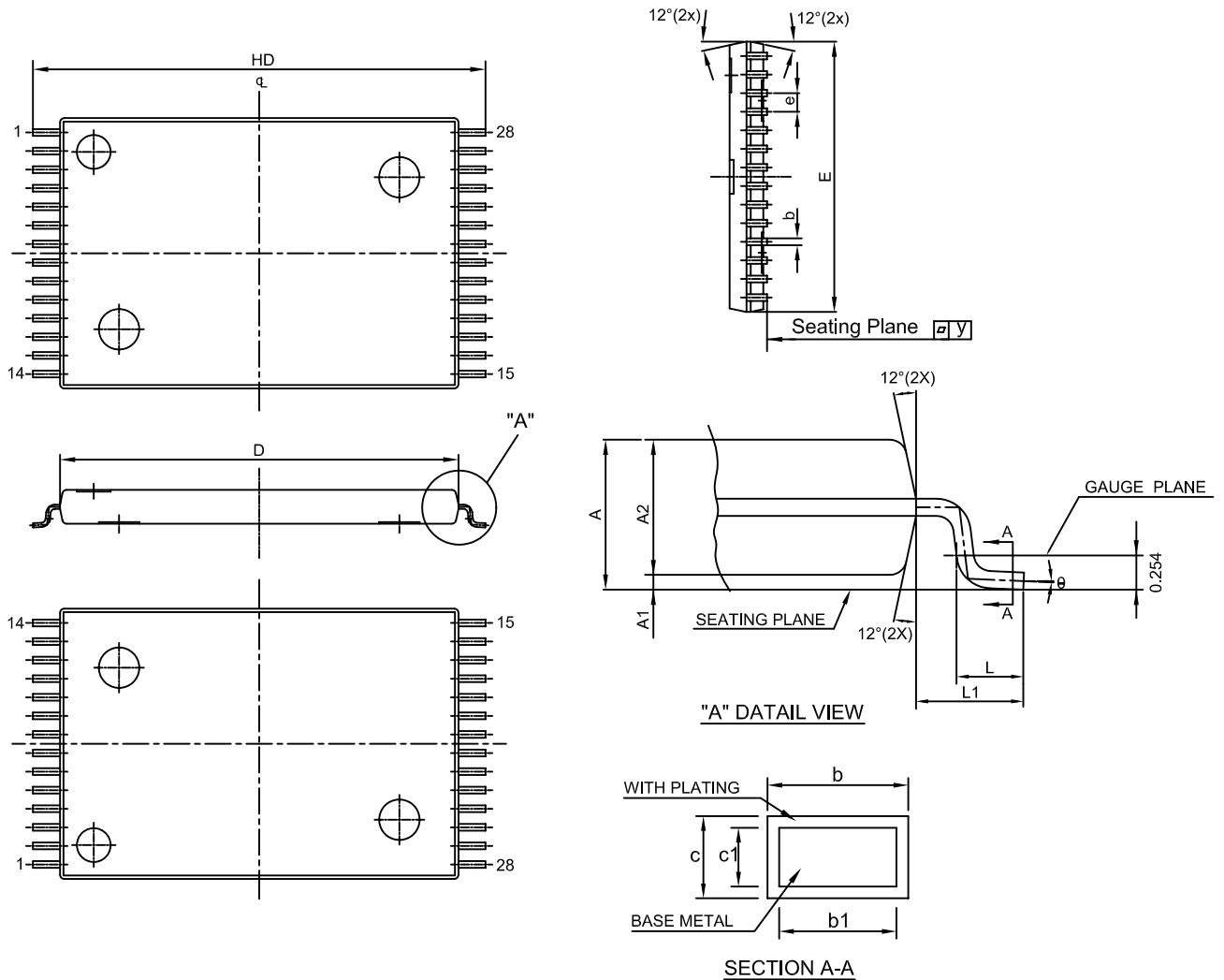


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## PACKAGE DIMENSIONS - 28L TSOP 1- 8x13.24mm



| SYMBOL<br>UNIT | A   | A1                                  | A2                      | b                       | b1                      | c                    | c1                  | D                       | E                       | e                       | HD                      | L                          | L1                         | y                    | θ             |
|----------------|---|-------------------------------------|-------------------------|-------------------------|-------------------------|----------------------|---------------------|-------------------------|-------------------------|-------------------------|-------------------------|----------------------------|----------------------------|----------------------|---------------|
|                | mm  | Min. 1.00<br>Nom. 1.10<br>Max. 1.20 | 0.050<br>0.115<br>0.180 | 0.95<br>1.00<br>1.05    | 0.17<br>0.22<br>0.27    | 0.17<br>0.20<br>0.23 | 0.10<br>—<br>0.21   | 0.10<br>—<br>0.16       | 11.70<br>11.80<br>11.90 | 7.90<br>8.00<br>8.10    | 0.45<br>0.55<br>0.65    | 13.20<br>13.40<br>13.60    | 0.40<br>0.50<br>0.70       | 0.70<br>0.80<br>0.90 | —<br>—<br>0.1 |
| inch           | Min. 0.0393<br>Nom. 0.0433<br>Max. 0.0473 | 0.0019<br>0.0045<br>0.0071          | 0.037<br>0.039<br>0.041 | 0.007<br>0.009<br>0.011 | 0.007<br>0.008<br>0.009 | 0.004<br>—<br>0.008  | 0.004<br>—<br>0.006 | 0.461<br>0.465<br>0.469 | 0.311<br>0.315<br>0.319 | 0.018<br>0.022<br>0.026 | 0.520<br>0.528<br>0.536 | 0.0157<br>0.0197<br>0.0277 | 0.0275<br>0.0315<br>0.0355 | —<br>—<br>0.004      | 0°<br>—<br>8° |

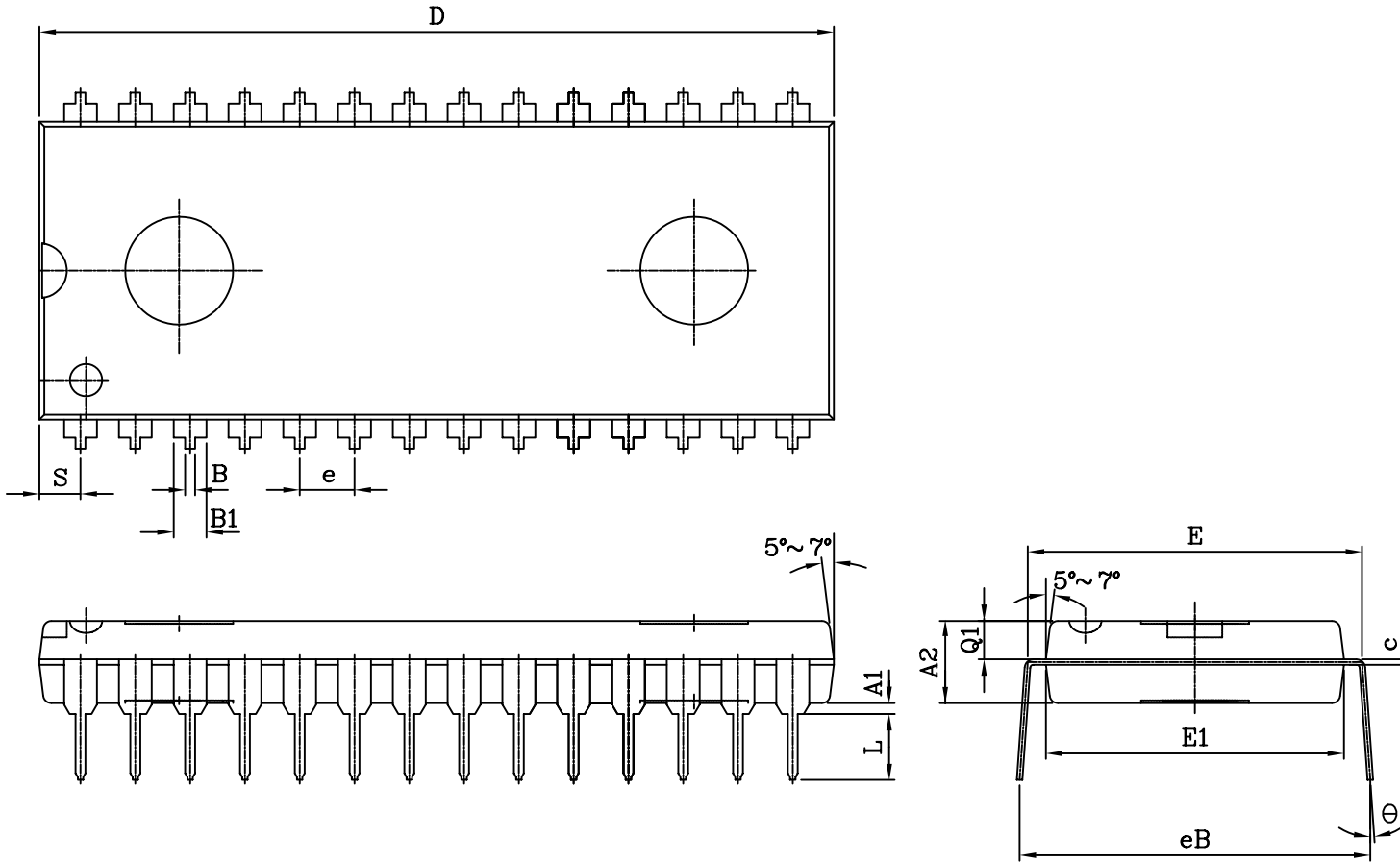


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## PACKAGE DIMENSIONS - 28L PDIP -600mil



| SYMBOL |      | A1    | A2    | B     | B1    | c     | D      | E      | E1     | e              | eB     | L     | S     | Q1    | θ  |
|--------|------|-------|-------|-------|-------|-------|--------|--------|--------|----------------|--------|-------|-------|-------|----|
| UNIT   |      |       |       |       |       |       |        |        |        |                |        |       |       |       |    |
| mm     | Min. | 0.254 | 3.683 | 0.330 | 1.270 | 0.152 | 36.957 | 14.986 | 13.716 | 2,540<br>(TYP) | 15.748 | 3.048 | 1.778 | 1.651 | 3° |
|        | Nom. | —     | 3.810 | 0.457 | 1.524 | 0.254 | 37.084 | 15.240 | 13.818 |                | 16.256 | 3.302 | 2.032 | 1.778 | 6° |
|        | Max. | —     | 3.937 | 0.584 | 1.778 | 0.356 | 37.211 | 15.494 | 13.920 |                | 16.764 | 3.556 | 2.286 | 1.905 | 9° |
| inch   | Min. | 0.010 | 0.145 | 0.013 | 0.050 | 0.006 | 1.455  | 0.590  | 0.540  | 0,100<br>(TYP) | 0.620  | 0.120 | 0.070 | 0.065 | 3° |
|        | Nom. | —     | 0.150 | 0.018 | 0.060 | 0.010 | 1.460  | 0.600  | 0.544  |                | 0.640  | 0.130 | 0.080 | 0.070 | 6° |
|        | Max. | —     | 0.155 | 0.023 | 0.070 | 0.014 | 1.465  | 0.610  | 0.548  |                | 0.660  | 0.140 | 0.090 | 0.075 | 9° |