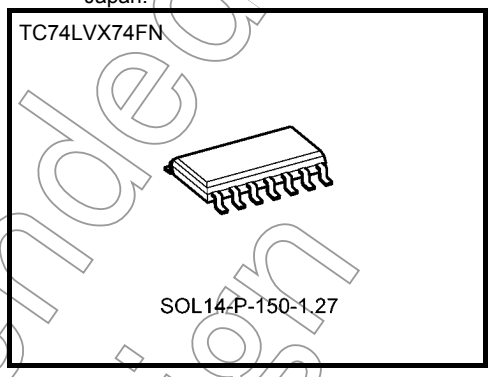
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVX74FN

Dual D-Type Flip-Flop with Preset and Clear

Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight
SOL14-P-150-1.27 : 0.12 g (typ.)

The TC74LVX74FN is a high-speed CMOS D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

The signal level applied to the D input is transferred to Q output during the positive going transition of the CK pulse.

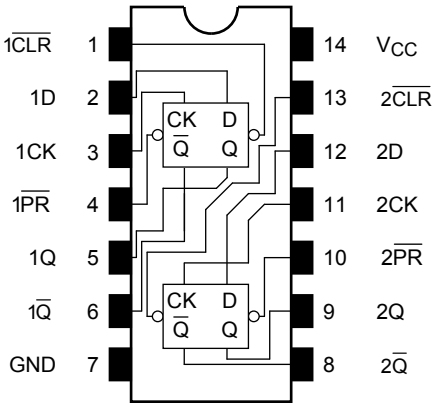
$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

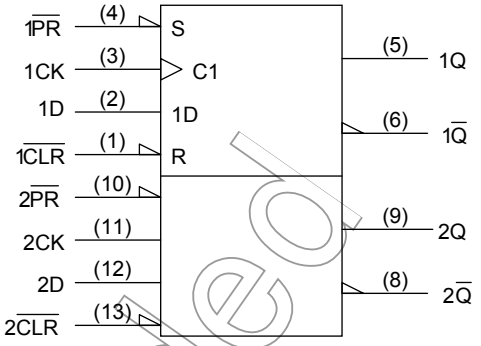
Features

- High-speed: f_{max} = 145 MHz (typ.) (V_{CC} = 3.3 V)
- Low power dissipation: I_{CC} = 2 μA (max) (Ta = 25°C)
- Input voltage level: V_{IL} = 0.8 V (max) (V_{CC} = 3 V)
  V_{IH} = 2.0 V (min) (V_{CC} = 3 V)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74HC74

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Qn	$\overline{Q}$ n	No change

X: Don't care

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Sym-bol	Test Condition		Ta = 25°C				Ta = −40 to 85°C		Unit
					V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	H-level	V_{IH}	—		2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—		2.0	—	
					3.6	2.4	—	—	2.4	—	
	L-level	V_{IL}	—		2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH} = −50 μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0	0.1	—	0.1	
				I_{OL} = 50 μA	3.0	—	0	0.1	—	0.1	
				I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
Input leakage current		I_{IN}	V_{IN} = 5.5 V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	μA

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = −40 to 85°C	Unit
			V_{CC} (V)	Limit	Limit	
Minimum pulse width (CK)	$t_{W(L)}$	—	2.7	8.5	10.0	ns
	$t_{W(H)}$		3.3 ± 0.3	6.0	7.0	
Minimum pulse width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$	—	2.7	8.5	10.0	ns
			3.3 ± 0.3	6.0	7.0	
Minimum set-up time	t_s	—	2.7	8.0	9.5	ns
			3.3 ± 0.3	5.5	6.5	
Minimum hold time	t_h	—	2.7	0.5	0.5	ns
			3.3 ± 0.3	0.5	0.5	
Minimum removal time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}	—	2.7	6.5	7.5	ns
			3.3 ± 0.3	5.0	5.0	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	2.7	15	—	7.3	15.0	1.0	18.5	ns
				50	—	9.8	18.5	1.0	22.0	
			3.3 ± 0.3	15	—	5.7	9.7	1.0	11.5	
				50	—	8.2	13.2	1.0	15.0	
Propagation delay time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	2.7	15	—	8.4	15.6	1.0	18.5	ns
				50	—	10.9	19.1	1.0	22.0	
			3.3 ± 0.3	15	—	6.6	10.1	1.0	12.0	
				50	—	9.1	13.6	1.0	15.5	
Maximum clock frequency	f_{max}	—	2.7	15	55	135	—	50	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	95	145	—	80	—	
				50	60	85	—	50	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C_{IN}			(Note 2)	—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}			(Note 3)	—	25	—	—	—	pF

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

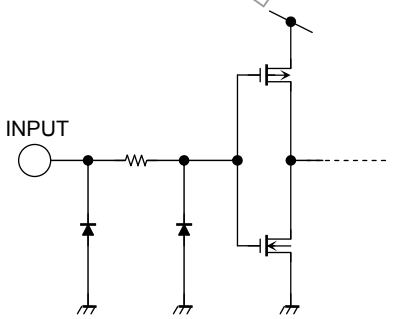
Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per F/F)

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)

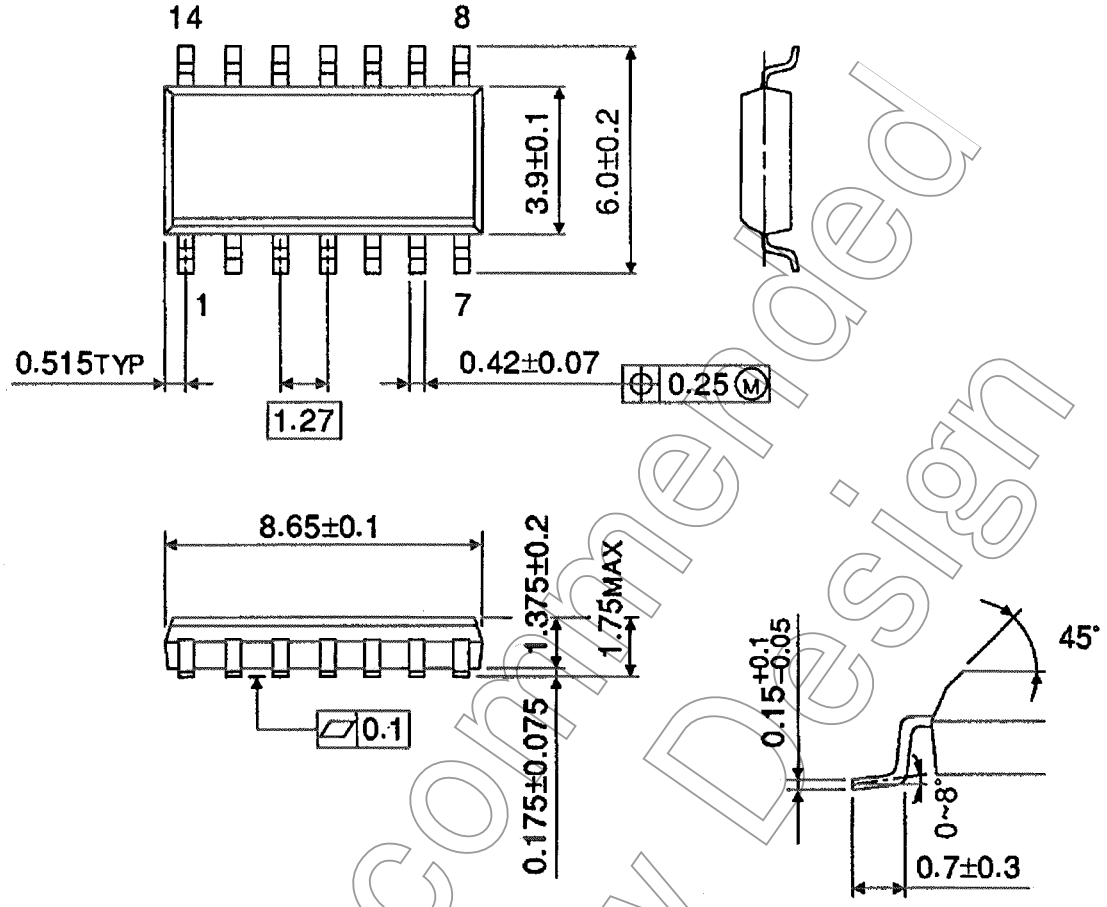
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	—	3.3	0.3	0.5	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	—	3.3	−0.3	−0.5	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	—	3.3	—	0.8	V

Input Equivalent Circuit



Package Dimensions (Note)

SOL14-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

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