



Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377
IDT54/74FCT377A
IDT54/74FCT377C

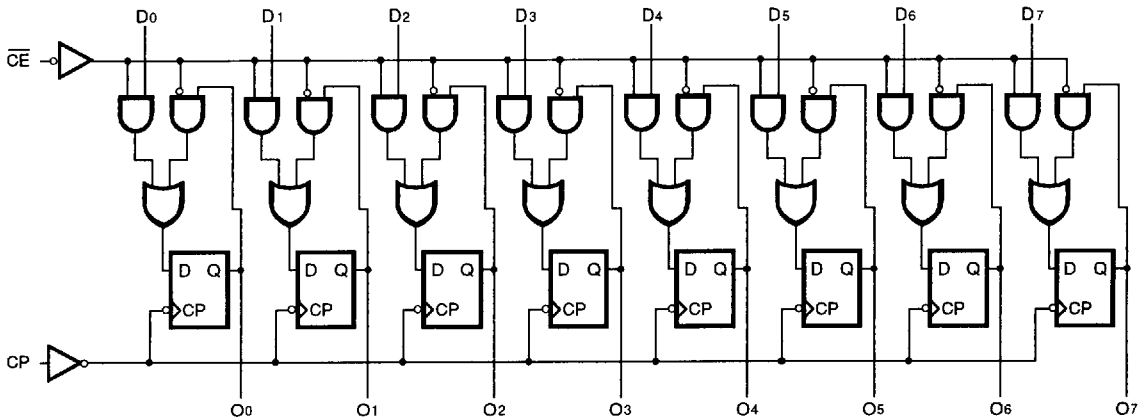
FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed
- **IDT54/74FCT377A 25% faster than FAST**
- **IDT54/74FCT377C 40% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial) and 32mA (military)
- IIH and IIL only 5µA max.
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Meets or exceeds JEDEC Standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

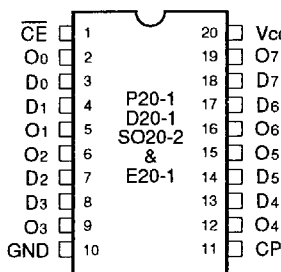
DESCRIPTION:

The IDT54/74FCT377/A/C is an octal D flip-flop built using an advanced dual metal CMOS technology. The IDT54/74FCT377/A/C have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable (CE) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The CE input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

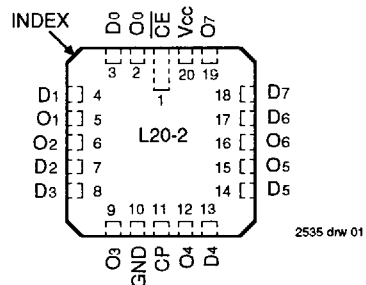
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

PIN DESCRIPTION

Pin Names	Description
D ₀ -D ₇	Data Inputs
CE	Clock Enable (Active LOW)
O ₀ -O ₇	Data Outputs
CP	Clock Pulse Input

2535 tbl 01

FUNCTION TABLE⁽¹⁾

Operating Mode	Inputs			Outputs
	CP	CE	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	H	H	X	No Change

NOTE:

2535 tbl 02

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock Transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition
- X = Immaterial
- ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTES:

2535 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

2535 tbl 04

- This parameter is guaranteed but not tested.



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$
 Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_I = V_{CC}$ $V_I = 2.7V$ $V_I = 0.5V$ $V_I = \text{GND}$	—	—	5	μA	
I_{IL}	Input LOW Current		—	—	5 ⁽⁴⁾		
			—	—	-5 ⁽⁴⁾		
			—	—	-5		
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$	-60	-120	—	mA	
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	V_{HC}	V_{CC}	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}		—
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3		—
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	V_{LC}	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3		0.5

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2535 tbl 05

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open CE = GND One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle CE = GND One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4.0	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6.0	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle CE = GND Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	4.0	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.2	16.8 ⁽⁵⁾	

NOTES: 2535 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH \cdot N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT377				IDT54/74FCT377A				IDT54/74FCT377C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay CP to On	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.2	2.0	5.5	ns
tSU	Set-up Time HIGH or LOW Dn to CP		2.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Dn to CP		2.0	—	2.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW CE to CP		4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
tH	Hold Time HIGH or LOW CE to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns

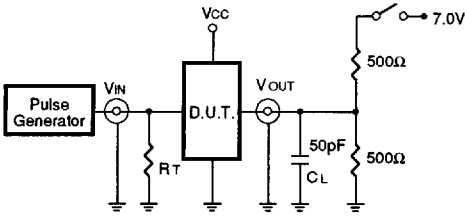
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2535 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

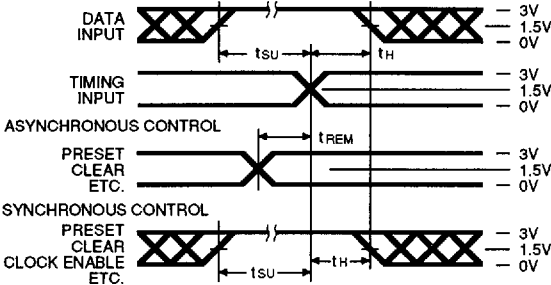
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

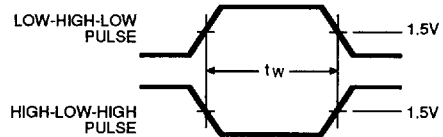
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Z_{out} of the Pulse Generator.

2535 tbi 08

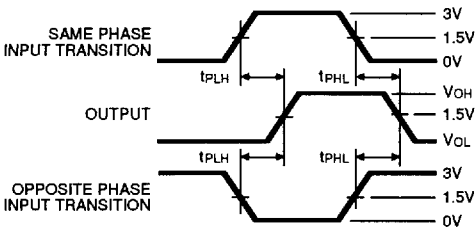
SET-UP, HOLD AND RELEASE TIMES



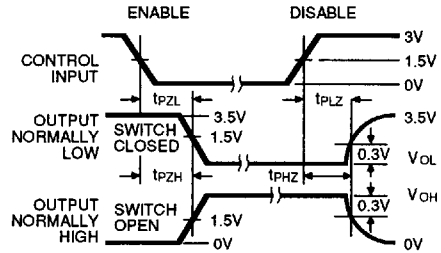
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

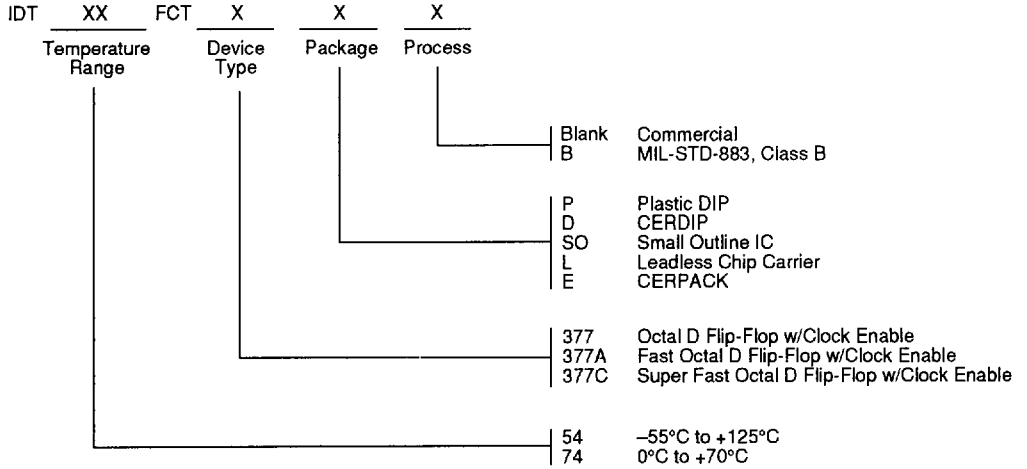


NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_o ≤ 50Ω; t_r ≤ 2.5ns; t_r ≤ 2.5ns.

2535 drw 04

ORDERING INFORMATION



2535 drw 03