The documentation and process conversion measures necessary to comply with this document shall be completed by 27 August 2004.

INCH-POUND

MIL-PRF-19500/560F
27 May 2004
SUPERSEDING
MIL-PRF-19500/560E
6 March 2002

* PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, SWITCHING TYPE 2N5339 AND 2N5339U3, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN silicon switching transistors. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500 and two levels of product assurance are provided for each unencapsulated device type as specified in MIL-PRF-19500.

* 1.2 Physical dimensions. See figure 1 (TO-39), figure 2 for U3 devices (TO-276AA) and figures 3, 4, and 5 for JANHC and JANKC (die) dimensions.

* 1.3 Maximum ratings Unless specified, T_A = 25°C.

Types	P_T (1) T_A = +25°C	P_T (1) T_C = +25°C	$R_{\theta JA}$	$R_{\theta JC}$	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_B	T_J and T_{STG}
	W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	°C
2N5339	1.0	17.5	175	10	100	100	6.0	5.0	1.0	-65 to +200
2N5339U3	1.0	75		2.3	100	100	6.0	5.0	1.0	-65 to +200

(1) For derating, see figures 6, 7, and 8.

1.4 Primary electrical characteristics T_A = +25°C. (Unless otherwise indicated, applies to all devices.)

Limits	h_{FE1} (1) V_{CE} = 2.0 V dc; I_C = 0.5 A dc	h_{FE2} (1) V_{CE} = 2.0 V dc; I_C = 2.0 A dc	h_{FE3} (1) V_{CE} = 2.0 V dc; I_C = 5.0 A dc
Min	60	60	40
Max		240	

(1) See note at end of 1.4.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://www.dodssp.daps.mil/.

1.4 Primary electrical characteristics T_A = +25°C. - Continued.

Limits	$\|h_{FE}\|$ f = 10 MHz V_{CE} = 10 V dc I_C = 0.5 A dc	C_{obo} V_{CE} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	Switching		$V_{CE(SAT)1}$ I_C = 2.0 A dc I_B = 0.2 A dc (1)	$V_{BE(SAT)1}$ I_C = 2.0 A dc I_B = 0.2 A dc (1)
			See figure 4 t_{on}	See figure 5 t_{off}		
		pF	µs	µs	V dc	V dc
Min	3.0					
Max	15.0	250	0.2	2.2	0.7	1.2

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://www.dodssp.daps.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

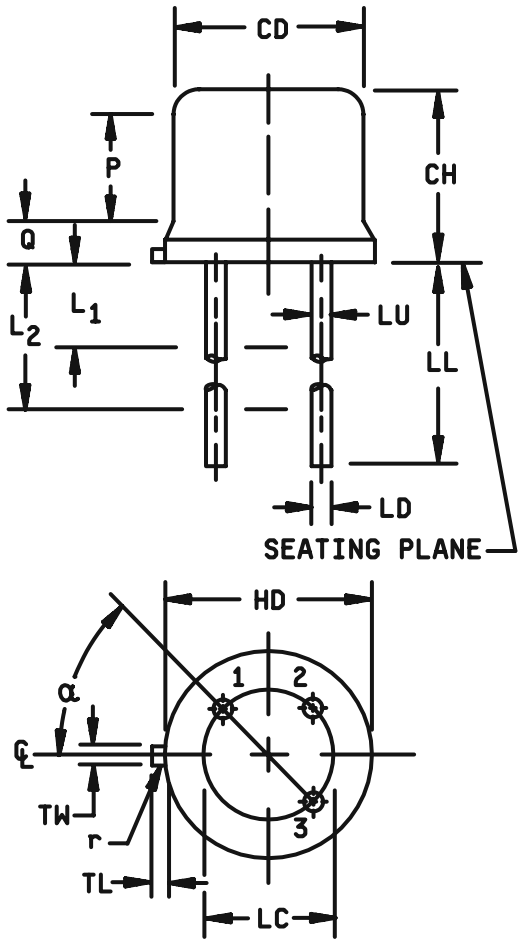


FIGURE 1. Physical dimensions (TO-39).

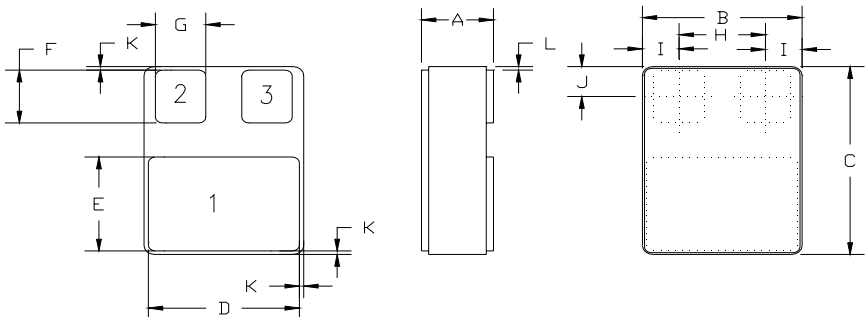
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.355	7.75	8.51	5
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	3
LC	.200 TP		5.08 TP		6
LD	.016	.021	.41	.53	7
LL	.500	.750	12.70	19.05	7
LU	.016	.019	.41	.48	7
L1		.050		1.27	7
L2	.250		6.35		7
TL	.029	.045	.74	1.14	3
TW	.028	.034	.71	.86	10
P	.100		2.54		5
Q		.050		1.27	4
r		.010		.25	10, 11
α	45° TP		45° TP		6
Notes	1, 2, 8, 9		1, 2, 8, 9		

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L1 and L2. Dimension LD applies between L2 and LL minimum.
8. Lead designation, depending on device type, shall be as follows:

Lead number	TO-39
1	Emitter
2	Base
3	Collector

9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 1. Physical dimensions (TO-39) - Continued.

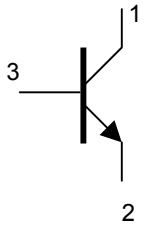


BOTTOM VIEW

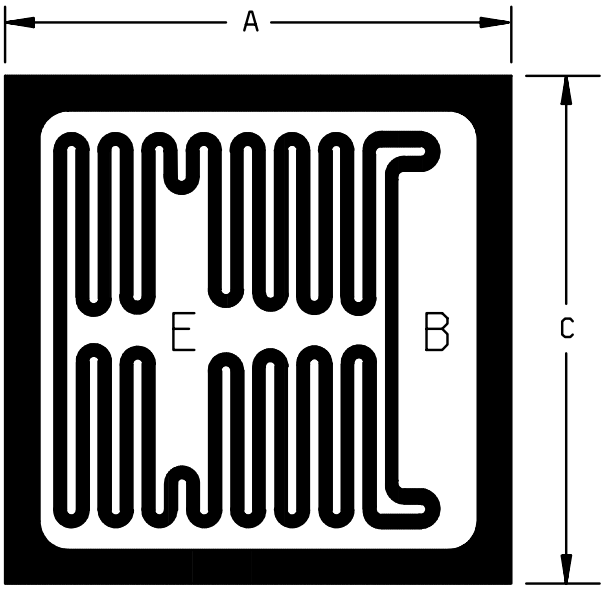
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.111	.122	2.82	3.10
B	.291	.301	7.39	7.65
C	.395	.405	10.03	10.29
D	.281	.291	7.14	7.39
E	.220	.230	5.59	5.84
F	.115	.125	2.92	3.18
G	.09	.100	2.29	2.54
H	.145	.155	3.68	3.94
I	.073 TYP.		1.85 TYP.	
J	.083 TYP.		2.11 TYP.	
K	.005 TYP.		0.13 TYP.	
L	.015 TYP.		0.38 TYP.	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.

SCHEMATIC



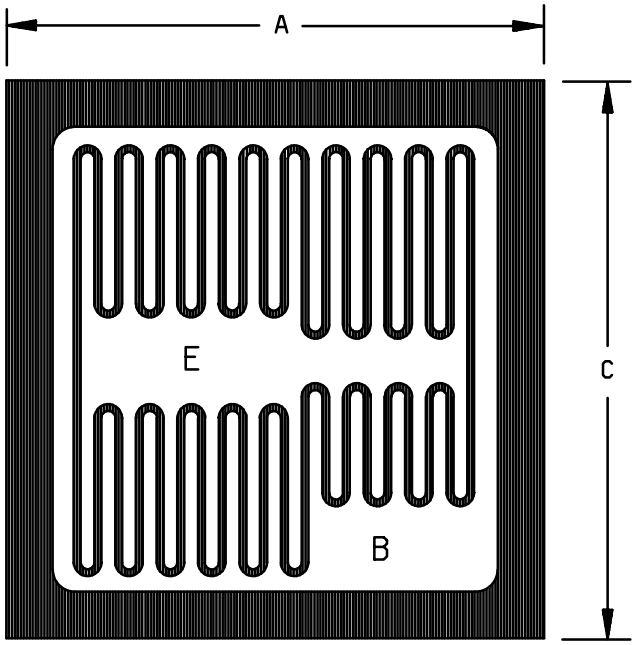
* FIGURE 2. Physical dimensions and configuration (U3) (SMD 5) (TO-276AA).



Letter	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.120	.124	3.05	3.15
C	.120	.124	3.05	3.15

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
   Thickness: .008 inch (0.20 mm) to .012 inch (0.30 mm).
   Top metal: Aluminum 40,000 Å minimum, 50,000 Å nominal.
   Back metal: Gold 2,500 Å minimum, 3,000 Å nominal.
   Back side: Collector.
   Bonding pad: B = .015 inch (0.38 mm) x .072 inch (1.83 mm).
   E = .015 inch (0.38 mm) x .060 inch (1.52 mm).
4. Unless otherwise specified, tolerance is ± .005 inch (0.13 mm).

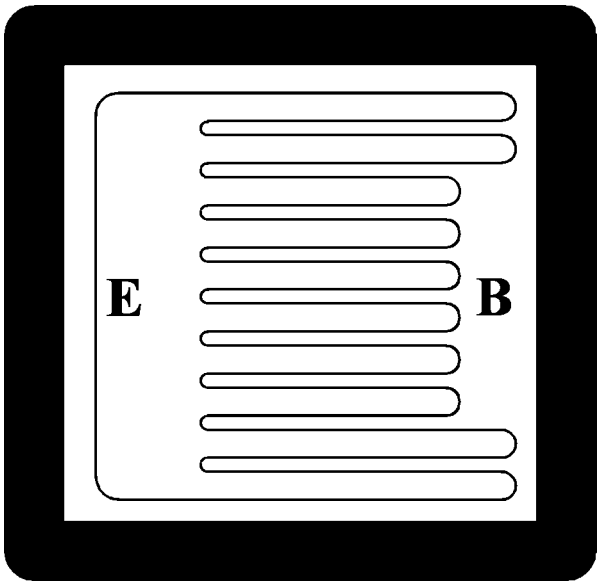
FIGURE 3. Physical dimensions JANHCA and JANKCA.



Letter	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.098	.102	2.49	2.59
C	.098	.102	2.49	2.59

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The physical characteristics of the die are:
   Thickness: .006 inch (0.15 mm) to .010 inch (0.25 mm).
   Top metal: Aluminum 25,000 Å minimum, 37,500 Å nominal.
   Back metal: Gold 1,500 Å minimum, 6,500 Å nominal.
   Back side: Collector.
4. Unless otherwise specified, tolerance is ± .005 inch (0.13 mm).

FIGURE 4. Physical dimensions JANHCB and JANKCB.



1.	Chip size.	.120 (3.05 mm) x .120 (3.05 mm) inch ±.002 inch (0.051 mm).
2.	Chip thickness	.010 (0.254 mm) ±.0015 (0.038 mm) inch nominal.
3.	Top metal	Aluminum 30,000Å minimum, 33,000Å nominal.
4.	Back metal	A. Al/Ti/Ni/Ag12kÅ/3kÅ/7kÅ/7kÅ minimum15kÅ/5kÅ/10kÅ/10kÅ nominal. B. Gold 2,500Å minimum, 3000Å nominal.
5.	Backside	Collector.
6.	Bonding pad	B = .052 (1.32 mm) x .012 (0.305 mm) inch, E = .084 (3.05 mm) x .012 (0.305 mm) inch.

FIGURE 5. Physical dimensions JANHCC and JANKCC.

3. REQUIREMENTS

* 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (TO-39), figure 2 for U3 (TO-276AA), and figures 3, 4, and 5 (JANHC and JANKC) devices herein.

* 3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

* 3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I, group A herein.

* 3.7 Marking. Devices shall be marked in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX, JANTXV, and JANS levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see MIL-PRF-19500)	Measurements	
	JANS level	JANTX and JANTXV levels
* 3C	Thermal impedance, method 3131 of MIL-STD-750.	Thermal impedance, method 3131 of MIL-STD-750.
7	Optional	Optional
9	I_{CBO1} and h_{FE2}	Not applicable
11	I_{CBO1}; h_{FE2}, ΔI_{CBO1} = ± 100 percent of initial value or 1.0 μA dc, whichever is greater; Δh_{FE2} = ± 15 percent	I_{CBO1} and h_{FE2}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO1} = ± 100 percent of initial value or 1.0 μA dc, whichever is greater; Δh_{FE2} = ± 15 percent.	Subgroup 2 of table I herein; ΔI_{CBO1} = ± 100 percent of initial value or 1.0 μA dc, whichever is greater; Δh_{FE2} = ± 15 percent.
14	Required	Required

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750. Power shall be applied to the device to achieve T_J = minimum +175°C and minimum power dissipation of P_D = 75 percent P_T maximum as defined in 1.3.

4.3.2 Screening for JANHC and JANKC. Screening for JANHC and JANKC die shall be in accordance with MIL-PRF-19500, “Discrete Semiconductor Die/Chip Lot Acceptance”. Burn-in duration for JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). See figures 9, 10, and 11. The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in 4.3, screen 3c and the subgroup 2 of table I shall comply with the thermal impedance graph in figures 9 10, and 11 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131 of MIL-STD-750.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein. Electrical measurements (end-points) requirements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa of MIL-PRF-19500 (JANS) and 4.4.2.1 herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. See 4.4.2.2 herein and table VIb of MIL-PRF-19500 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) requirements shall be in accordance with table I, subgroup 2 herein.

* 4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Conditions
B4	1037	$V_{CB} \geq 10$ V dc.
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) $V_{CB} = 10$ V dc; $P_D \geq 100$ percent of rated P_T (see 1.3). Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table Via, adjust T_A or P_D to achieve $T_J = +275°C$ minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve $T_J = +225°C$ minimum.
B5	2037	Test condition A.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

	Step	Method	Condition
*	1	1027	Steady-state life: Test condition B, 1,000 hours, $V_{CB} = 10$ V dc, power shall be applied to the device to achieve $T_J = +175°C$ minimum using a minimum of P_D of 75 percent of maximum rated P_T as defined in 1.3. n = 45, c = 0.
	2	1048	HTRB (high temperature reverse bias): Test condition A, 48 hours minimum. n = 45, c = 0.
	3	1032	High- temperature life (non-operating), t = 340 hours, $T_A = +200°C$. n = 22, c = 0.

4.4.3 Group C inspection, Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

* 4.4.3.1 Group C inspection, table VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E.
C5	3131	See 4.5.3.
C6	1037	For solder die attach: $V_{CB} \geq 10$ V dc, T_A = room ambient as defined in the general requirements of MIL-STD-750. 6,000 cycles.
* C6	1027	For eutectic die attach: $V_{CB} \geq 10$ V dc, adjust P_T to achieve $T_J = + 175°C$ min.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500, and herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

* 4.5.3 Thermal resistance (to be performed for qualification inspection only). The thermal resistance measurements shall be conducted in accordance with method 3131 of MIL-STD-750. The following details shall apply:

a. Collector current magnitude during power application shall be 0.15 A dc.

b. Collector to emitter voltage magnitude shall be 20 V dc.

c. Reference temperature measuring point shall be the case.

d. Reference point temperature shall be + 25°C ≤ T_R ≤ +35° C and recorded before the test is started.

e. Mounting arrangement shall be with heat sink to case.

f. Maximum limit shall be $R_{\theta JC}$ = 10.0°C/W for TO-39 devices and $R_{\theta JC}$ = 2.3°C/W for U3 devices.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
* Subgroup 1 2/						
Visual and mechanical examination 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Heremetic seal 4/	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 5/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs n = 11 wires, c = 0				
Decap internal visual (design verification) 5/	2075	n = 4 device, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = 50 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	100		V dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 100 V dc	I_{CEO}		100	μA dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 1.5 V dc; V_{CE} = 90 V dc	I_{CEX1}		1	μA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 100 V dc	I_{CBO}		1	μA dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Emitter to base, cutoff current	3061	Bias condition D; V_{EB} = 6.0 V dc	I_{EBO}		100	μA dc
Forward - current transfer ratio	3076	V_{CE} = 2.0 V dc; I_C = 0.5 A dc, pulsed (see 4.5.1)	h_{FE1}	60		
Forward - current transfer ratio	3076	V_{CE} = 2.0 V dc; I_C = 2.0 A dc; pulsed (see 4.5.1)	h_{FE2}	60	240	
Forward - current transfer ratio	3076	V_{CE} = 2.0 V dc; I_C = 5.0 A dc; pulsed (see 4.5.1)	h_{FE3}	40		
Collector to emitter voltage (saturated)	3071	I_C = 2.0 A dc; I_B = 0.2 A dc; pulsed (see 4.5.1)	$V_{CE(SAT)1}$		0.7	V dc
Collector to emitter voltage (saturated)	3071	I_C = 5.0 A dc; I_B = 0.5 A dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = 2.0 A dc; I_B = 0.2 A dc; pulsed (see 4.5.1)	$V_{BE(SAT)1}$		1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; I_C = 5.0 A dc; I_B = 0.5 A dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		1.8	V dc
Subgroup 3						
High - temperature operation		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{CE} = 90 V dc; V_{BE} = 1.5 V dc;	I_{CEX2}		1.0	mA dc
Low-temperature operation		T_A = -55°C				
Forward - current transfer ratio	3076	V_{CE} = 2.0 V dc; I_C = 2.0 A dc; Pulsed (see 4.5.1)	h_{FE4}	12		

See footnotes at end of table.

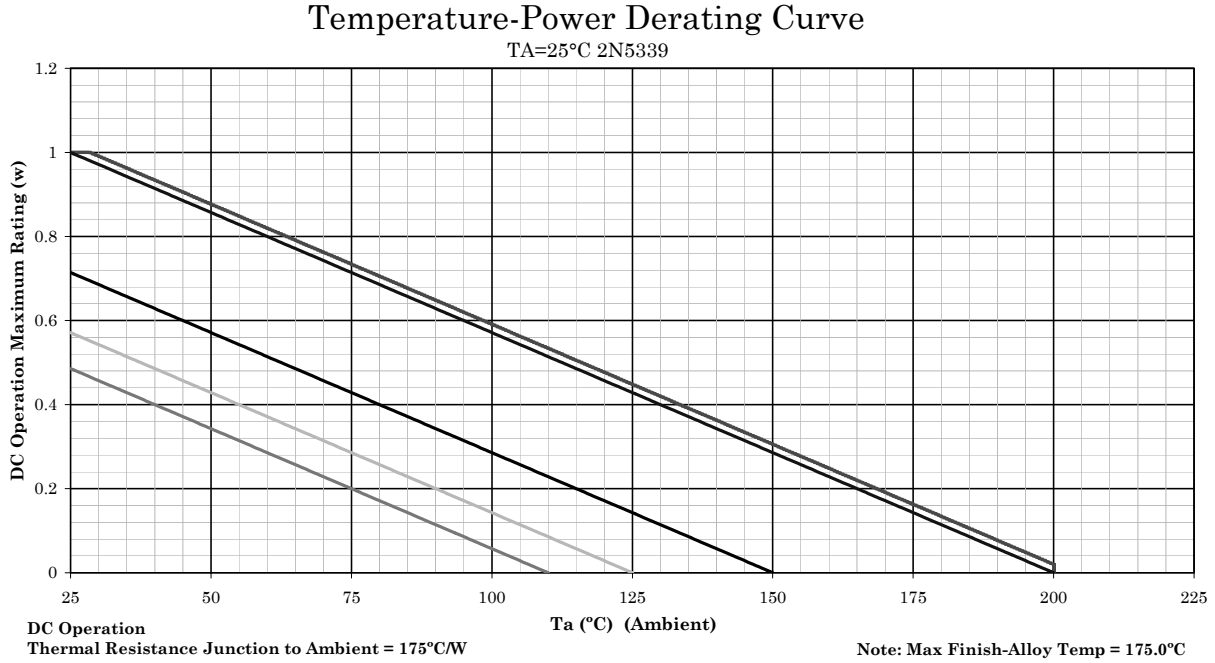
* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Small - signal short - circuit forward - current transfer ratio	3306	V_{CE} = 10 V dc; I_C = 0.5 A dc; f = 10 MHz	$\|h_{fe}\|$	3	15	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		250	pF
Input capacitance (output open - circuited)	3240	V_{BE} = 2.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz (see 4.5.2)	C_{ibo}		1,000	pF
Pulse response						
Pulse delay time	3251	See figure 12	t_d		100	ns
Pulse rise time	3251	See figure 12	t_r		100	ns
Pulse storage time	3251	See figure 13	t_s		2	μs
Pulse fall time	3251	See figure 13	t_f		200	ns
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = +25°C; t ≥ 0.5 s; 1 cycle				
Test 1		V_{CE} = 2.0 V dc; I_C = 5.0 A dc				
Test 2		V_{CE} = 5.0 V dc; I_C = 2.0 A dc				
Test 3		V_{CE} = 90 V dc; I_C = 55 mA dc				
End-point electrical measurements		See table I, subgroup 2				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for laser marked devices.
5/ Not required for JANS devices.

* TABLE II. Group E inspection (all quality levels) - for qualification and requalification only.

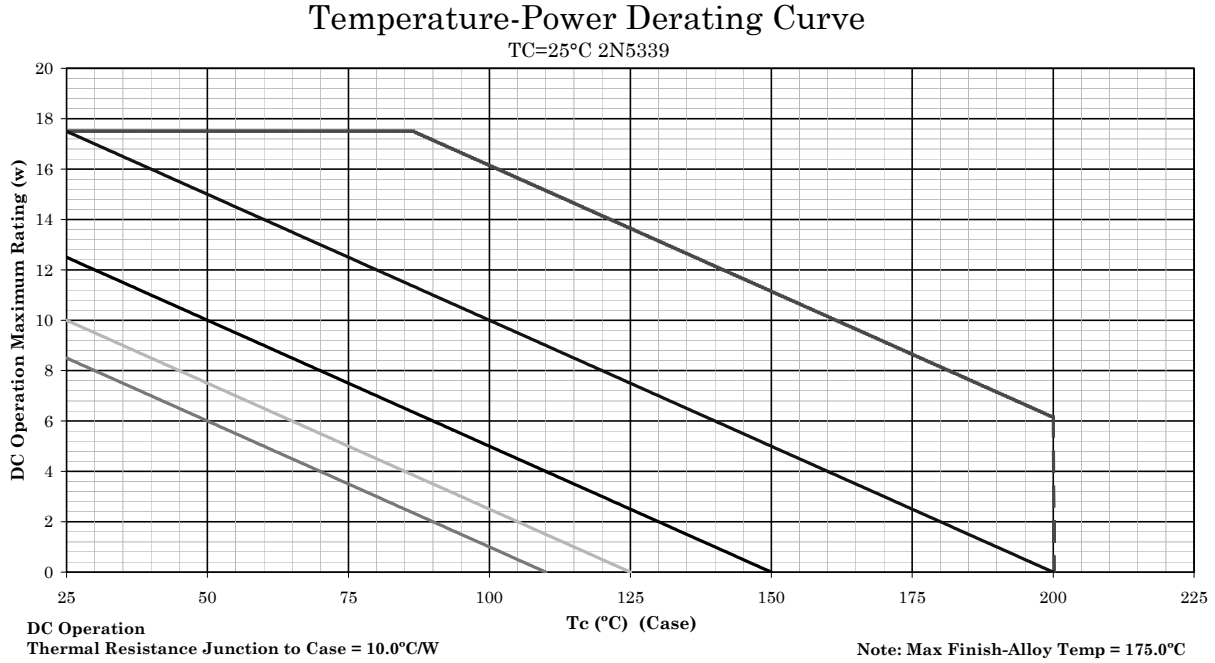
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal			
Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 3			
DPA (destructive physical analysis)	2102		3 devices c = 0
Subgroups 4			N/A
Thermal impedance curves		Each supplier shall submit their (typical) design thermal impedance curves. In addition, test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
Subgroups 5 and 6			
Not applicable			
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A for devices $\geq$ 400 V Condition B for devices $<$ 400 V	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

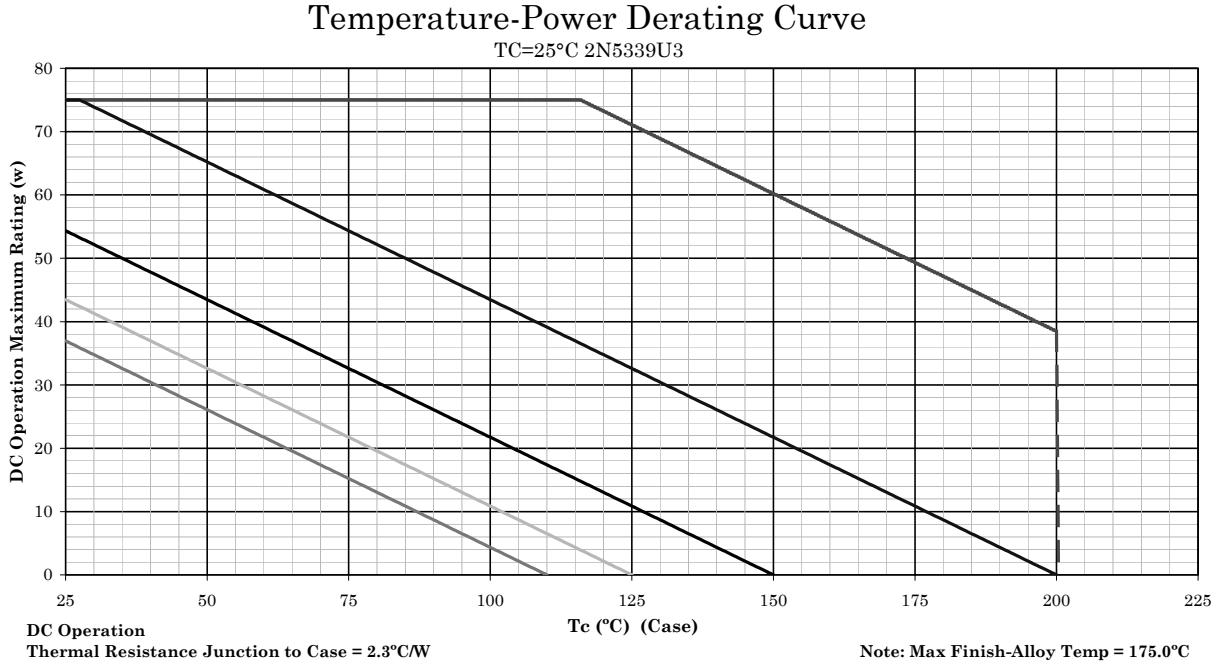
*FIGURE 6. Derating for 2N5339 ($R_{\theta JA}$) (TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

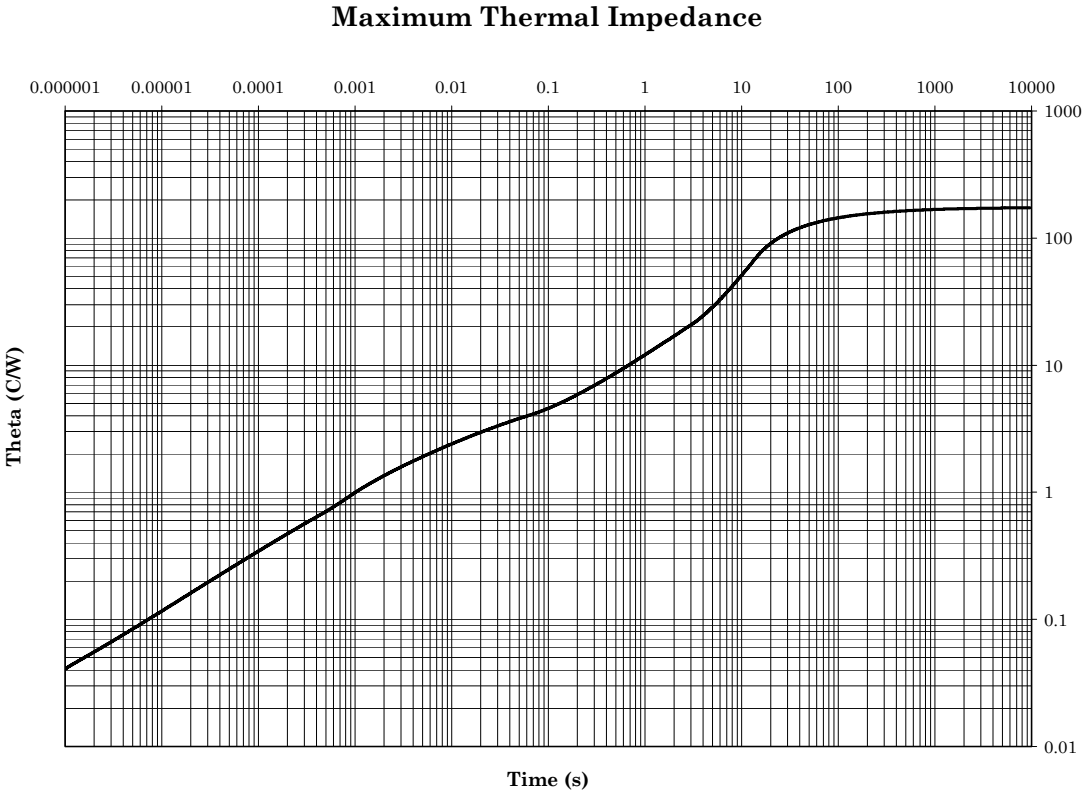
*FIGURE 7. Derating for 2N5339 ($R_{\theta JC}$) (TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

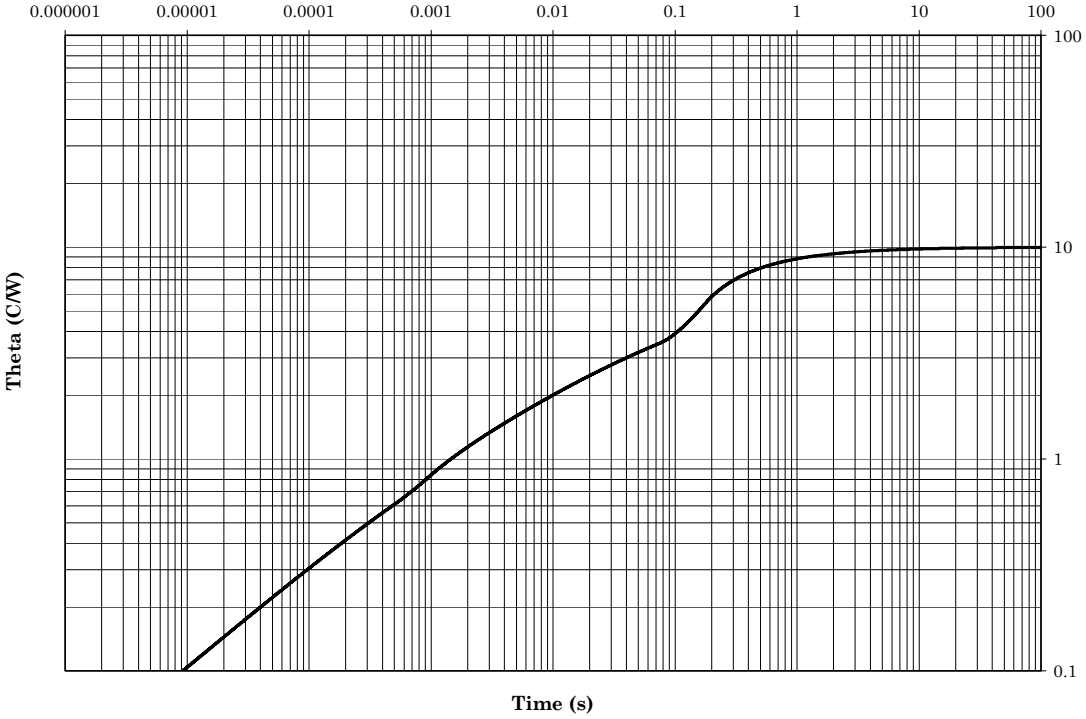
*FIGURE 8. Derating for 2N5339U3 ($R_{\theta JC}$).



T_A = +25°C, Pdiss = 800 mW, thermal resistance = 175°C/W (ambient thermal resistance varies with power).

* FIGURE 9. Thermal impedance graph ($R_{\theta JA}$) for 2N5339 (TO-5 and TO-39).

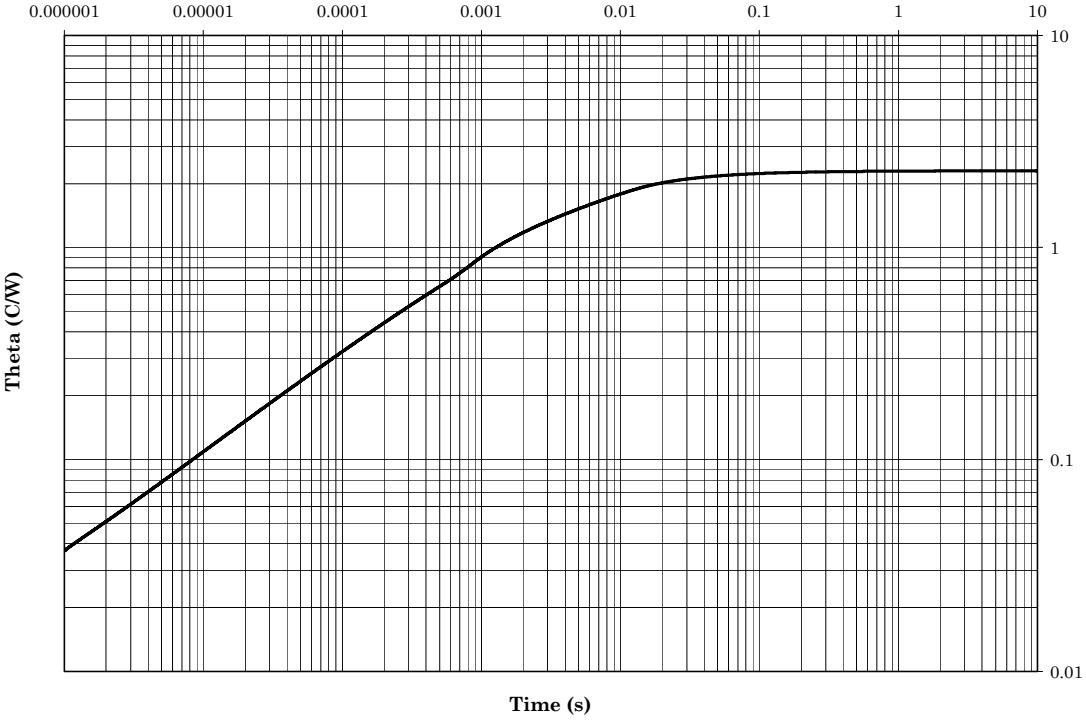
Maximum Thermal Impedance



T_C = +25°C, thermal resistance = 10°C/W.

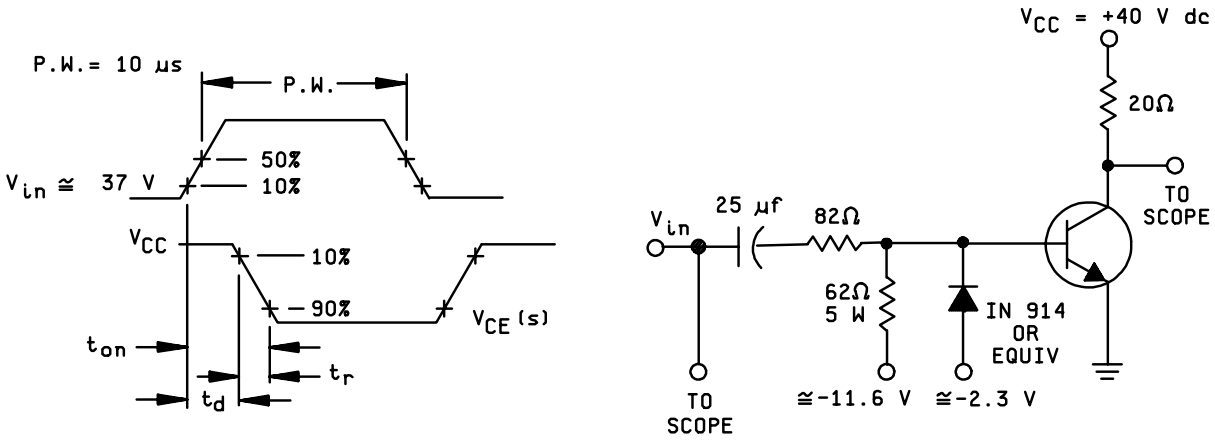
* FIGURE 10. Thermal impedance graph ($R_{\theta JC}$) for 2N5339 (TO-5 and TO-39).

Maximum Thermal Impedance



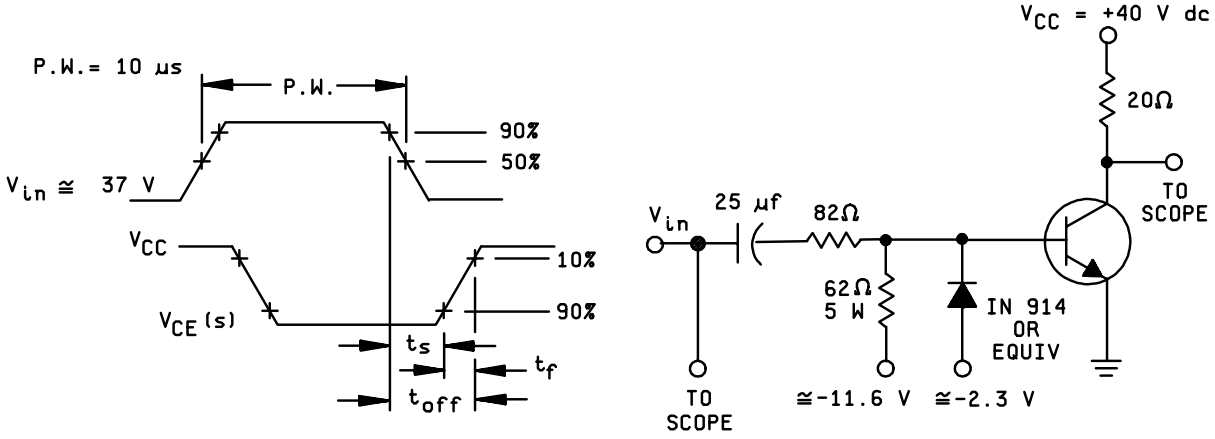
T_C = +25°C, thermal resistance = 2.3°C/W.

* FIGURE 11. Thermal impedance graph ($R_{\theta JC}$) for 2N5339U3 (U3).



NOTES:
1. The rise time (t_r) of the applied pulse shall be ≤ 20 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF, rise time ≤ 20 ns.
3. t_{on} conditions: I_C = 2 A, I_{B1} = 200 mA.

FIGURE 12. Saturated turn-on switching waveform and time test circuit.



NOTES:
1. The rise time (t_r) of the applied pulse shall be ≤ 20 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω.
2. Sampling oscilloscope: Z_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF, rise time ≤ 20 ns.
3. t_{on} conditions: C_I = 2 A, I_{B1} = I_{B2} = 200 mA.

FIGURE 13. Saturated turn-off switching time waveform and test circuit.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For die acquisition, the JANHC or JANKC letter version shall be specified (see figures 3 and 4).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

6.4 Application guidance. The following PNP type transistor is complimentary to the NPN device listed herein.

NPN	PNP
2N5339	2N6193

6.5 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example, JANHCA2N6193) will be identified on the QML.

JANC ordering information			
PIN	Manufacturers		
	33178	34156	43611
2N5339	JANHCA2N5339 JANKCA2N5339	JANHCB2N5339 JANKCB2N5339	JANHCC2N5339 JANKCC2N5339

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue

Custodians:
Army - CR
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2749)

Review activities:
Army - MI
Air Force - 19, 71, 99

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://www.dodssp.daps.mil/ .