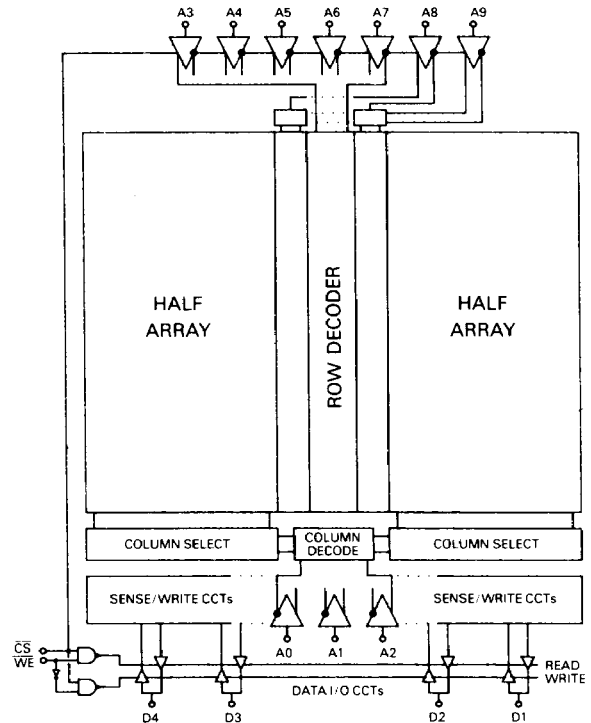


Radiation Hard 1024 × 4 Bit Static RAM

FEATURES

- Radiation hard 3μm CMOS-SOS technology
- Fast access time 90ns typical
- Total dose 10⁵ rad(Si)
- Transient upset 5 × 10¹⁰ rad(Si)/sec
- SEU 3.1 × 10⁻¹⁰ errors/bit day
- No latch-up possible
- Single 5V supply
- TTL and CMOS compatible inputs
- Fully static operation
- Three state output
- Low standby current 50μA typical
- -55°C to +125°C operation
- Data retention at 2 volts supply

BLOCK DIAGRAM



GENERAL DESCRIPTON

The MA5114 4K Static RAM is configured as 1024 × 4 bits and manufactured using MEDL's CMOS-SOS high performance, radiation hard, 3μm technology.

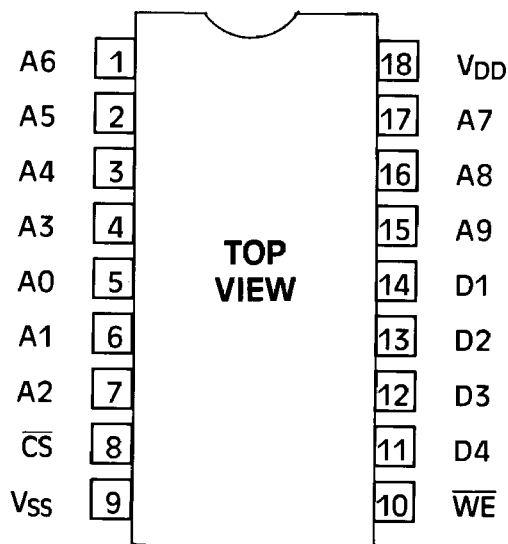
The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the High state.

TRUTH TABLE

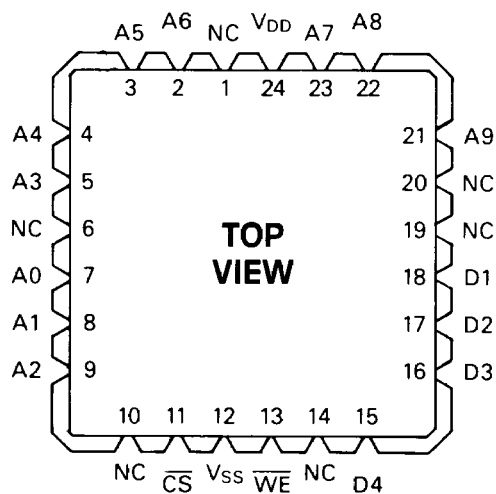
\overline{CS}	\overline{WE}	I/O Pin	Mode
H	H	High Z	Not selected
H	L	High Z	Not selected
L	H	Data out	Selected
L	L	Data in	Selected

Radiation Hard 1024 × 4 Bit Static RAM

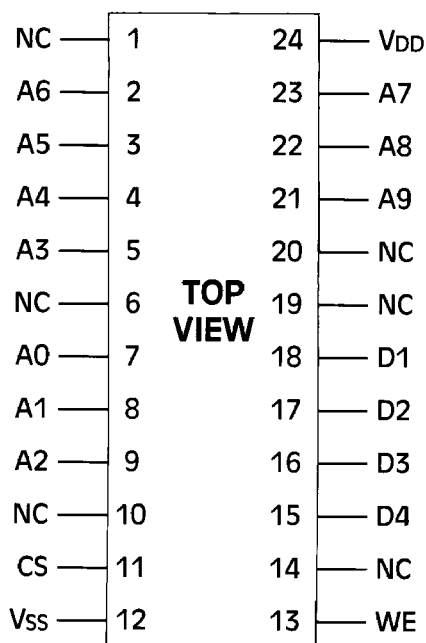
PIN ASSIGNMENT



**PACKAGE A —
18 LEAD CERAMIC DIL**



**PACKAGE I —
24 CONTACT CERAMIC LCC**



**PACKAGE H —
24 LEAD CERAMIC FLATPACK**

Radiation Hard 1024 × 4 Bit Static RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max
V _{DD}	Supply Voltage	−0.5V	8V
V _I	Input Voltage	−0.3V	V _{DD} + 0.3V
T _A	Operating Temperature	−55°C	125°C
T _S	Storage Temperature	−65°C	150°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The following D.C. and A.C. electrical characteristics apply pre-radiation at T_A = −55°C to +125°C, V_{DD} = 5V ±10% and to post 100kRad(Si) total dose radiation at T_A = 25°C, V_{DD} = 5V ±10%

OPERATING D.C. ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{DD}	Supply Voltage	4.5	5	5.5	V	
V _{IH}	Logical '1' Input Voltage	$\frac{V_{DD}}{2}$		V _{DD}	V	
V _{IL}	Logical '0' Input Voltage	V _{SS}		0.8	V	
V _{OH}	Logical '1' Output Voltage	2.4			V	I _{OH} = −1mA
V _{OL}	Logical '0' Output Voltage			0.4	V	I _{OL} = 2mA
I _{LI}	Input Leakage Current			±10	μA	All inputs except \overline{CS}
I _{ZOH}	Output Leakage Current			+10	μA	Output disabled, V _{OUT} = V _{DD}
I _{ZOL}	Output Leakage Current			−20	μA	Output disabled, V _{OUT} = V _{SS}
I _{PUI}	Input Pull-Up Current			−100	μA	V _{IN} = V _{SS} \overline{CS} input only
I _{PDI}	Input Leakage Current			5	μA	V _{IN} = V _{DD} \overline{CS} input only
I _{DDL}	Power Supply Current, Standby		50	1000	μA	Chip disabled
I _{DD}	Power Supply Current		12	16	mA	f _{RC} = 1MHz, \overline{CS} = 50% mark:space

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{DR}	V _{CC} for Data Retention	2.0			V	\overline{CS} = V _{DR}
I _{DDR}	Data Retention Current		30	500	μA	\overline{CS} = V _{DR} , V _{DR} = 2.0V

Radiation Hard 1024 × 4 Bit Static RAM

A.C. ELECTRICAL CHARACTERISTICS

READ CYCLE

Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	135		ns
t_A	Access Time		135	ns
t_{CA}	Chip Select to Output Valid		135	ns
t_{CX} (Note 4)	Chip Select to Output Active	10		ns
t_{COT} (Note 4)	Chip Select to Output THREE STATE	10	50	ns
t_{OHA}	Output Hold from Address Change	10		ns

WRITE CYCLE

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time	135		ns
t_{AW}	Address to Write Set-Up Time	10		ns
t_{WP}	Write Pulse Width	50		ns
t_{WR}	Write Recovery Time	5		ns
t_{DS}	Data Set-Up Time	35		ns
t_{DH}	Data Hold Time	5		ns
t_{WOT} (Note 4)	Write Enable to Output THREE-STATE	10	50	ns
t_{CW}	Chip Selection to Write Low	25		ns

A.C. CONDITIONS OF TEST

- NOTE: 1 — Input Pulse V_{SS} to 3.0Volts
 2 — Times Measurement Reference Level 1.5Volts
 3 — Full Output Current Loading and $C_L = 100\text{pF}$
 4 — Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
 5 — Input Rise and Fall Times $\leq 5\text{ns}$

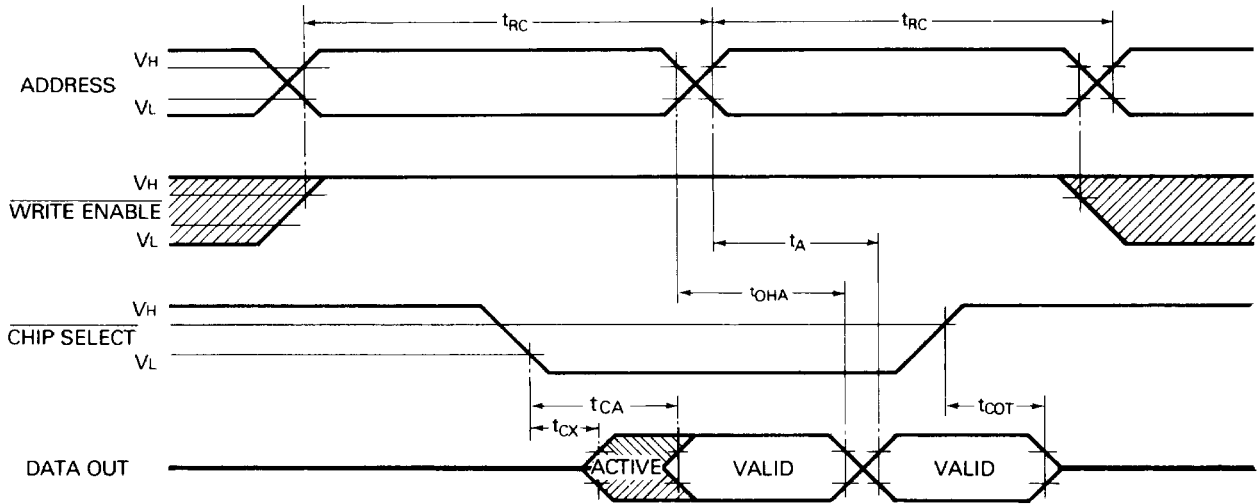
CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$

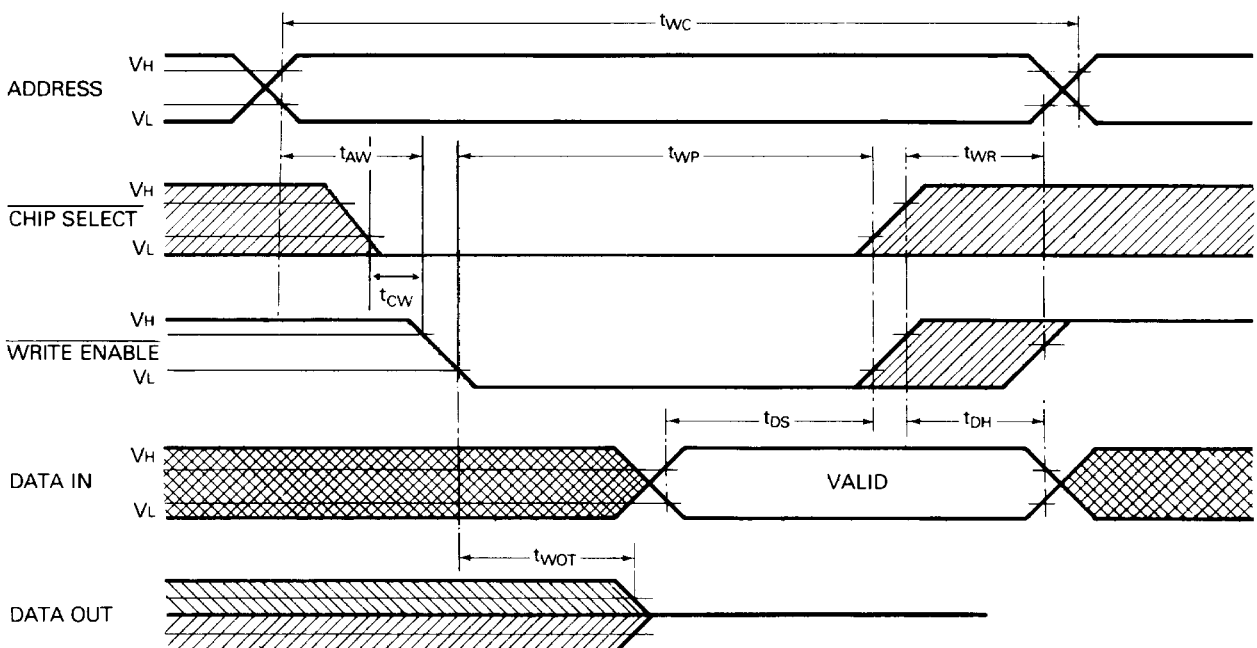
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{IN}	Input Capacitance		6	10	pF	$V_I = 0V$
C_{OUT}	Output Capacitance		8	12	pF	$V_O = 0V$

SWITCHING TIME WAVEFORMS

READ CYCLE



WRITE CYCLE



Marconi

Electronic Devices

MAXXXX

Radiation Hard Static RAM Family

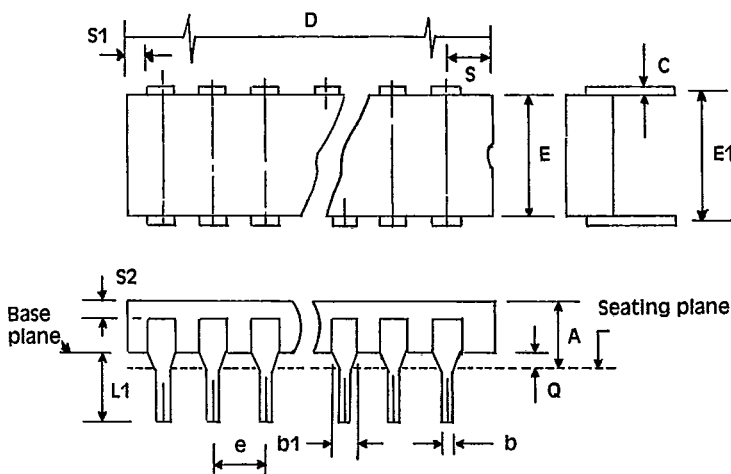
PACKAGING INFORMATION

Device Number	Sidebrazed Ceramic DIL	Ceramic Flatpack	Ceramic LCC
MA5101	Package D		
MA5104	Package A	Package H	
MA5114	Package A	Package H	Package I
MA6116	Package E	Package H	
MA6216	Package E	Package H	
MA9167	Package B	Package H	
MA9167	Package E		
MA9187	Package E	Package H	Package K

NOTE: Other Packages available on request.

PACKAGING INFORMATION

Packages A to E — CERAMIC DIL



DIMENSIONS IN INCHES

Dim.	Package A 18 LEAD 0.3 pitch		Package B 20 LEAD 0.3 pitch		Package C 22 LEAD 0.3 pitch		Package D 22 LEAD 0.4 pitch		Package E 24 LEAD 0.6 pitch	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A		.220		.220		.220		.220		.220
b	.013	.023	.014	.023	.014	.023	.014	.023	.014	.023
b1		.060		.060		.060		.060		.060
C	.008	.014	.008	.014	.008	.014	.008	.014	.008	.014
D		.910		1.010	1.089	1.111		1.100		1.212
E	.30 Nom.		.30 Nom.		.30 Nom.		.40 Nom.		.60 Nom.	
E1		.320		.320		.320		.420		.620
e	.10 Nom.		.10 Nom.		.10 Nom.		.10 Nom.		.10 Nom.	
L1	.175	.212	.185	.212	.175	.212	.185	.212	.185	.212
Q	.015	.060	.015	.060	.037	.039	.015	.060	.015	.060
S		.050		.050		.050		.050		.050
S1	.005		.005	0	.005		.005		.005	
S2	.005		.005		.005		.005		.005	

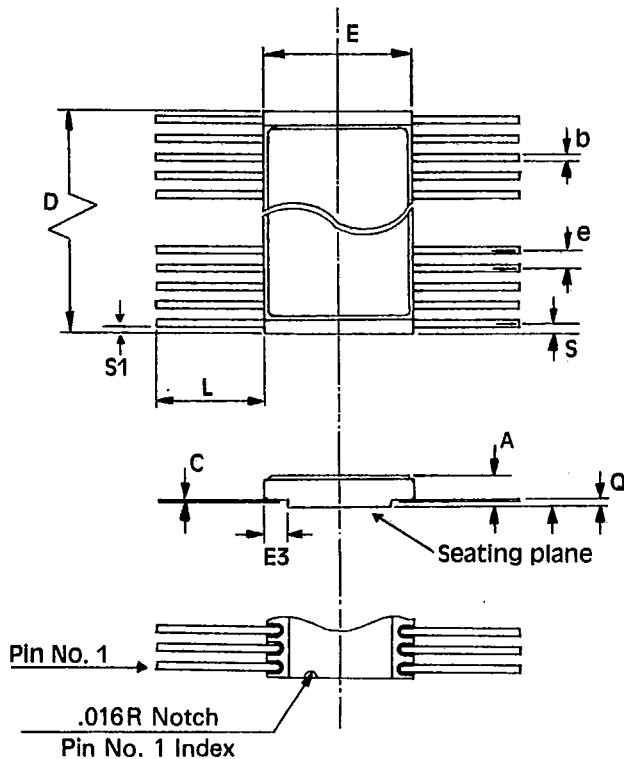
MAXXXX

**Radiation Hard
Static RAM Family**



PACKAGING INFORMATION

Packages H and J — CERAMIC FLATPACK



DIMENSIONS IN INCHES

Dim.	Package H		Package J	
	24 LEAD		28 LEAD	
	Min.	Max.	Min.	Max.
A		.105		.130
b	.015	.019	.015	.019
c	.004	.007	.003	.006
D	.585	.615		.740
E	.390	.410	.380	.420
E3	.030		.030	
e	.050 Nom.		.050 Nom.	
L	.265	.305	.250	.370
Q	.011	.018	.026	.045
S		.045		.045
S1	.005		.000	

Marconi

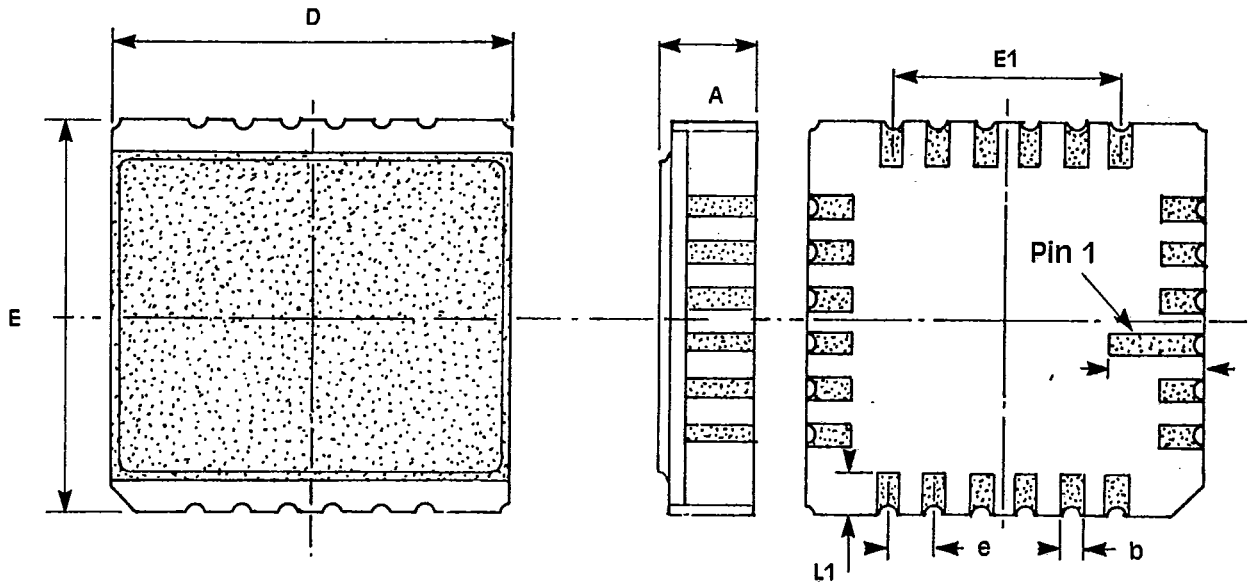
Electronic Devices

MAXXXX

Radiation Hard Static RAM Family

PACKAGING INFORMATION

PACKAGES I and K — LEADLESS CHIP CARRIER



DIMENSIONS IN INCHES

Dim.	Package I		Package K	
	24 LEAD		44 LEAD	
	Min.	Max.	Min.	Max.
A	—	0.096	0.101	0.119
b	0.018	0.022	0.025 Typ.	
D	0.345	0.360	0.643	0.662
E	0.345	0.360	0.643	0.662
E1	0.198	0.202	0.500 Typ.	
e	0.037	0.043	0.050 Typ.	
L1	0.040 Typ.		0.045	0.050

MARCONI ELECTRONIC DEVICES, INC



PREFIX DEVICE SUFFIX

MA 5101 CBC - XXX

Add S for Radiation Hard CMOS/SOS
 Package
 Screening & Inspection
 Temperature Range
 Special Requirements/Enhancements

PACKAGE

- A. Pin Grid Array
- C. Ceramic DIL
- E. Epic
- F. Flat Pack
- G. Cerdip
- L. Leadless Chip Carrier
- M. Module
- N. Naked Die
- P. Plastic DIL
- Q. Quad Plastic J-Lead
- R. Quad Cerpack J-Lead
- S. SO Plastic
- X. Special

TEMPERATURE RANGE

- A. Special
- B. 0 to 70°C
- C. -55 to +125°C
- D. -25 to +70°C
- E. -25 to +85°C
- F. -40 to +85°C
- G. -55 to +85°C
- H. -40 to +125°C
- J. -10 to +80°C
- K. 0 to +200°C

SCREENING & INSPECTION

- B. Mil Std-883C Class B
- G. Commercial Hermetic
- L. Commercial Plastic
- S. Mil Std-883C Class S
- T. ESA9000
- X. Special

