

DATA SHEET

74ALVCH16952

16-bit registered transceiver (3-State)

Preliminary specification
Supersedes data of 1994 Jul
IC24 Data Handbook

1998 Sep 01

16-bit registered transceiver (3-State)

74ALVCH16952

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple center pin power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{XX}, where X is AB or BA) provided that the clock enable (CE_{XX}) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input (OE_{XX}) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; t_r = t_f = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay CP _{nn} , to An, Bn	V _{CC} = 3.3V, C _L = 50pF V _{CC} = 2.5V, C _L = 30pF	3.2	ns
f _{MAX}	Maximum clock frequency		350	MHz
C _i	Input capacitance		3.0	pF
C _{PD}	Power dissipation capacitance per buffer	V _I = GND to V _{CC} ¹	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16952 DGG	ACH16952 DGG	SOT364-1

FUNCTION TABLE for register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CP _{XX}	CE _{XX}		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level
 L = LOW voltage level
 ↑ = LOW-to-HIGH transition

FUNCTION TABLE for output enable

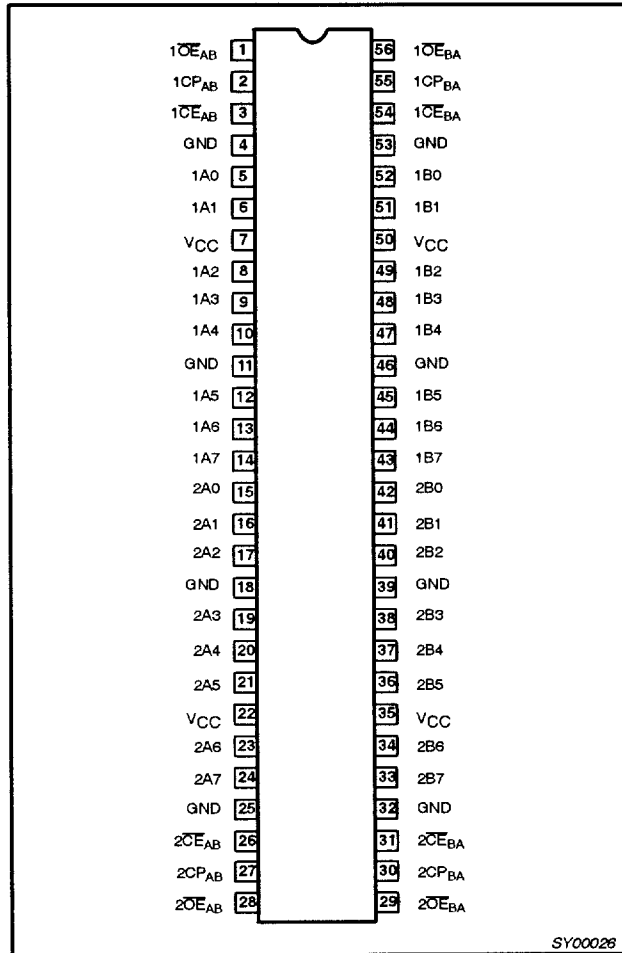
INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
OE _{nn}			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

NC = no change
 X = don't care
 Z = high impedance OFF-state

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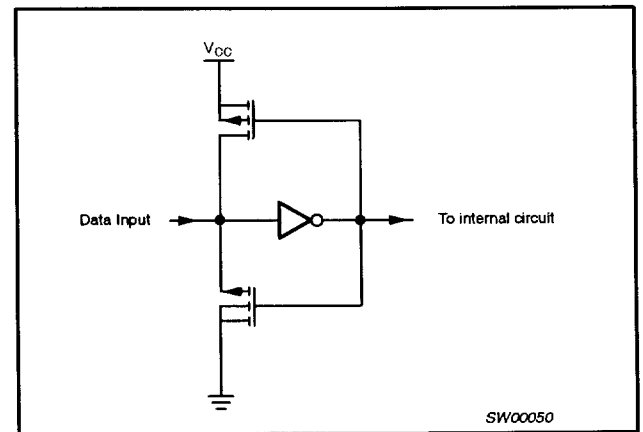
PIN CONFIGURATION



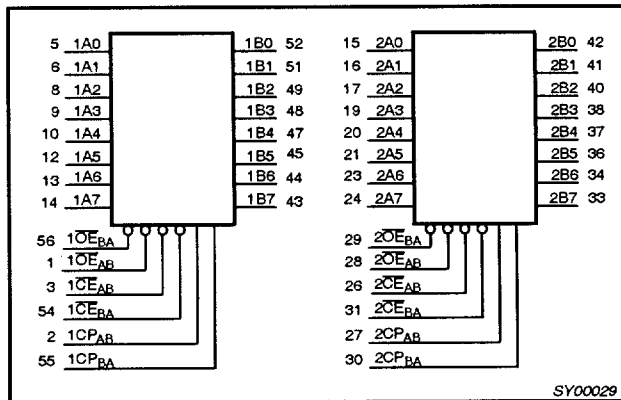
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	nOE _{AB}	Output enable A-to-B
2, 27	nCP _{AB}	Clock input A-to-B
3, 26	nCE _{AB}	A-to-B enable
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	Data inputs/outputs
29, 56	nOE _{BA}	Output enable B-to-A
30, 55	nCP _{BA}	Clock input B-to-A
31, 54	nCE _{BA}	B-to-A enable
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	Data inputs/outputs

BUSHOLD CIRCUIT



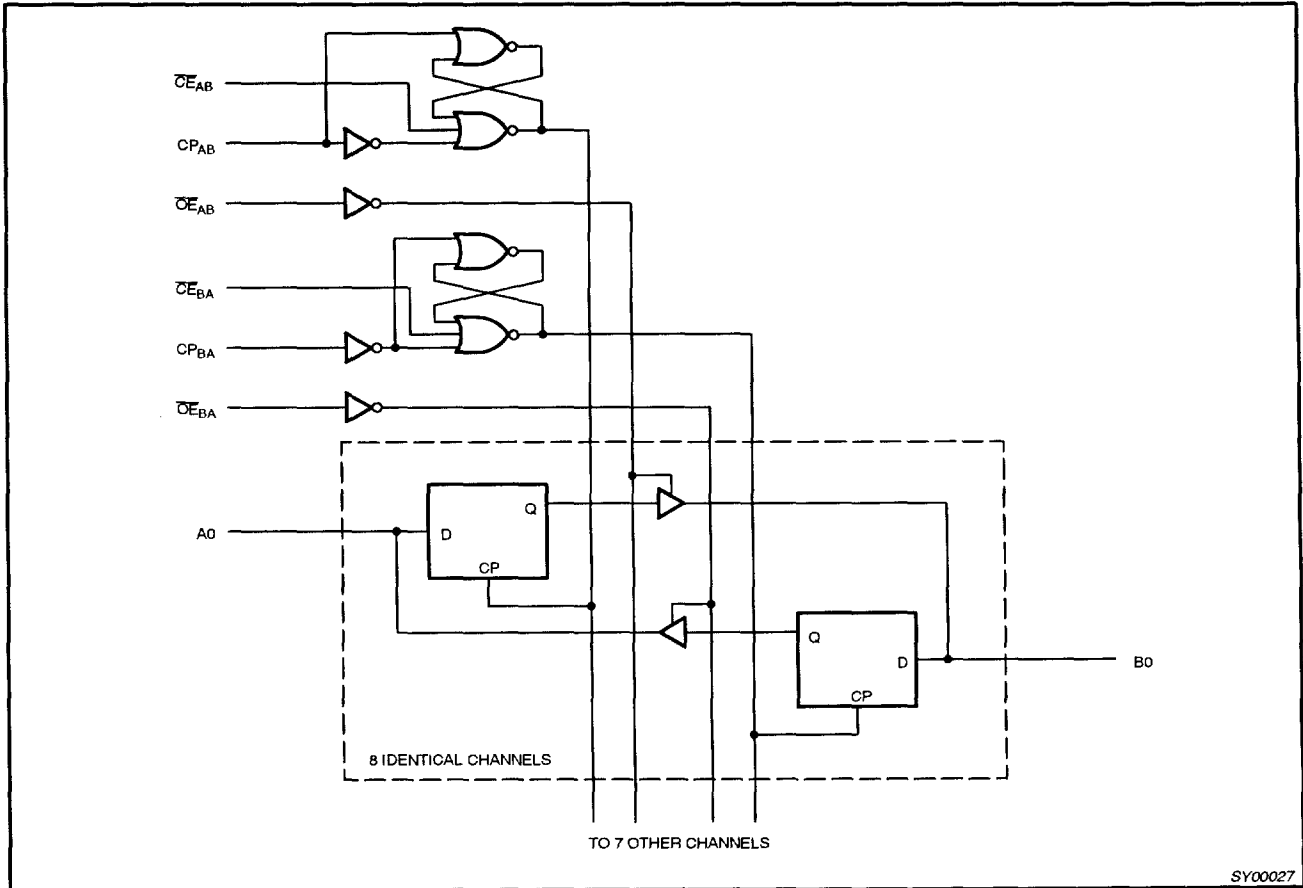
LOGIC SYMBOL



16-bit registered transceiver (3-State)

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LOGIC SYMBOL (one section)

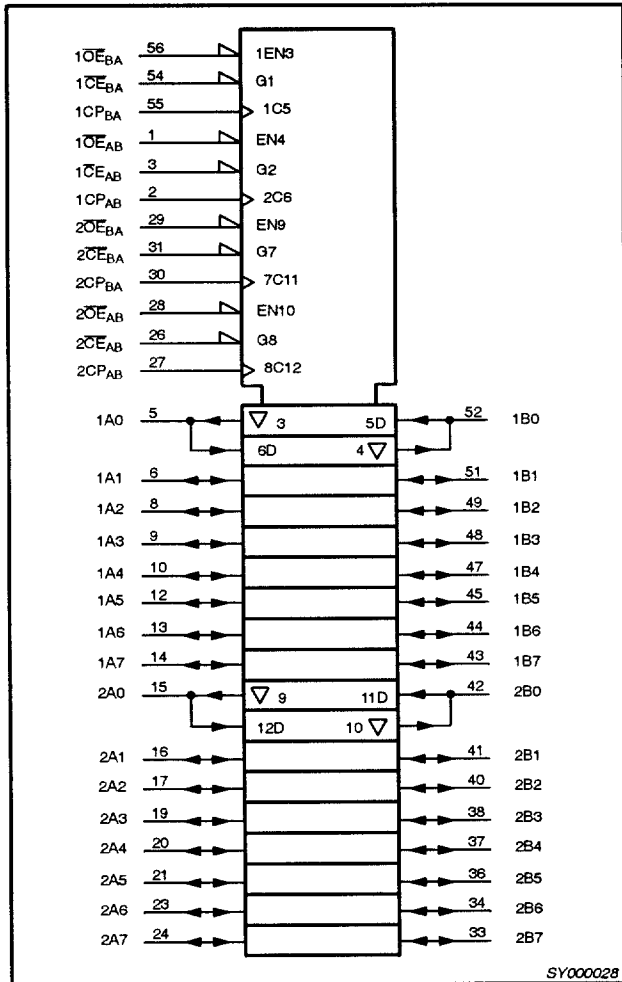


SY00027

16-bit registered transceiver (3-State)

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LOGIC SYMBOL (IEEE/IEC)



SY000028

16-bit registered transceiver (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 2.3$ to $3.0V$ $V_{CC} = 3.0$ to $3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For control pins ¹	-0.5 to +4.6	V
		For data inputs ¹	-0.5 to $V_{CC} + 0.5$	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	600	

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 2.3 to 2.7V	1.7	1.2		V
		V _{CC} = 2.7 to 3.6V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 2.3 to 2.7V		1.2	0.7	V
		V _{CC} = 2.7 to 3.6V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} -0.3	V _{CC} -0.08		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.6	V _{CC} -0.26		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.5	V _{CC} -0.14		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.6	V _{CC} -0.09		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} -1.0	V _{CC} -0.28		
V _{OL}	LOW level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.07	0.40	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.15	0.70	V
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.14	0.40	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA		0.27	0.55	
I _I	Input leakage current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND		0.1	5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 2.7 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	μA
I _{CC}	Quiescent supply current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0		0.2	40	μA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.3V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		150	750	μA
I _{BHL}	Bus hold LOW sustaining current	V _{CC} = 2.3V; V _I = 0.7V ²	45	-		μA
		V _{CC} = 3.0V; V _I = 0.8V ²	75	150		
I _{BHH}	Bus hold HIGH sustaining current	V _{CC} = 2.3V; V _I = 1.7V ²	-45			μA
		V _{CC} = 3.0V; V _I = 2.0V ²	-75	-175		
I _{BHLO}	Bus hold LOW overdrive current	V _{CC} = 3.6V ²	500			μA
I _{BHHO}	Bus hold HIGH overdrive current	V _{CC} = 3.6V ²	-500			μA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

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AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGEGND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP	MAX	
t_{PLH}/t_{PHL}	Propagation delay nCP _{AB} to nBn, nCP _{BA} to nAn	3	1.0		4.1	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nAn, nBn	4	1.0		5.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nAn, nBn	4	1.0		5.3	ns
t_W	Pulse width HIGH or LOW nCP _{AB} , nCP _{BA}	3	3.3			ns
t_{SU}	Set up time An or Bn before CP _{AB}	3	1.7			ns
	Set up time CE _{AB} or CE _{BA} before CP _{AB}	3	1.2			
t_H	Hold time An or Bn after CP _{AB}	3	0.6			ns
	Hold time An or Bn after CP _{AB}	3	1.1			
F_{max}	Maximum clock pulse frequency	3	150			MHz

NOTE:1. All typical values are at $V_{CC} = 2.5V$ and $T_{amb} = 25^\circ C$.**AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$** GND = 0V; $t_r = t_f = 2.5ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP _{AB} to nBn, nCP _{BA} to nAn	1, 4	1.0		3.9	1.0		4.6	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nAn, nBn	2, 4	1.0		4.4	1.0		5.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nAn, nBn	2, 4	1.1		4	1.4		4.4	ns
t_W	Pulse width HIGH or LOW nCP _{AB} , nCP _{BA}	3, 4	3.3			3.3			ns
t_{SU}	Set up time An or Bn before CP _{AB}	3, 4	1.5			1.9			ns
	Set up time CE _{AB} or CE _{BA} before CP _{AB}	3, 4	1			1			
t_H	Hold time An or Bn after CP _{AB}	3, 4	0.8			0.6			ns
	Hold time An or Bn after CP _{AB}	3, 4	1.1			0.9			
F_{max}	Maximum clock pulse frequency	1, 4	150			150			MHz

NOTES:1. All typical values are at $T_{amb} = 25^\circ C$.2. $V_{CC} = 3.3V$

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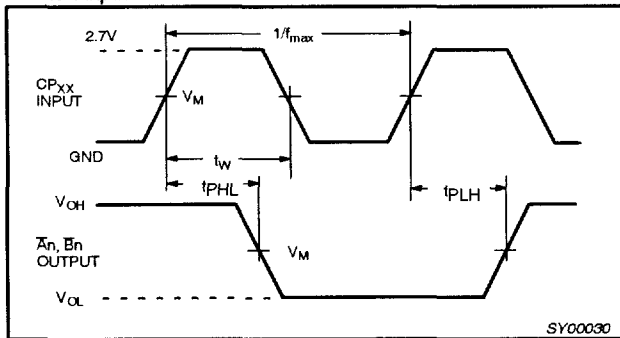
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

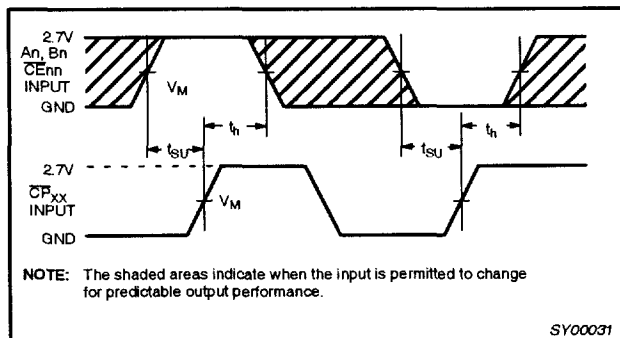
1. V_M = 0.5 V
2. V_X = V_{OL} + 0.15V
3. V_Y = V_{OH} - 0.15V
4. V_I = V_{CC}
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

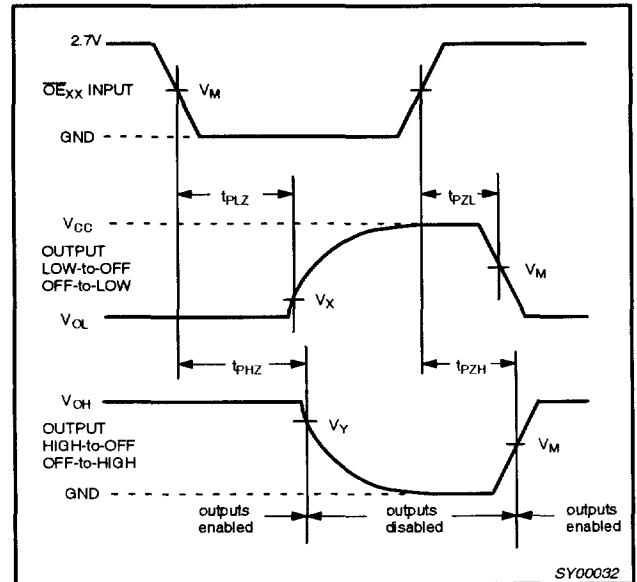
1. V_M = 1.5 V
2. V_X = V_{OL} + 0.3V
3. V_Y = V_{OH} - 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Clock input (CP_{BA}, CP_{AB}) to output (_B, _A) propagation delays, the clock pulse width and the maximum clock pulse frequency.

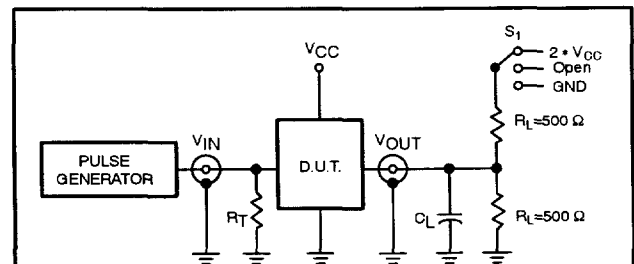


Waveform 2. Set-up and hold times for the _A, _B and _{CE} inputs.



Waveform 3. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	2 * V _{CC}
t _{PHZ} /t _{PZH}	GND

V _{CC}	V _{IN}
< 2.7V	V _{CC}
2.7 - 3.6V	2.7V

DEFINITIONS

- R_L = Load resistor
- C_L = Load capacitance includes jig and probe capacitance
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

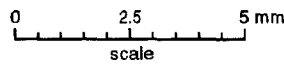
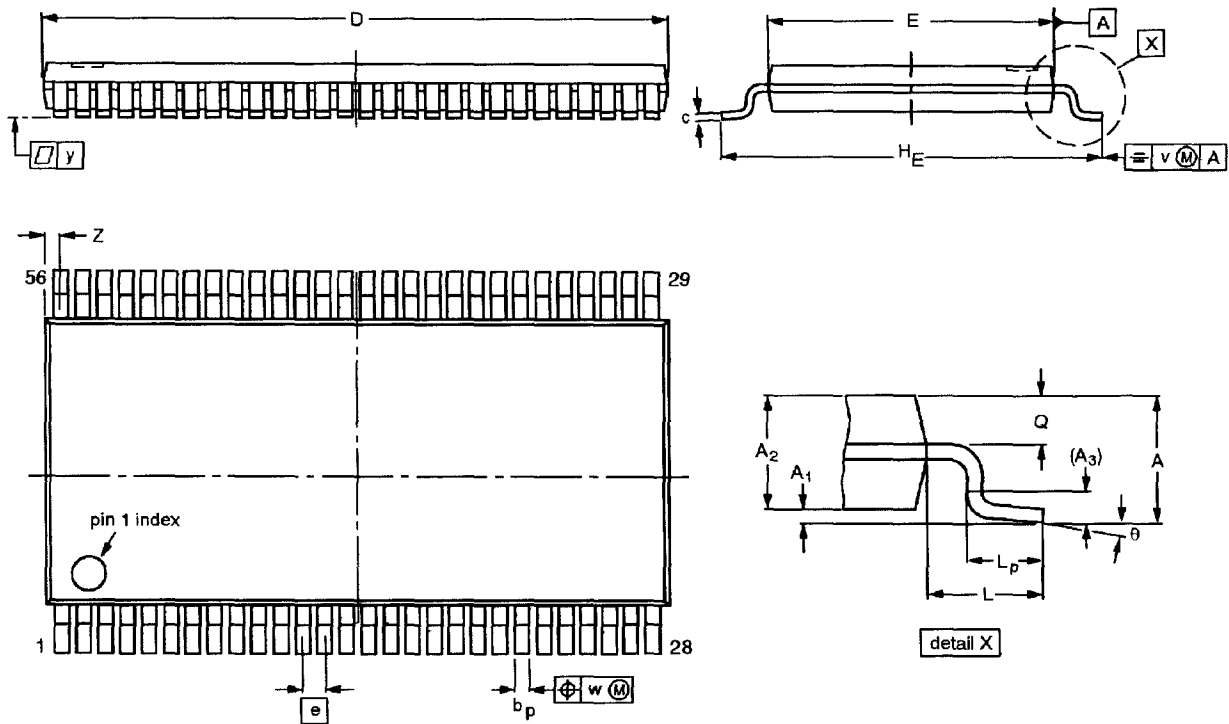
Load circuitry for switching times

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				99-02-09 95-02-10

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NOTES

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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Product Information

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Description

The 74ALVCH16952 consists of two section each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{XX} where X is AB or BA) provided that the clock enable (CE_{XX}) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input (OE_{XX}) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

Features

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductancemultiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50 Ohm transmission lines @ 85°C

Applications


 [Ground And VCC Bounce Of High-Speed Integrated Circuits](#) (date 01-Jan-93)

 [Interfacing 3 Volt and 5 Volt Applications](#)


 [Live Insertion Aspects of Philips Logic Families](#) (date 22-Jul-99)

 [Hardware and software verification procedure](#) (date 07-Oct-98)


Datasheet

<u>Type number</u>	<u>Title</u>	<u>Publication release date</u>	<u>Datasheet status</u>	<u>Page count</u>	<u>File size (kB)</u>	<u>Datasheet</u>
74ALVCH16952	16-bit registered transceiver (3-State)	01-Sep-98	Preliminary Specification	12	95	 Download

Products, packages, availability and ordering

<u>Type number</u>	<u>North American Type number</u>	<u>Order code (12nc)</u>	<u>marking/packing</u>  IC packing info	<u>package</u>	<u>device status</u>	<u>buy online</u>
74ALVCH16952DGG	74ALVCH16952DG	9352 628 01112	Standard Marking * Tube	SOT364-1 (TSSOP56)	Full production	order this -
	74ALVCH16952DG-T	9352 628 01118	Standard Marking * Reel Pack, SMD, 13"	SOT364-1 (TSSOP56)	Full production	order this -

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