TYPES SN54HCT189, SN54HCT219, SN74HCT189, SN74HCT219 64-BIT RANDOM-ACCESS MEMORIES WITH 3-STATE OUTPUTS

D2804, MARCH 1984

- **Inputs are TTL-Voltage Compatible**
- **Organized as 16 Words of Four Bits Each**
- **Choice of Noninverted or Inverted Outputs**
- **High-Current 3-State Inverting Outputs Can Drive up to 15 LSTTL Loads**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

Information to be stored in the memory is written into the selected address location when the chip-select ($\overline{S}$) and the write-enable ($R/\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off (Hi-Z). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by the other active outputs or a passive pull-up.

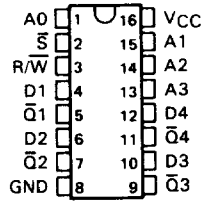
Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

The SN54HCT189 and SN54HCT219 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT189 and SN74HCT219 are characterized for operation from −40°C to 85°C.

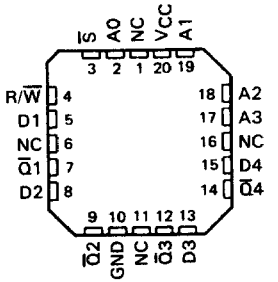
FUNCTION TABLE

FUNCTION	INPUTS		OUTPUTS	
	CHIP SELECT	WRITE ENABLE	'HCT189	'HCT219
Write	L	L	Z	Z
Read	L	H	Complement of data entered	Data entered
Inhibit	H	X	Z	Z

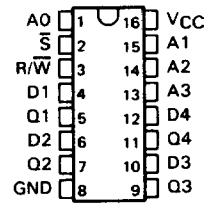
SN54HCT189 . . . J PACKAGE
SN74HCT189 . . . J OR N PACKABE
(TOP VIEW)



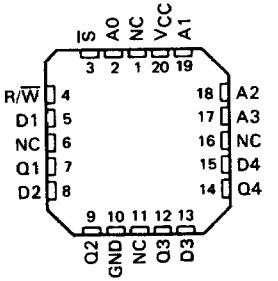
SN54HCT189 . . . FH OR FK PACKAGE
SN74HCT189 . . . FH OR FN PACKAGE
(TOP VIEW)



SN54HCT219 . . . J PACKAGE
SN74HCT219 . . . J OR N PACKAGE
(TOP VIEW)



SN54HCT219 . . . FH OR FK PACKAGE
SN74HCT219 . . . FH OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

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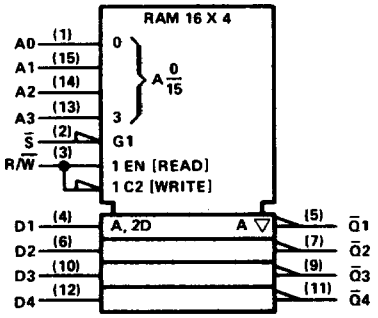
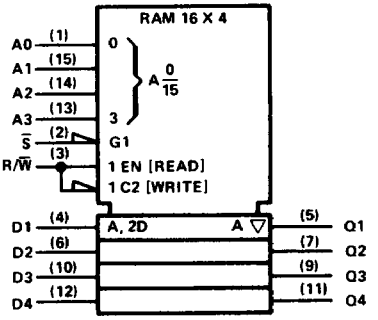
logic symbols

'HCT189



'HCT219



Pin numbers shown are for J and N packages.

maximum ratings, recommended operating conditions, and electrical characteristics

See Table VII, page 2-14.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT189 SN54HCT219		SN74HCT189 SN74HCT219		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, R/$\overline{W}$ low		4.5 V	55		80		70		ns
			5.5 V	50		75		63		
t_{su}	Setup time	Address before R/$\overline{W}$↓	4.5 V	0		0		0		ns
			5.5 V	0		0		0		
		Data before R/$\overline{W}$↑	4.5 V	55		80		70		ns
			5.5 V	50		75		63		
		Chip-select before R/$\overline{W}$↑	4.5 V	55		80		70		ns
			5.5 V	50		75		63		
t_h	Hold time	Address after R/$\overline{W}$↑	4.5 V	0		0		0		ns
			5.5 V	0		0		0		
		Data after R/$\overline{W}$↑	4.5 V	0		0		0		ns
			5.5 V	0		0		0		
		Chip-select after R/$\overline{W}$↑	4.5 V	0		0		0		ns
			5.5 V	0		0		0		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT189 SN54HCT219		SN74HCT189 SN74HCT219		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{a(ad)}$	A	Any	4.5 V		27						ns
			5.5 V		23						
$t_{a(S)}$	$\overline{S}$	Any	4.5 V		27						ns
			5.5 V		23						
t_{en}	R/$\overline{W}$	Any	4.5 V		16						ns
			5.5 V		14						
t_{dis}	$\overline{S}$	Any	4.5 V		8						ns
			5.5 V		7						
	R/$\overline{W}$	Any	4.5 V		11						
			5.5 V		10						
t_t		Any	4.5 V		12						ns
			5.5 V		11						

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	55 pF typ

NOTE 1: For load circuit and voltage waveforms, see page 1-14.

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