

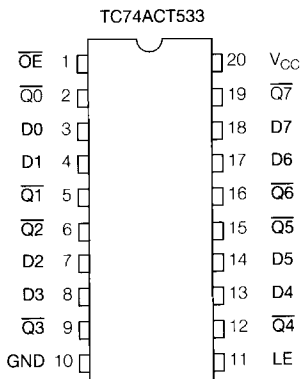
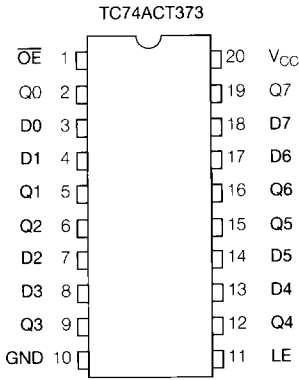
TC74ACT373, 533 Octal D-Type Latch with 3-State Output

373: Non-Inverting,
533: Inverting

Features:

- **High Speed:** $t_{pd} = 5.2\text{ns}$ (typ.) at $V_{CC} = 5\text{V}$
- **Low Power Dissipation:** $I_{CC} = 8\mu\text{A}$ (max.) at $T_a = 25^\circ\text{C}$
- **Compatible with TTL Outputs:** $V_{IL} = 0.8\text{V}$ (max.); $V_{IH} = 2.0\text{V}$ (min.)
- **Symmetrical Output Impedance:** $I_{OH}, I = I_{OL} = 24\text{mA}$ (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Pin and Function Compatible with 74F373/533**
- **ACT373 Available in DIP, SOIC, SOP and SSOP Packages**
- **ACT368 Available in DIP, SOIC and SOP Packages**

Pin Assignment



The TC74ACT373 and TC74ACT533 are advanced high speed CMOS OCTAL LATCHES with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to high speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The TC74ACT373 has non-inverting outputs, and TC74ACT533 has inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Truth Table

INPUTS			OUTPUTS	
\overline{OE}	LE	D	Q(373)	\overline{Q} (533)
H	X	X	Z	Z
L	L	X	Q_n	\overline{Q}_n
L	H	L	L	H
L	H	H	H	L

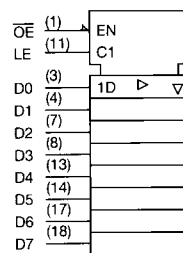
X: Don't care

Z: High Impedance

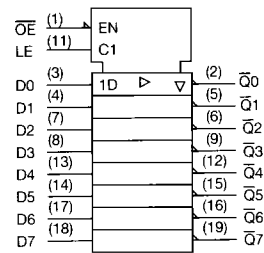
Q_n (\overline{Q}_n): Q (\overline{Q}) outputs are latched at the time when the LE input is taken to a low logic level.

IEC Logic Symbol

TC74ACT373



TC74ACT533



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5-7.0	V
DC Input Voltage	V_{IN}	-0.5- $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5- $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP) * /180 (SOP)	mW
Storage Temperature	T_{stg}	-65-150	$^{\circ}C$
Lead Temperature 10sec	T_L	300	$^{\circ}C$

* 500mW in the range of $T_a = -40^{\circ}C$ - $65^{\circ}C$.
From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of
-10mW/ $^{\circ}C$ should be applied up to 300mW.

Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5-5.5	V
Input Voltage	V_{IN}	0- V_{CC}	V
Output Voltage	V_{OUT}	0- V_{CC}	V
Operating Temperature	T_{opr}	-40-85	$^{\circ}C$
Input Rise and Fall Time	dt/dv	0-10	ns/v

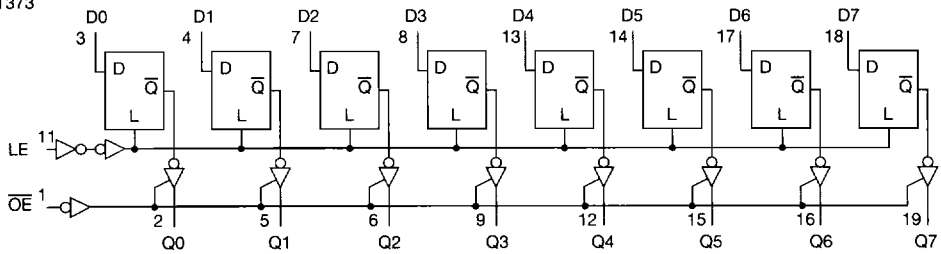
DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION	$T_a = 25^{\circ}C$			$T_a = -40$ - $85^{\circ}C$		UNIT		
			V_{CC}	Min.	Typ.	Max.	Min.		Max.	
High-Level Input Voltage	V_{IH}	—	4.5-5.5	2.0	—	—	2.0	—	V	
Low-Level Input Voltage	V_{IL}	—	4.5-5.5	—	—	0.8	—	0.8	V	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -24mA$	4.5	3.94	—	—	3.80	—	
			$I_{OH} = -75mA^*$	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu A$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 24mA$	4.5	—	—	0.36	—	0.44	
			$I_{OL} = 75mA^*$	5.5	—	—	—	—	1.65	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.5	—	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0	mA	
	ΔI_{CC}	Per input: $V_{CC} = 3.4V$ Other input: V_{CC} or GND	5.5	—	—	1.35	—	1.5		

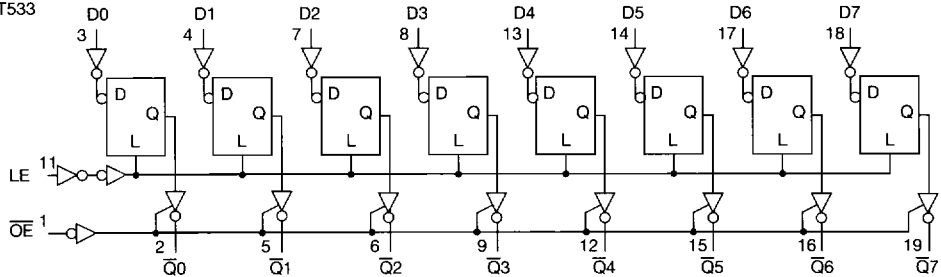
* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

System Diagram

TC74ACT373



TC74ACT533



Timing Requirements (Input $t_r = t_f = 3n$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40-85°		UNIT
			V _{CC}	Typ.	Max.	Max.	
Minimum Pulse Width (LE)	$t_{W(H)}$	—	5.0±0.5	—	5.0	5.0	ns
Minimum Set-up Time	t_s	—	5.0±0.5	—	2.0	2.0	
Minimum Hold Time	t_h	—	5.0±0.5	—	3.0	3.0	

AC Electrical Characteristics (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40-85°C		UNIT	
			V _{CC}	Min.	Typ.	Max.	Min.		Max.
Propagation Delay Time (LE-Q, Q)	t_{pLH}	—	5.0±0.5	—	5.8	9.2	1.0	ns	
	t_{pHL}	—	5.0±0.5	—	5.9	9.6	1.0		
Output Enable Time	t_{pZL}	—	5.0±0.5	—	6.5	10.5	1.0		12.0
	t_{pZH}	—	5.0±0.5	—	6.5	10.5	1.0		
Output Disable Time	t_{pLZ}	—	5.0±0.5	—	5.5	7.8	1.0		9.0
	t_{pHZ}	—	5.0±0.5	—	5.5	7.8	1.0		
Input Capacitance	C _{IN}	—	—	—	5	10	—	pF	
Output Capacitance	C _{OUT}	—	—	—	10	—	—		
Power Dissipation Capacitance	C _{PD} [†]	—	—	—	32	—	—		

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per Latch). And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation: C_{PD} (total) = 20 + 12 • n.