

INTERNATIONAL RECTIFIER

REPETITIVE AVALANCHE RATED AND dv/dt RATED

HEXFET[®] TRANSISTOR

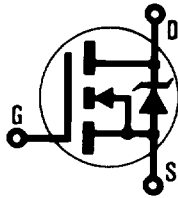
IRFM450

2N7228

JANTX2N7228

JANTXV2N7228

[REF: MIL-S-19500/592]



N-CHANNEL

500 Volt, 0.415 Ohm HEXFET

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies and virtually any application where military and/or high reliability is required.

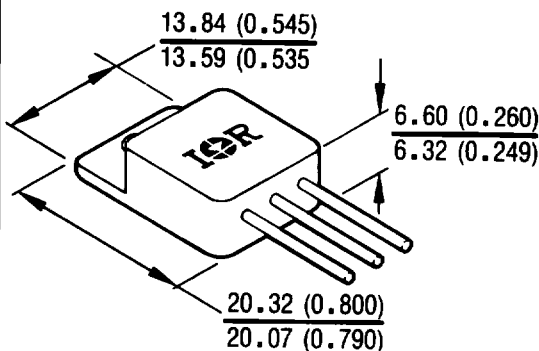
Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRFM450	500V	0.415 Ω	12A

FEATURES:

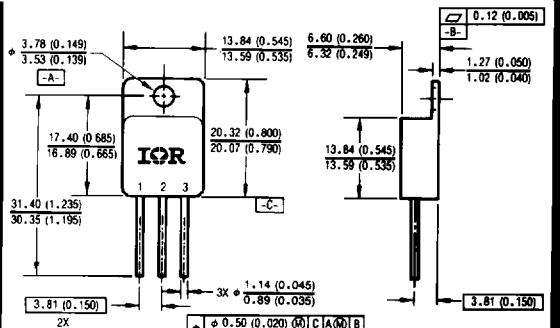
- Repetitive Avalanche Rating
- Isolated and Hermetically Sealed
- Alternative to TO-3 Package
- Simple Drive Requirements
- Ease of Paralleling
- Ceramic Eyelets

CASE STYLE AND DIMENSIONS



CAUTION

BERYLLIA WARNING PER MIL-S-19500
SEE PAGE I-364



LEGEND
1 DRAIN
2 SOURCE
3 GATE

NOTES
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
2 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Conforms to JEDEC Outline TO-254AA*
Dimensions in Millimeters and (Inches)

*For leadform configurations see page I-364, fig. 15



Absolute Maximum Ratings

Parameter	IRFM450, JANTXV-, JANTX-, 2N7228	Units
$I_D @ V_{GS} = 10V, T_C = 25^\circ C$ Continuous Drain Current	12	A
$I_D @ V_{GS} = 10V, T_C = 100^\circ C$ Continuous Drain Current	8.0	
I_{DM} Pulsed Drain Current ①	48	
$P_D @ T_C = 25^\circ C$ Max. Power Dissipation	150	W
	Linear Derating Factor	1.2
V_{GS} Gate-to-Source Voltage	± 20	V
E_{AS} Single Pulse Avalanche Energy ②	750	mJ
I_{AR} Avalanche Current ①	12	A
E_{AR} Repetitive Avalanche Energy ①	15	mJ
dv/dt Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J Operating Junction Temperature Range	-55 to 150	°C
Lead Temperature	300 (0.063 in. (1.6 mm) from case for 10s)	
Weight	9.3 (typical)	g


Electrical Characteristics @ $T_J = 25^\circ C$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 1.0 \text{ mA}$
$\Delta BV_{DSS}/\Delta T_J$ Temperature Coefficient of Breakdown Voltage	—	0.68	—	V/°C	Reference to $25^\circ C, I_D = 1.0 \text{ mA}$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance	—	—	0.415	Ω	$V_{GS} = 10V, I_D = 8.0A$ ④
	—	—	0.515		
$V_{GS(th)}$ Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
g_{fs} Forward Transconductance	6.5	—	—	S (Ω)	$V_{DS} \geq 15V, I_{DS} = 8.0A$ ④
I_{DSS} Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}, V_{GS} = 0V$
	—	—	250		$V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS} Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS} Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_g Total Gate Charge	55	—	120	nC	$V_{GS} = 10V, I_D = 12A$
Q_{gs} Gate-to-Source Charge	5.0	—	19		$V_{DS} = 0.5 \times \text{Max. Rating}$
Q_{gd} Gate-to-Drain ("Miller") Charge	27	—	70		See Fig. 6 and 14
$t_{d(on)}$ Turn-On Delay Time	—	—	35	ns	$V_{DD} = 250V, I_D = 12A, R_G = 2.35\Omega$ See Fig. 11
t_r Rise Time	—	—	190		
$t_{d(off)}$ Turn-Off Delay Time	—	—	170		
t_f Fall Time	—	—	130		
L_D Internal Drain Inductance	—	8.7	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	—	8.7	—		Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	—	2700	—	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1.0 \text{ MHz}$ See Fig. 5
C_{oss} Output Capacitance	—	600	—		
C_{rss} Reverse Transfer Capacitance	—	240	—		
C_{DC} Drain-to-Case Capacitance	—	12	—		





Source-Drain Diode Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	—	—	12	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM} Pulsed Source Current (Body Diode) ①	—	—	48		
V_{SD} Diode Forward Voltage	—	—	1.7	V	$T_J = 25^\circ\text{C}$, $I_S = 12\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr} Reverse Recovery Time	—	—	1800	nS	$T_J = 25^\circ\text{C}$, $I_F = 12\text{A}$, $dI/dt \leq 100\text{ A}/\mu\text{s}$ ④
Q_{RR} Reverse Recovery Charge	—	—	14	μC	$V_{DD} \leq 50\text{V}$
t_{on} Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC} Junction-to-Case	—	—	0.83	K/W ⑤	Mounting surface flat, smooth, and greased Typical socket mount
R_{thCS} Case-to-Sink	—	0.21	—		
R_{thJA} Junction-to-Ambient	—	—	48		

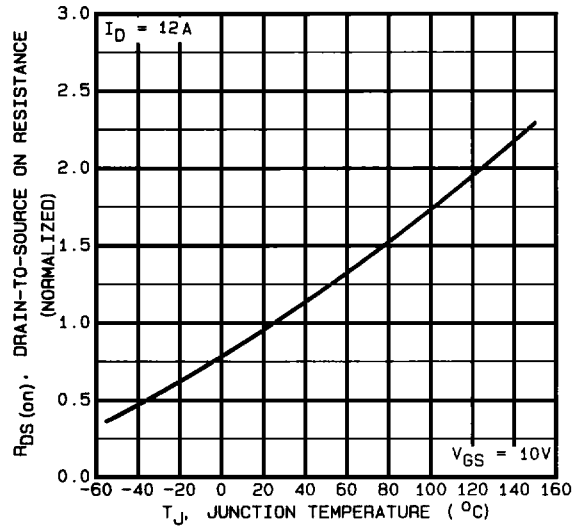
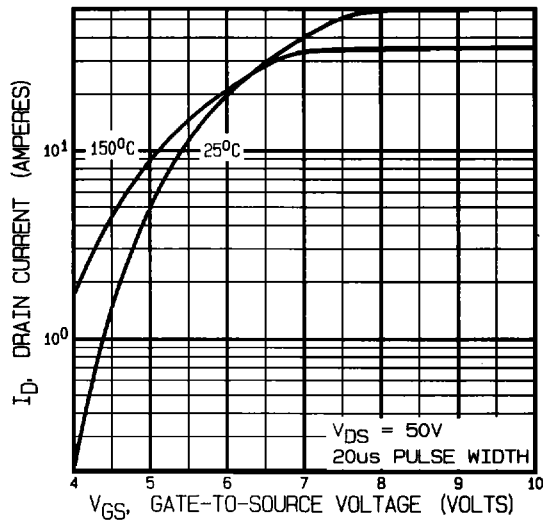
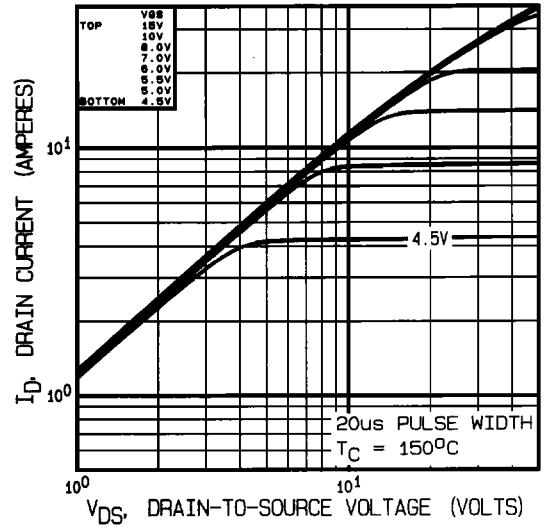
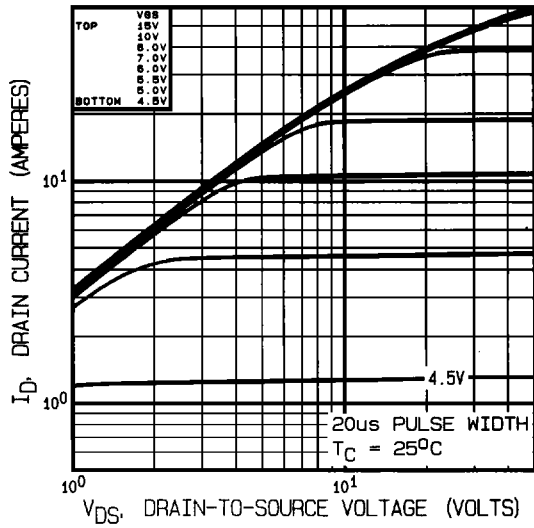
① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 9) Refer to current HEXFET reliability report

② @ $V_{DD} = 50\text{V}$, Starting $T_J = 25^\circ\text{C}$,
 $L \geq 9.4\text{ mH}$, $R_G = 25\Omega$,
Peak $I_L = 12\text{A}$

③ $I_{SD} \leq 12\text{A}$, $dI/dt \leq 130\text{ A}/\mu\text{s}$,
 $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ\text{C}$
Suggested $R_G = 2.35\Omega$

④ Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$

⑤ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$



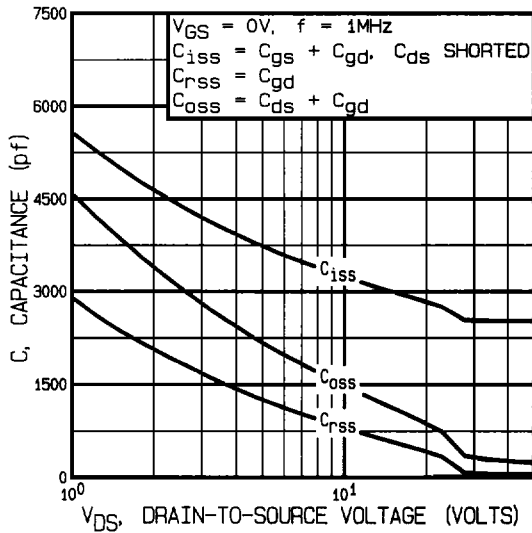


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

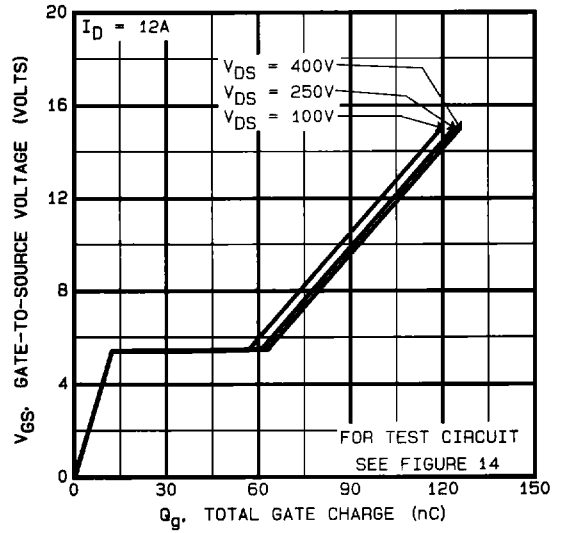


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

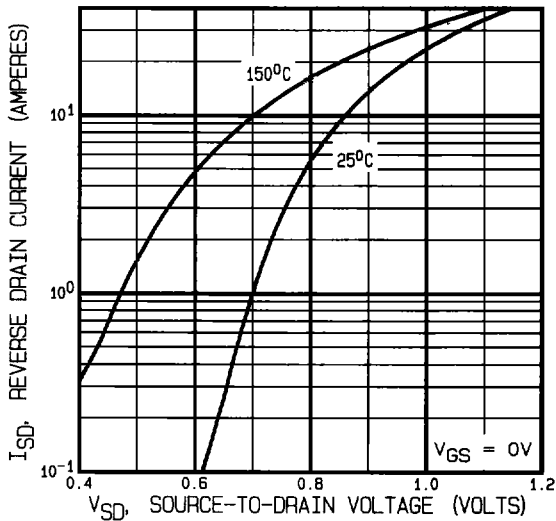


Fig. 7 — Typical Source-Drain Diode Forward Voltage

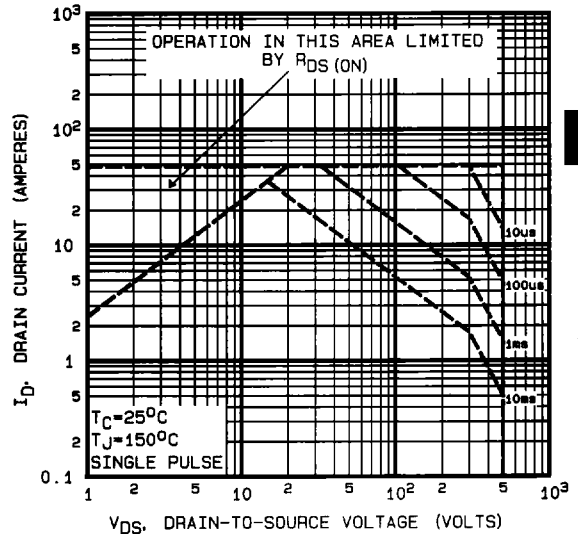


Fig. 8 — Maximum Safe Operating Area

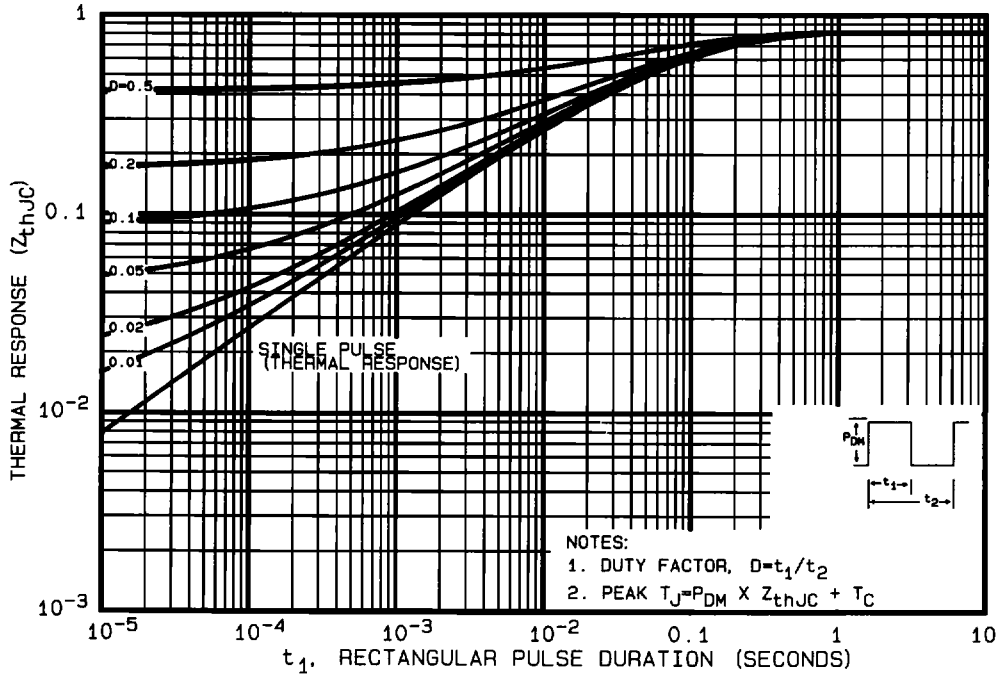


Fig. 9 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

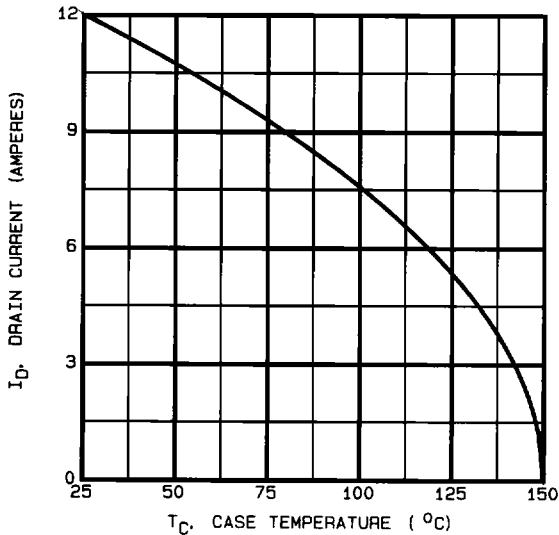


Fig. 10 — Maximum Drain Current Vs. Case Temperature

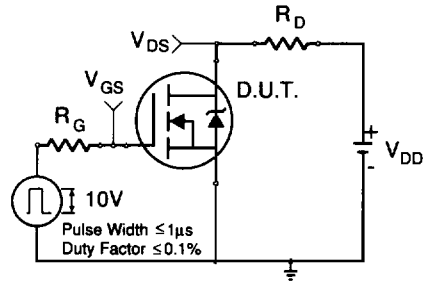


Fig. 11a — Switching Time Test Circuit

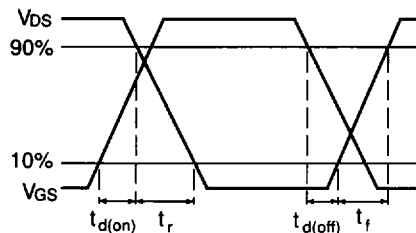


Fig. 11b — Switching Time Waveforms

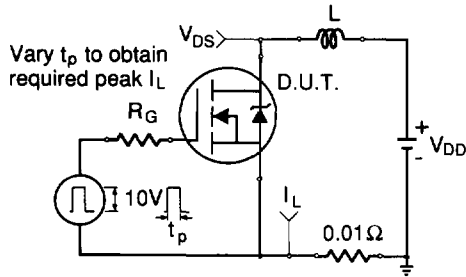


Fig. 12a — Unclamped Inductive Test Circuit

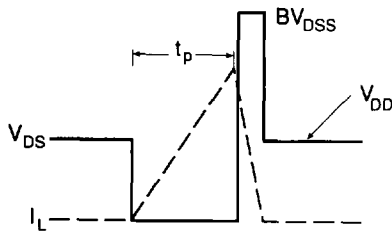


Fig. 12b — Unclamped Inductive Waveforms

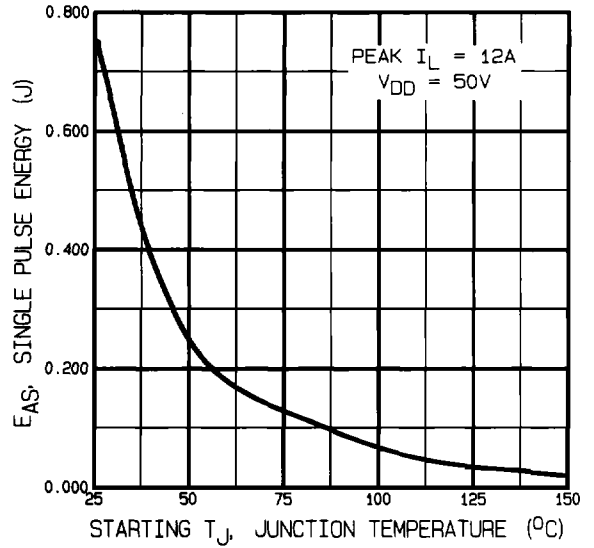


Fig. 12c — Maximum Avalanche Energy Vs. Starting Junction Temperature

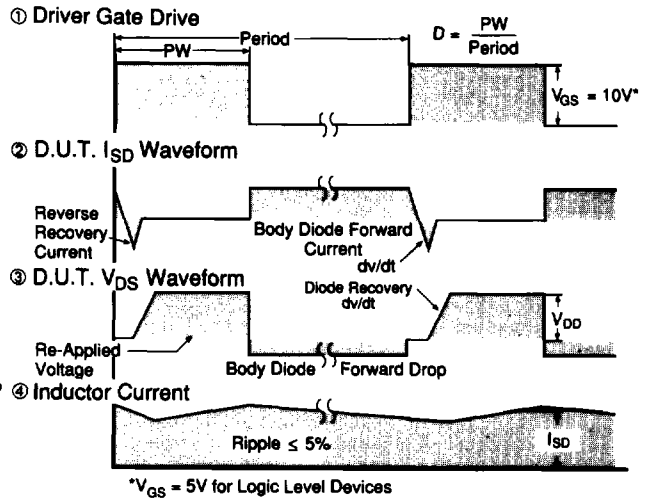
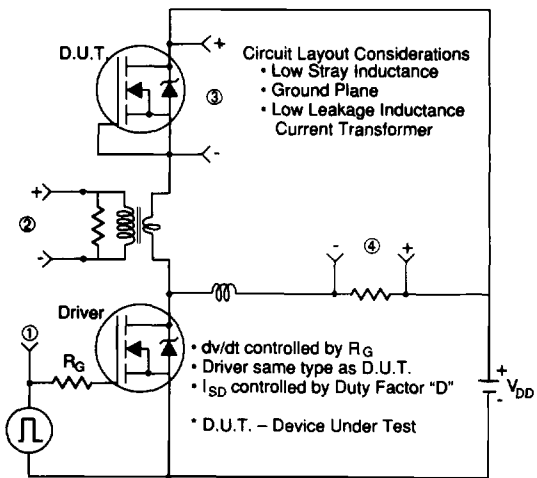


Fig. 13 — Peak Diode Recovery dv/dt Test Circuit

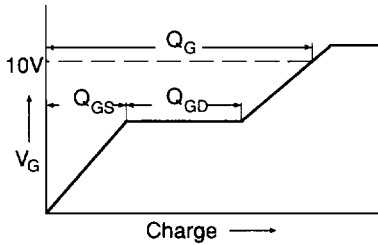


Fig. 14a — Basic Gate Charge Waveform

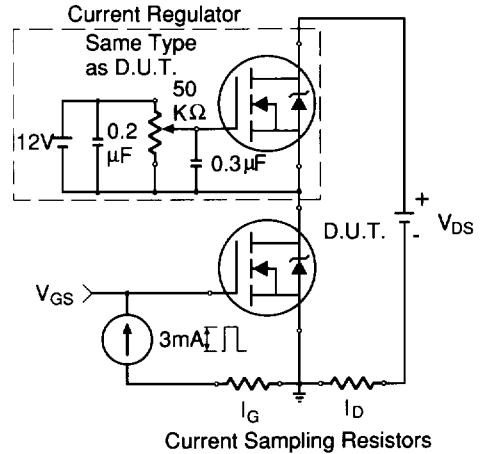


Fig. 14b — Gate Charge Test Circuit

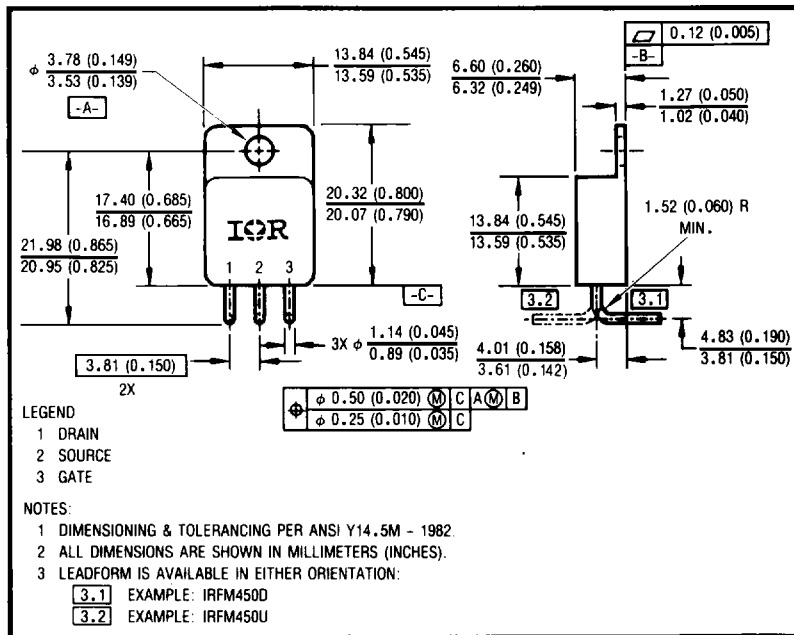


Fig. 15 — Optional Leadforms for Outline TO-254

BERYLLIA WARNING PER MIL-S-19500
 Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.