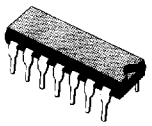
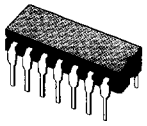
TRIPLE 3 INPUT OR GATE

- HIGH SPEED
  t_{PD} = 8 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4075B



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HC4075F1R M74HC4075M1R
M74HC4075B1R M74HC4075C1R

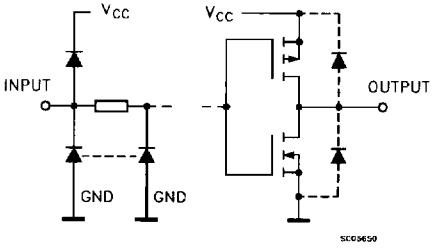
DESCRIPTION

The M54/74HC4075 is a high speed CMOS TRIPLE 3-INPUT OR GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

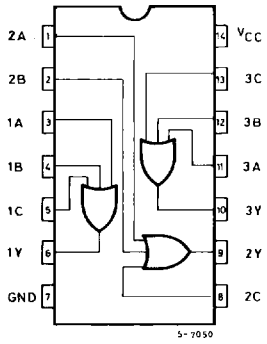
The internal circuit is composed of 4 stages including buffered output, which gives high noise immunity and a stable output.

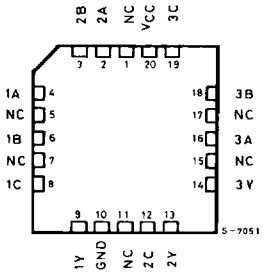
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



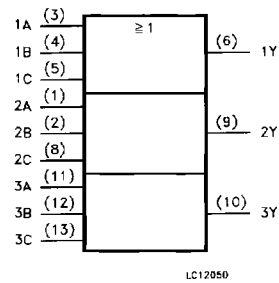


NC =
No Internal
Connection

TRUTH TABLE

A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

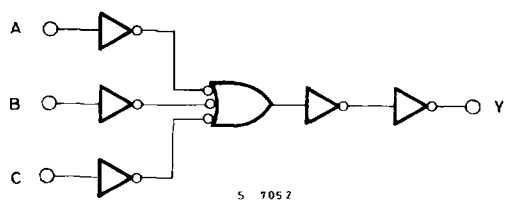
IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3, 1, 11	1A to 3A	Data Inputs
4, 2, 12	1B to 3B	Data Inputs
5, 8, 13	1C to 3C	Data Inputs
6, 9, 10	1Y to 3Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

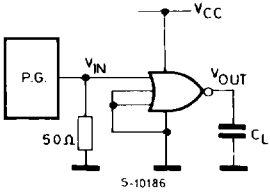
Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				1		10		20	µA

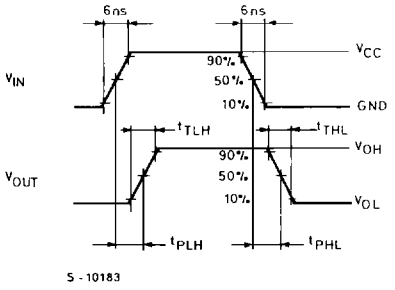
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Test Conditions V_{CC} (V)	Value T_A = 25 °C 54HC and 74HC Min.	Typ.	Max.	-40 to 85 °C 74HC Min.	Max.	-55 to 125 °C 54HC Min.	Max.	Unit
t_{TLH} t_{THL}	Output Transition Time	2.0		30	75		95		110	ns
		4.5		8	15		19		22	
		6.0		7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time	2.0		40	80		100		120	ns
		4.5		10	16		20		24	
		6.0		9	14		17		20	
C_{IN}	Input Capacitance			5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			24						pF

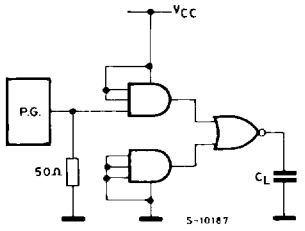
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT





TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.