The documentation and process conversion measures necessary to comply with this document shall be completed by 20 July 2007.

INCH-POUND

MIL-PRF-19500/558F
20 April 2007
SUPERSEDING
MIL-PRF-19500/558E
15 August 2005

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, UNITIZED, PNP, SILICON, SWITCHING,
FOUR TRANSISTOR ARRAY, TYPES 2N6987, 2N6987U, AND 2N6988,
JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, switching transistors, four independent chip array. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figures 1, 2, 3, and 4 (14-pin dual-in-line, 14-pin flat-pack, and 20-pin leadless chip carrier).

1.3 Maximum ratings, unless otherwise specified T_A = +25°C. (1)

	P_T T_A = +25°C (2)	P_T $T_{A(AM)}$ = +25°C (2)	$R_{\theta JA}$ (3)	$R_{\theta JA(AM)}$ (3)	V_{CBO} (4)	V_{EBO} (4)	V_{CEO} (4)	I_C (3)	T_J and T_{STG}
	W	W	°C/W	°C/W	V dc	V dc	V dc	mA dc	°C
2N6987	1.5	N/A	85	N/A	60	5	60	600	-65
2N6987U	1.0	N/A	160	N/A	60	5	60	600	to
2N6988	1.0	1.0	175	23	60	5	60	600	+200

(1) Maximum voltage between transistors shall be ≥ 500 V dc.
(2) For derating see figures 5, 6, 7, and 8.
(3) For thermal impedance graphs, see figures 9, 10, 11, and 12.
(4) Ratings apply to each transistor in the array.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

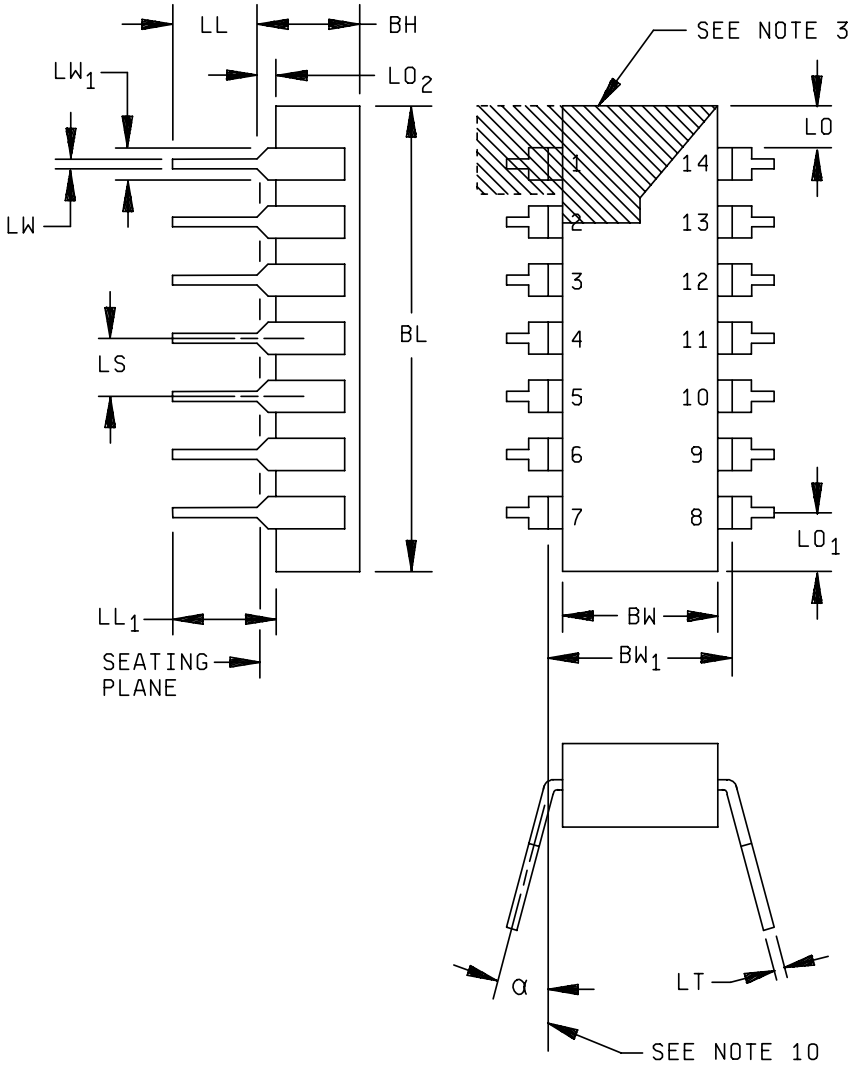


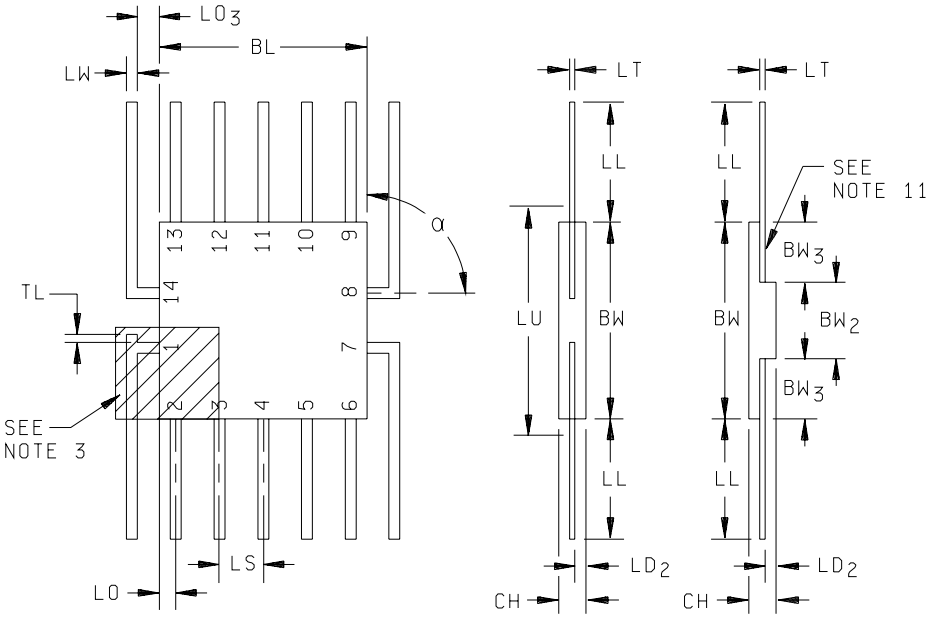
FIGURE 1. Dimensions and configuration for type 2N6987.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BH		.200		5.08	
LW	.014	.023	0.36	0.58	8
LW_1	.030	.070	0.76	1.78	4, 8
LT	.008	.015	0.20	0.38	8
BL		.785		19.94	4
BW	.220	.310	5.59	7.87	4
BW_1	.290	.320	7.37	8.13	7
LS	.100 BSC		2.54 BSC		5, 9
LL	.125	.200	3.18	5.08	
LL_1	.150		3.81		
LO_2	.015	.060	0.38	1.52	3
LO_1		.098		2.49	6
LO	.005		0.13		6
α	0°	15°	0°	15°	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Index area; a notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
4. The minimum limit for dimension LW_1 may be .023 inch (0.58 mm) for lead numbers 1, 7, 8, and 14 only.
5. Dimension LO_2 shall be measured from the seating plane to the base plane.
6. This dimension allows for off-center lid, meniscus, and glass overrun.
7. The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (±0.25 mm) of its exact longitudinal position relative to pins 1 and 14.
8. Applies to all four corners (lead numbers 1, 7, 8, and 14).
9. Lead center when α is 0 degrees. BW_1 shall be measured at the centerline of the leads.
10. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A is applied. Pointed or round lead ends are allowed.
11. Twelve spaces.
12. No organic or polymeric materials shall be molded to the bottom of the package to cover leads.
13. For terminal connections, see figure 4.
14. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Dimensions and configuration for type 2N6987 - Continued.



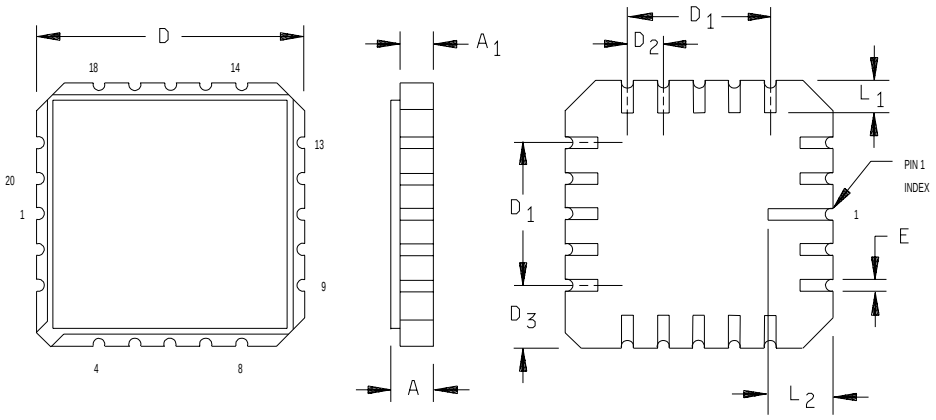
* FIGURE 2. Physical dimensions for type 2N6988.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.030	.115	0.76	2.92	
LW	.010	.019	0.25	0.48	7
TL	.008	.015	0.20	0.38	12
BL		.280		7.11	5
BW	.240	.260	6.10	6.60	
LU		.290		7.37	5
BW_2	.125		3.18		

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BW_3	.030		0.76		
LS	.050 BSC		1.27 BSC		6, 8
LT	.003	.006	0.076	0.152	7
LL	.250	.370	6.35	9.40	
LD_2	.005	.040	0.13	1.02	4
LO	.005		0.13		9, 10
LO_3	.004		`0.10		13
α	30°	90°	30°	90°	14

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Index area: A notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dim TL) may be used to identify pin one.
4. Dimension LD_2 shall be measured at the point of exit of the lead from the body.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within $\pm$.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
7. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat when the lead finish is solder.
8. Twelve spaces.
9. Applies to all four corners (leads number 2, 6, 9, and 13).
10. Dimension LO may be .000 inch (0.00 mm if leads number 2, 6, 9, and 13) bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body.
11. No organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
12. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
13. Applies to leads number 1, 7, 8, and 14.
14. Lead configuration is optional within dimension BW except dimensions LW and LT apply.
15. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
16. Pins 1, 7, 8, and 14 are collectors.
17. Pins 2, 6, 9, and 13 are bases.
18. Pins 3, 5, 10, and 12 are emitters.
19. Pins 4 and 11 are no contacts.

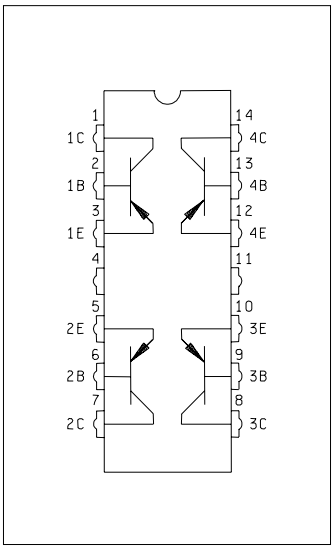
* FIGURE 2. Physical dimensions for type 2N6988 - Continued.



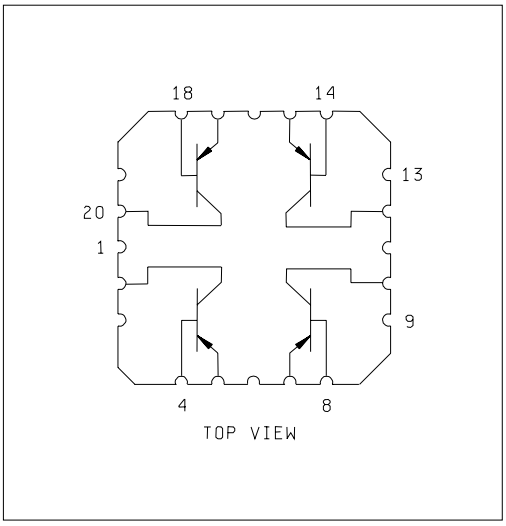
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.073	.085	1.85	2.16
A_1	.063	.075	1.60	1.90
D	.345	.355	8.76	9.02
D_1	.195	.205	4.95	5.21
D_2	.050 TYP		1.27 TYP	
D_3	.070	.080	1.76	2.03
E	.025 REF		0.64 REF	
L_1	.050 REF		1.27 REF	
L_2	.080	.090	2.03	2.28

NOTES:
1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 inch (0.13 mm).
4. For terminal connections, see figure 4.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 3. Physical dimensions for type 2N6987U.



14-lead flat-package or dual-in-line (top view)



20 pin leadless chip carrier (top view).

FIGURE 4. Schematic and terminal connections.

1.4 Primary electrical characteristics. Characteristics apply to each transistor in the array.

Limits	h_{FE2} (1) V_{CE} = 10 V dc I_C = 1.0 mA dc	h_{FE4} (1) V_{CE} = 10 V dc I_C = 150 mA dc	C_{obo} V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	Switching t_{on} see figure 13	Switching t_{off} see figure 14
			pF	ns	ns
Min	100	100			
Max	450	300	8	45	300

Limits	$\|h_{fe}\|$ V_{CE} = 20 V dc I_C = 50 mA dc f = 100 MHz	$V_{CE(sat)2}$ (1) I_C = 500 mA dc I_B = 50 mA dc	$V_{BE(sat)2}$ (1) I_C = 500 mA dc I_B = 50 mA dc
		V dc	V dc
Min	2.0		
Max	8.0	1.6	2.6

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1. General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2. Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3. Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

PCB	Printed circuit board.
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JA(AM)}$	Thermal resistance ambient (adhesive mount to PCB).
$T_{A(AM)}$	Temperature ambient (adhesive mount to PCB).

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1, 2, 3, and 4 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Schematic and terminal connections. The schematic and terminal connections shall be as shown on figure 4.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8. Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 appendix E, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see appendix E, table E-IV of MIL-PRF-19500)	Measurements	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750, see 4.3.2.	Thermal impedance, method 3131 of MIL-STD-750, see 4.3.2.
9	I_{CBO2} and h_{FE4}	Not applicable
10	24 hours minimum	24 hours minimum
11	I_{CBO2} and h_{FE4} ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent of initial value.	I_{CBO2} and h_{FE4}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent of initial value.	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent of initial value.
14	Required maximum leak rate = 1×10^{-7} atm cc/s Test condition C.	Required maximum leak rate = 1×10^{-7} atm cc/s Test condition C.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc; P_T = 1.5 W for 2N6987; P_T = 1.0 W for 2N6987U, and P_T = 1.0 W for 2N6988. T_A ambient rated as defined in 1.3. NOTE: No heat sink or forced air-cooling on the devices shall be permitted. Power ratings apply to total package. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed on each die in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit shall comply with the thermal impedance graph on figures 9, 10, 11, and 12 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131. See table II, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of table I, group A1 and group A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2 herein).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500 and 4.4.2.1 herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.5 herein, delta parameters apply to subgroups B4 and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.5 herein.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 V dc.
B5	1027	V_{CB} = 10 V dc, $P_D \geq$ 100 percent of max rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-Via, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS).and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.5 herein, delta parameters apply to subgroup C6.

4.4.3.1 Group C inspection, table E-VII (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, not applicable for U designation.
C6	1026	1,000 hours at V_{CB} = 10 - 30 V dc; T_J = +150°C minimum. No heat sink or forced-air cooling on device shall be permitted.

4.4.3.2 Group C inspection, table E-VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, not applicable for U designation.
C5	3131	$R_{\theta JA}$, see 1.3.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes group A tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Independent transistor inspections. Inspections shall be performed on each transistor in the array.

4.5.4 Transistor-to-transistor resistance. The leads of each transistor shall be shorted together for this test. The resistance shall be measured between each transistor in the array.

4.5.5 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 50 V dc	ΔI_{CB02} (1)	100 percent of initial value or ±8 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed see 4.5.1	Δh_{FE4} (1)	±25 percent change from initial reading.

(1) Devices which exceed the table I limits for this test shall not be accepted.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours. n = 11 wires, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to base, cutoff current	3036	V_{CB} = 60 V dc	I_{CBO1}		10	µA dc
Emitter to base, cutoff current	3061	V_{BE} = 5 V dc	I_{EBO1}		10	µA dc
Breakdown voltage collector to emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 50 V dc	I_{CBO2}		10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 4 V dc	I_{EBO2}		50	nA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 0.1 mA dc	h_{FE1}	75		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc	h_{FE2}	100	450	
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE3}	100		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc pulsed (see 4.5.1)	h_{FE4}	100	300	
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 500 mA dc pulsed (see 4.5.1)	h_{FE5}	50		
Collector to emitter voltage (saturated)	3071	I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.4	V dc
Collector to emitter voltage (saturated)	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.6	V dc
Base to emitter saturated voltage	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.3	V dc
Base to emitter saturated voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.6	V dc
Subgroup 3						
High temperature operation:		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 50 V dc	I_{CBO3}		10	µA dc
Low temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc	h_{FE6}	50		

See footnotes at end of table.

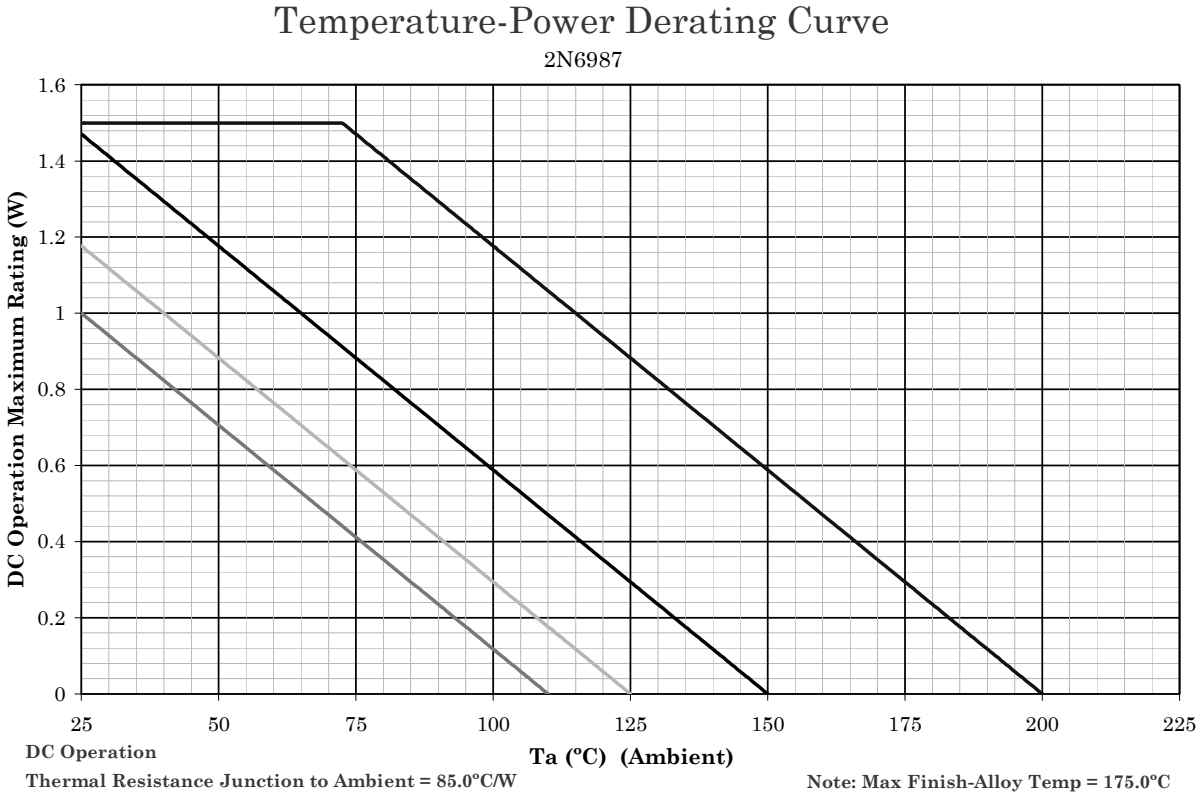
TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{fe}	100		
Magnitude of small-signal short-circuit forward- current transfer ratio	3306	V_{CE} = 20 V dc; I_C = 50 mA dc; f = 100 MHz	$\|h_{fe}\|$	2.0	8.0	
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		8.0	pF
Input capacitance (output open-circuited)	3240	V_{EB} = 2.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz; see 4.5.2	C_{ibo}		30	pF
Turn-on time		See figure 13	t_{on}		45	ns
Turn-off time		See figure 14	t_{off}		300	ns
Transistor-to-transistor resistance		$\|V_{T-T}\|$ = 500 V dc; see 4.5.4	R_{T-T}	10^{10}		ohms
Subgroups 5 and 6						
Not applicable						
Subgroups 7						
Decap internal visual (design verification)	2075	n = 1 device, c = 0				

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in group A, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.

* TABLE II. Group E inspection (all quality levels) - for qualification only.

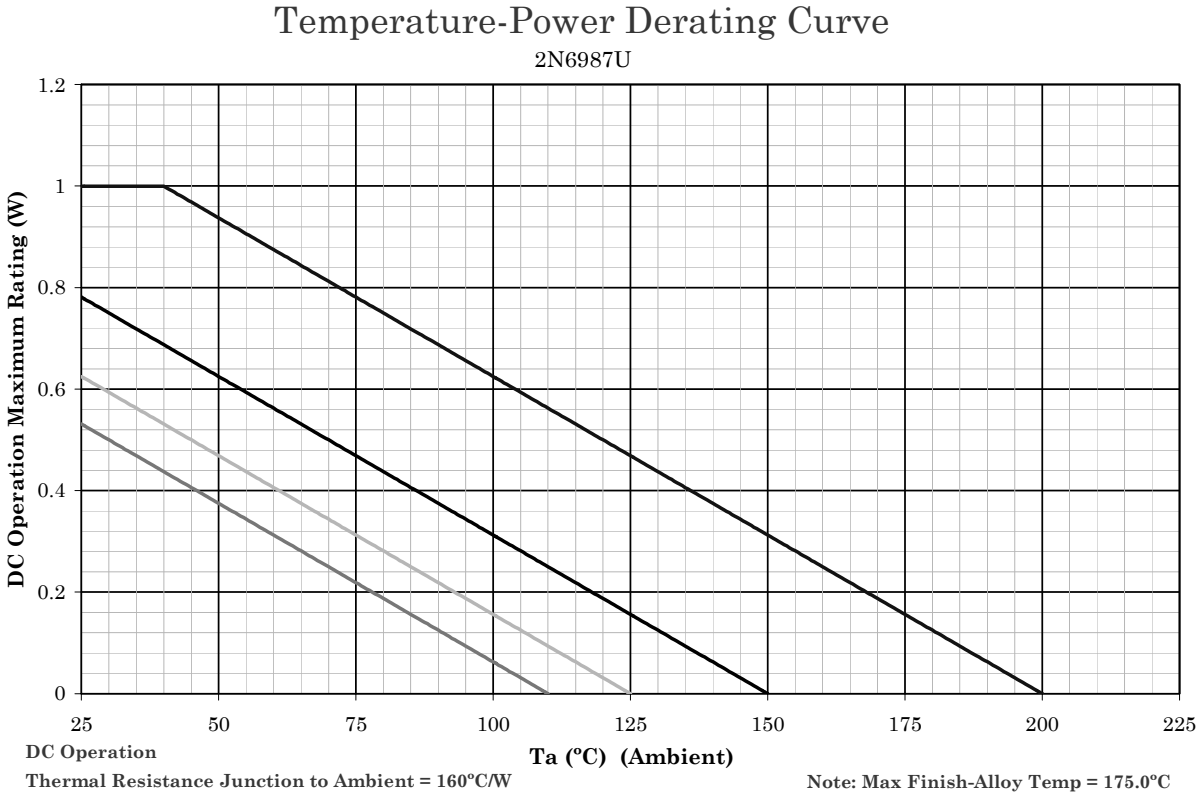
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.5 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 - 30 V dc , 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and 4.5.5 herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500.	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			3 devices c = 0
ESD	1020		
Subgroup 7			
Not applicable			
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B	



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

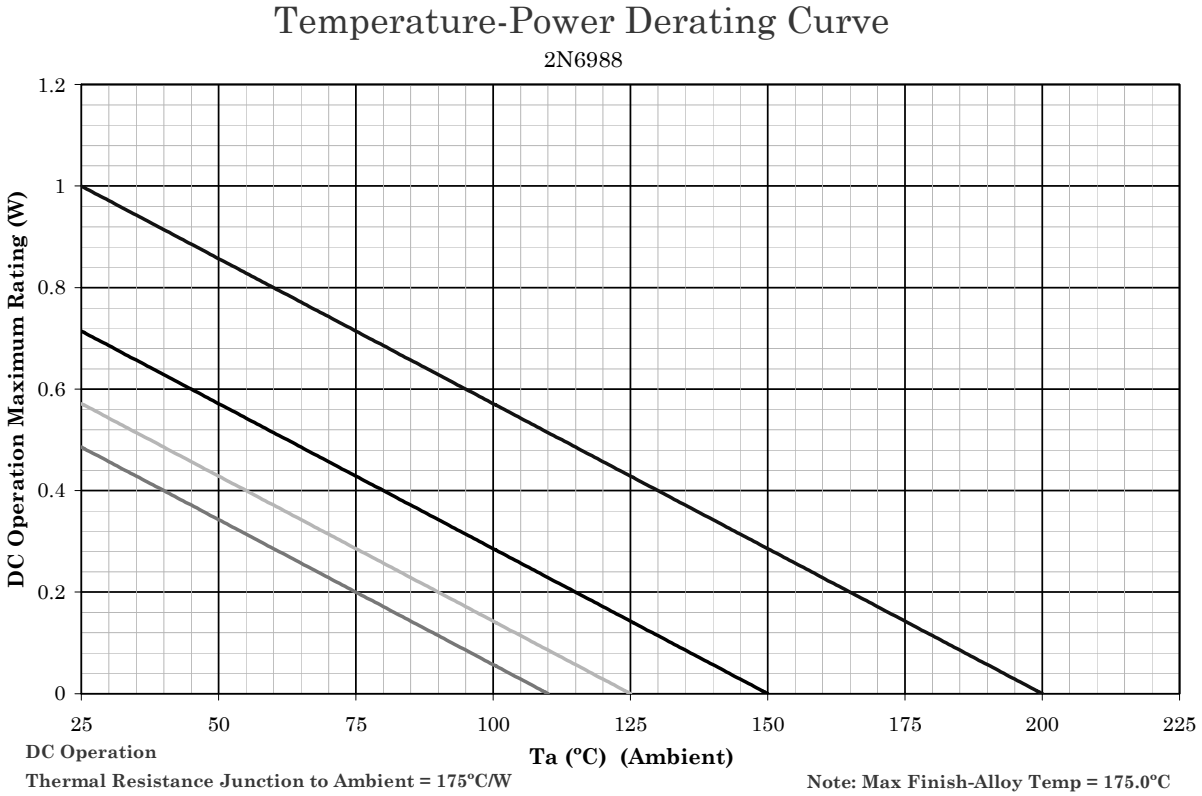
FIGURE 5. Temperature-power derating ($R_{\theta JA}$) for 2N6987 (DIP14).



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

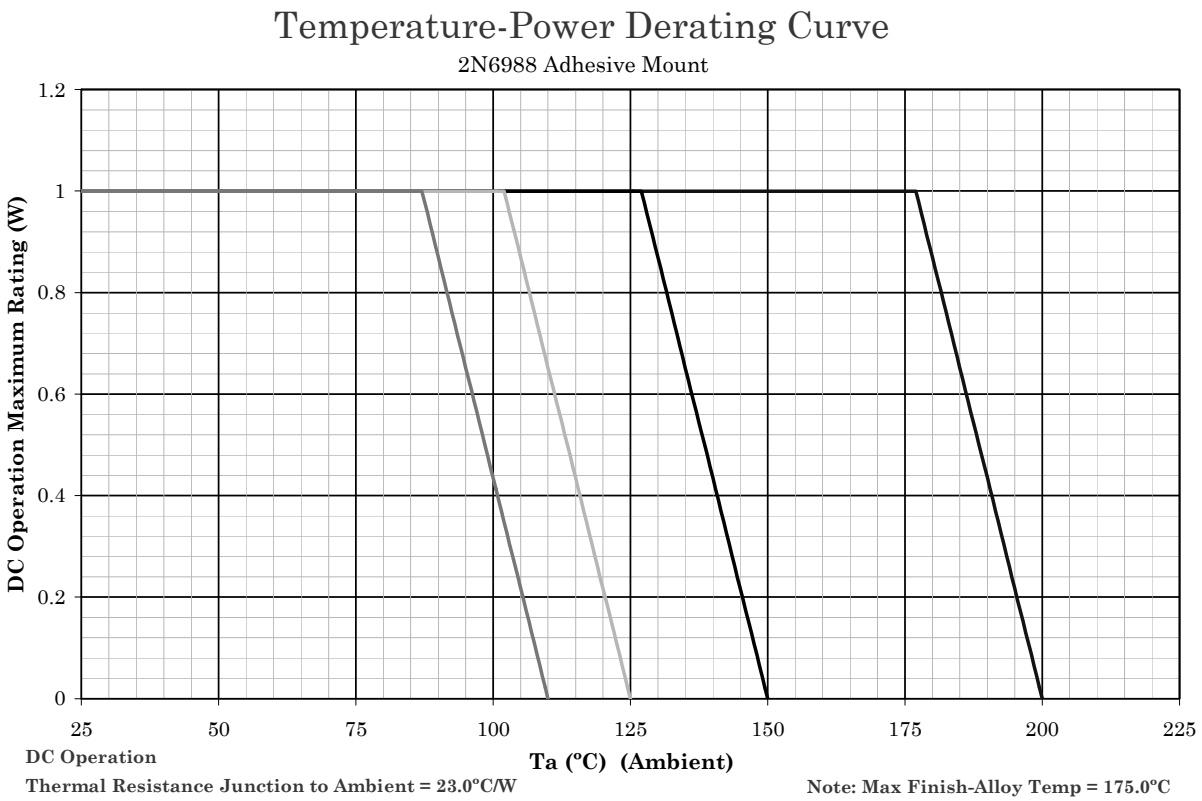
FIGURE 6. Temperature-power derating ($R_{\theta JA}$) for 2N6987U, (20 pin leadless chip).



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 7. Temperature-power derating ($R_{\theta JA}$) for 2N6988 (14 pin flat pack).



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125°C$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 8. Temperature-power derating ($R_{\theta JA(AM)}$) for 2N6988 (14 pin flat pack epoxy mount).

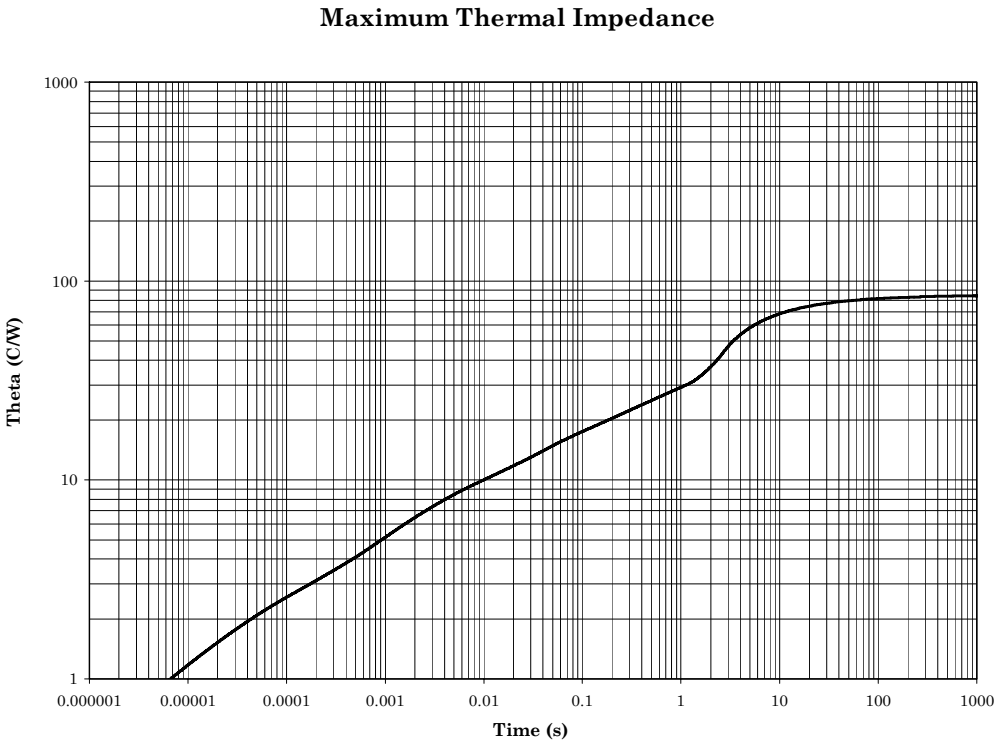


FIGURE 9. Thermal impedance graph ($R_{\theta JA}$) for 2N6987 (DIP14).

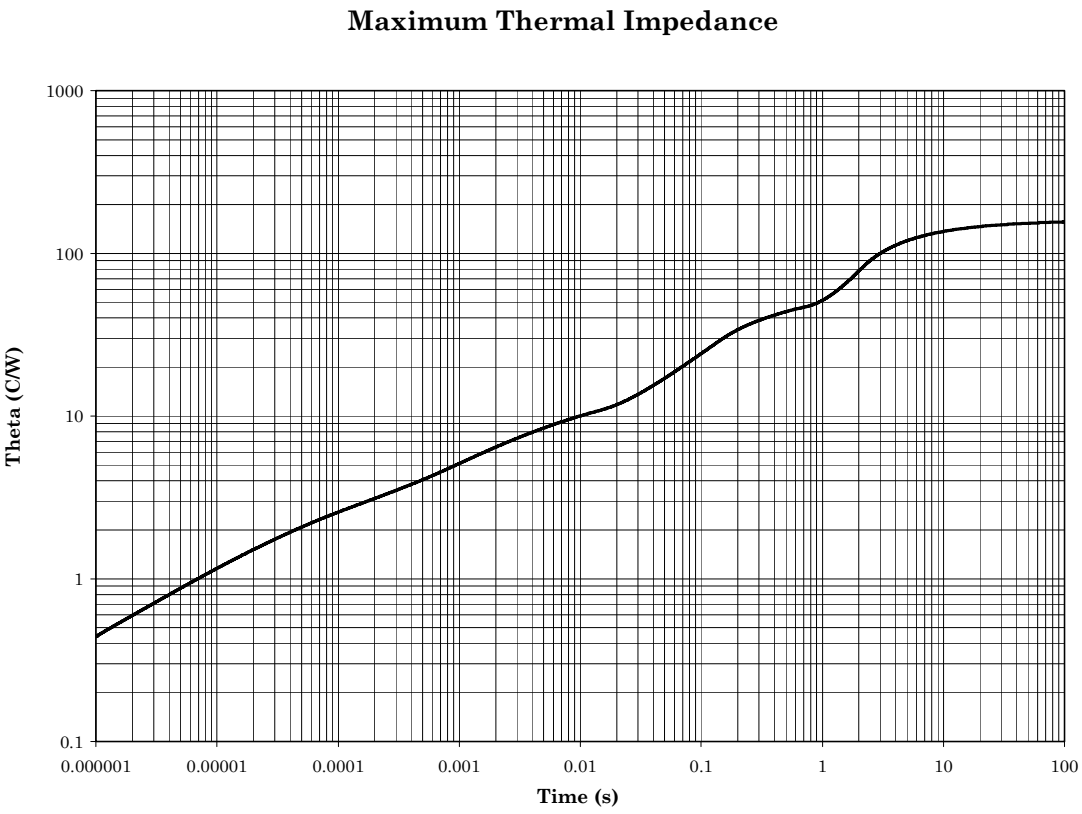


FIGURE 10. Thermal impedance graph ($R_{\theta JA}$) for 2N6987U (20 pin leadless chip).

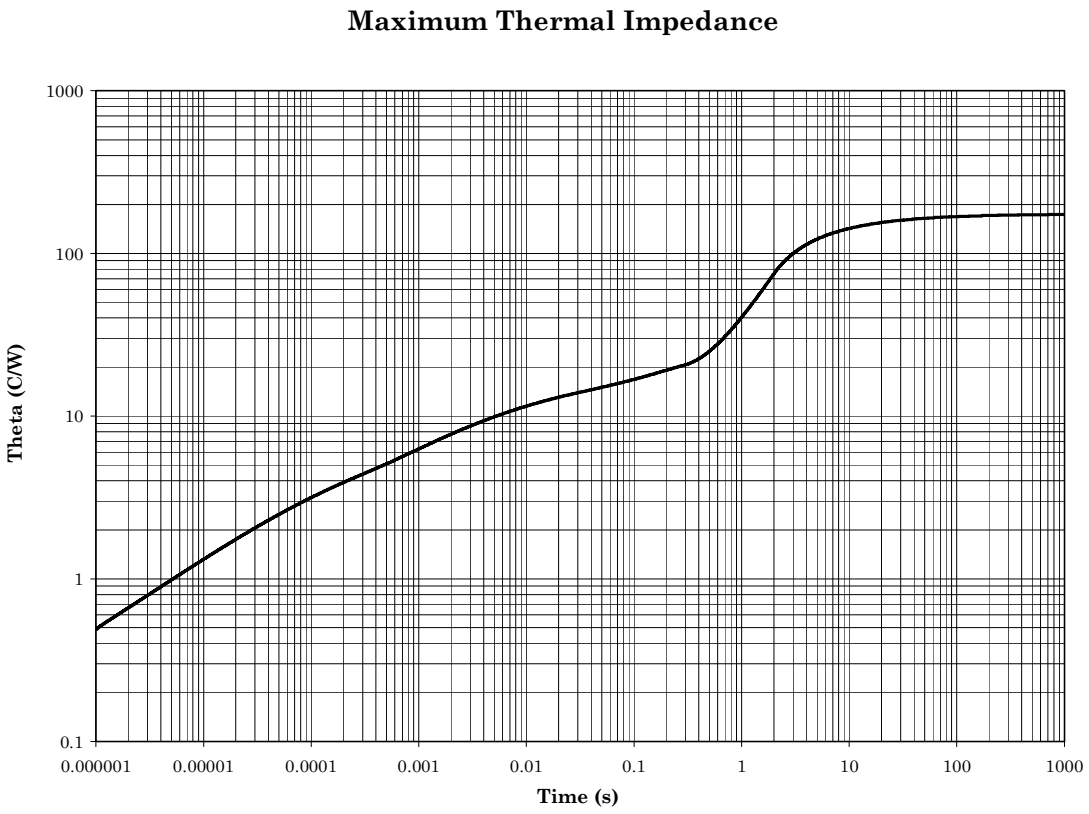


FIGURE 11. Thermal impedance graph ($R_{\theta JA}$) for 2N6988 (14 pin flat pack).

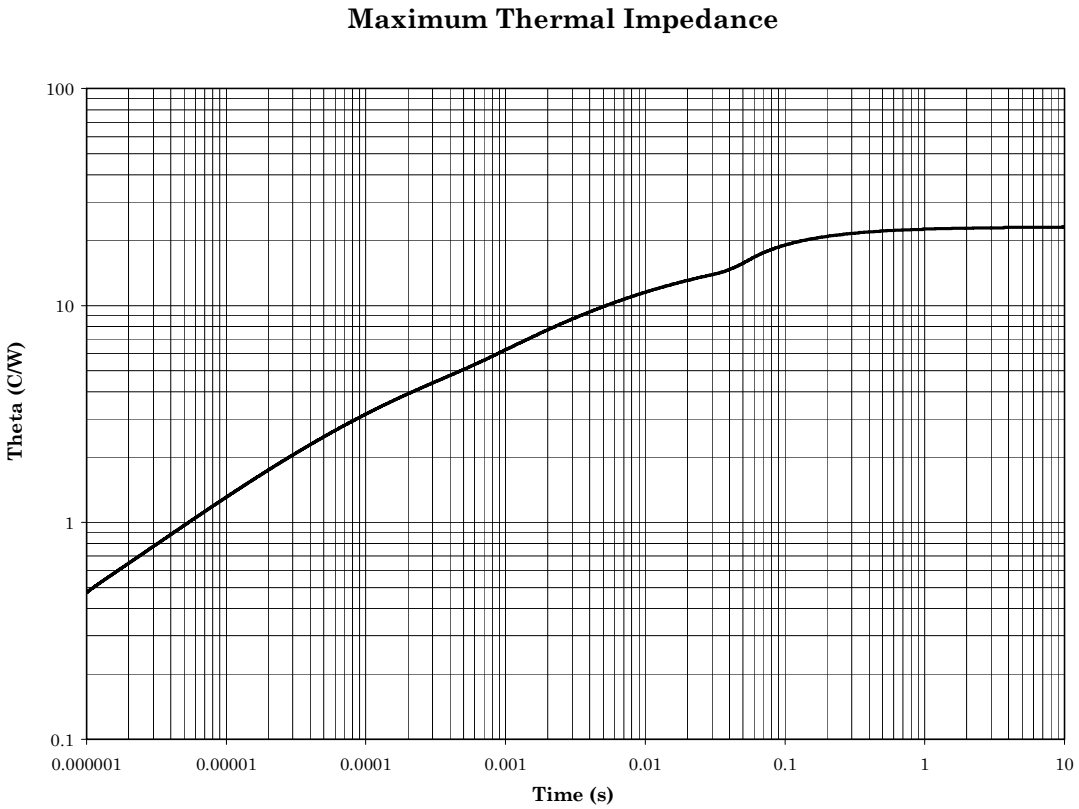
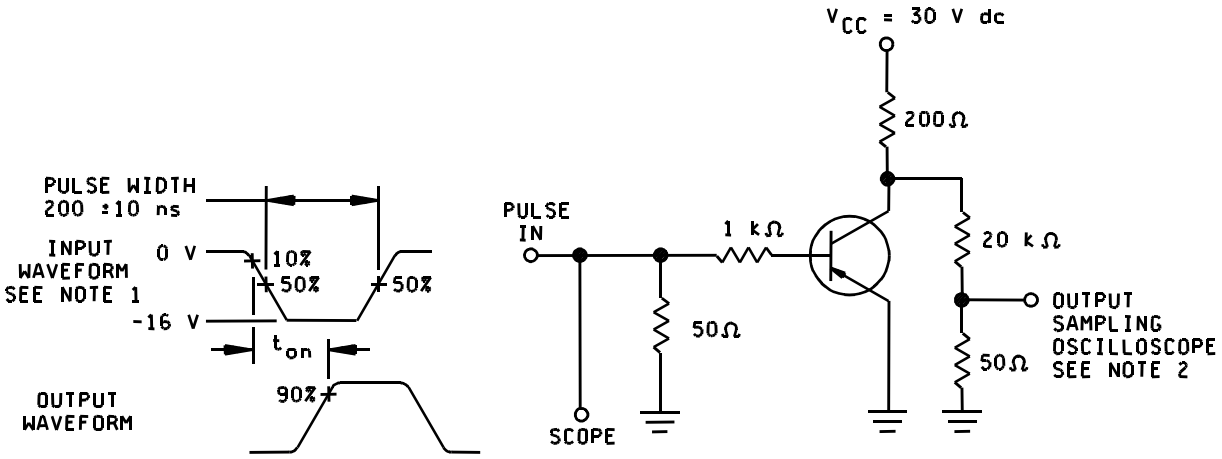


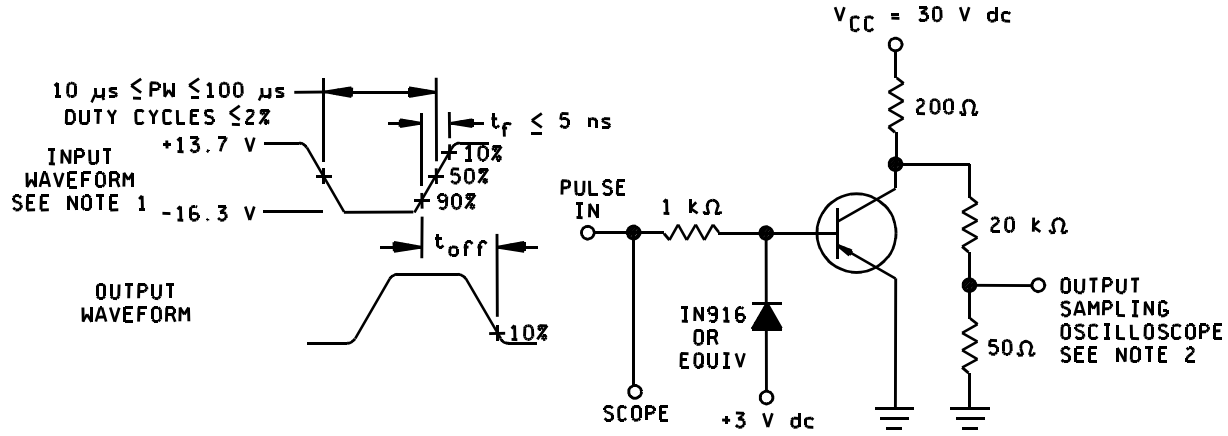
FIGURE 12. Thermal impedance graph ($R_{\theta JA}$) for 2N6988 (14 pin flat pack epoxy mount).



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 Ω.
2. Output sampling oscilloscope: Z_{in} ≥ 100 kΩ; C_{in} ≤ 12 pF; rise time ≤ 5.0 ns.

FIGURE 13. Saturated turn-on switching time test circuit and waveform.



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 2.0 ns; duty cycle ≤ 2 percent; generator source impedance shall be 50 Ω.
2. Output sampling oscilloscope: Z_{in} ≥ 100 kΩ; C_{in} ≤ 12 pF; rise time ≤ 5.0 ns.

FIGURE 14. Saturated turn-off switching time test circuit and waveform.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2007-014)

Review activities:
Army - AR, MI, SM
Navy - AS, MC
Air Force - 19, 71, 99

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