DECT Single-Chip Transceiver

Description

The T2801 is an RF IC for low-power DECT applications. The HP-VFQFP-N48-packaged IC is a complete transceiver including image rejection mixer, IF amplifier, FM demodulator, baseband filter, RSSI, TX preamplifier, power-ramping generator for power amplifiers, integrated synthesizer, fully integrated VCO, TX filter and modulation compensation circuit for advanced closed-loop modulation concept. No mechanical tuning is necessary in production.

Features

- Supply-voltage range 3 V to 4.6 V (unregulated)
- Auxiliary-voltage regulator on-chip
- Low current consumption
- Few low cost external components
- No mechanical tuning required
- Non-blindslot and blindslot operation
- Unlimited multislot operation with advanced closed-loop modulation (13.824 MHz/ 27.648 MHz and 10.368 MHz/ 20.736 MHz)
- TX preamplifier with 0 dBm output power at 1.9 GHz and ramp-signal generator for SiGe power amplifier

Block Diagram

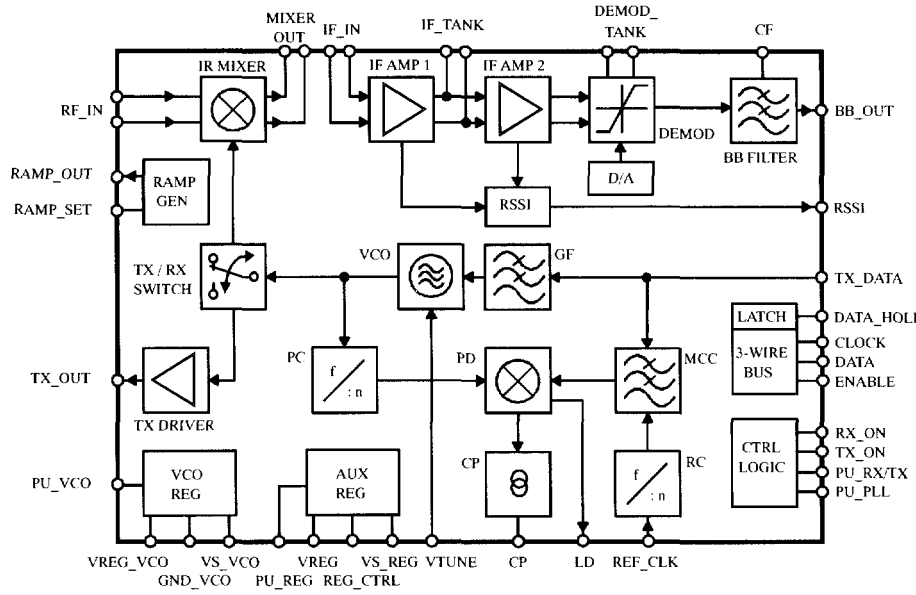


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
T2801-PLT	HP-VFQFP-N48	Tray
T2801-PLQ	HP-VFQFP-N48	Taped and reeled

Pin Description

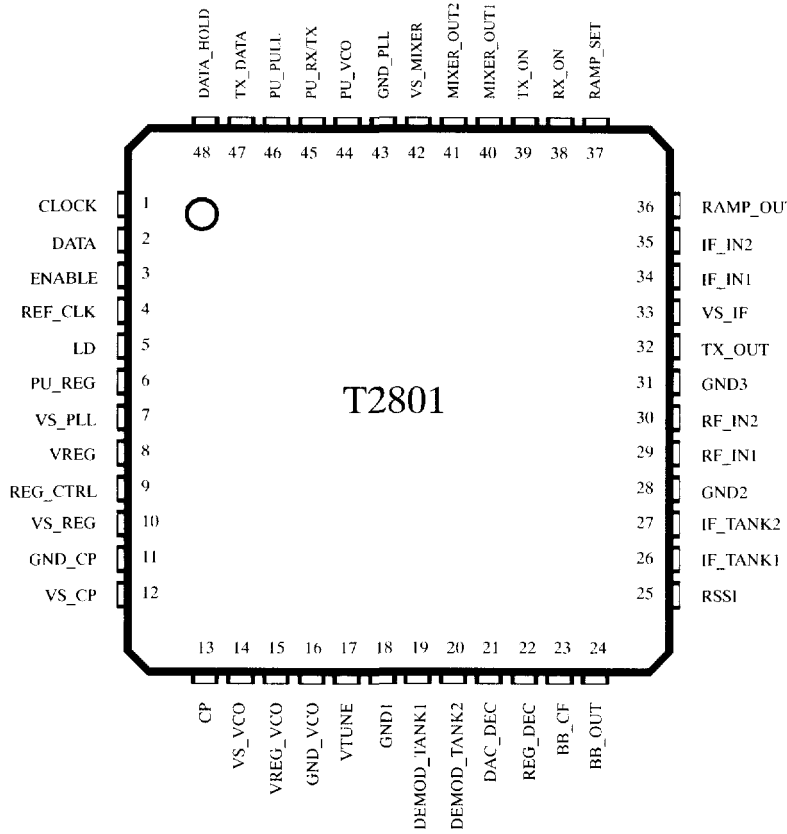
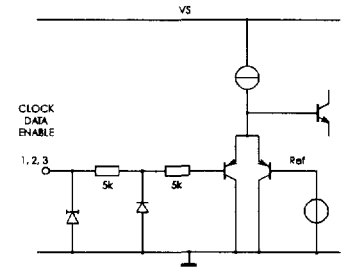
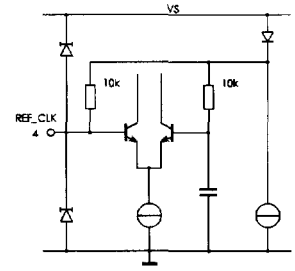
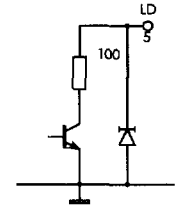
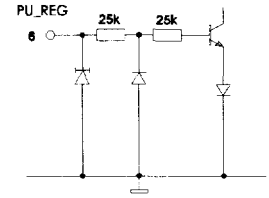
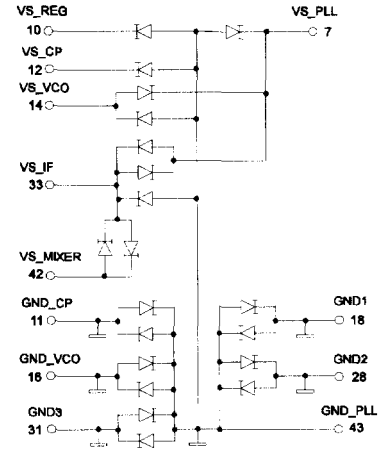


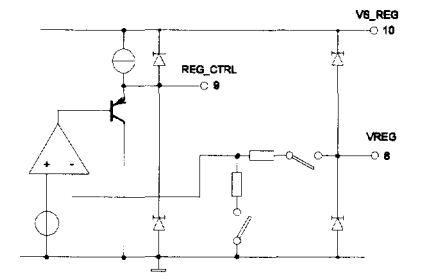
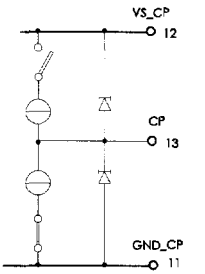
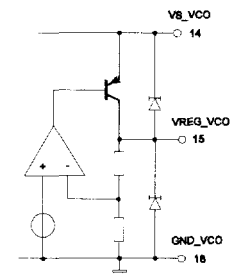
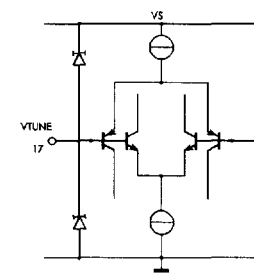
Figure 2. Pinning

Pin	Symbol	Function	Configuration
1	CLOCK	3-wire-bus: Clock input	
2	DATA	3-wire-bus: Data input	
3	ENABLE	3-wire-bus: Enable input	

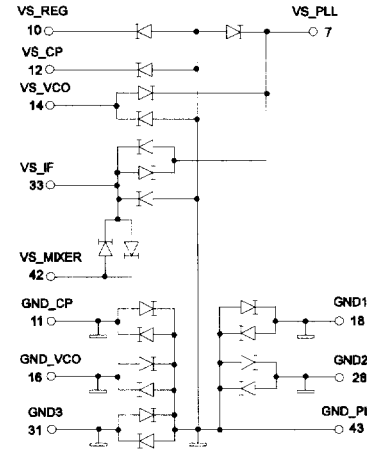
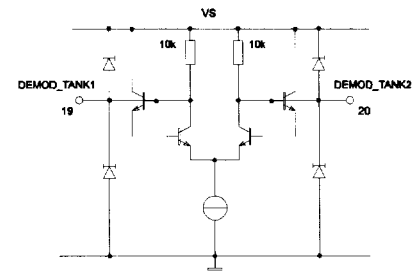
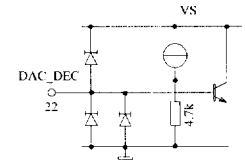
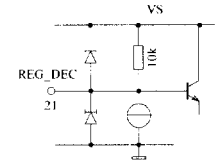
Pin Description (continued)

Pin	Symbol	Function	Configuration
4	REF_CLK	Reference-frequency input	
5	LD	Lock-detect output	
6	PU_REG	Aux. voltage regulator power-up input	
7	VS_PLL	PLL supply voltage	

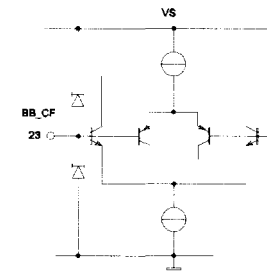
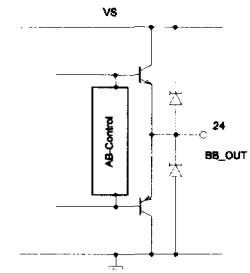
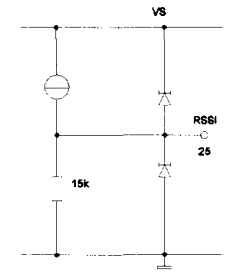
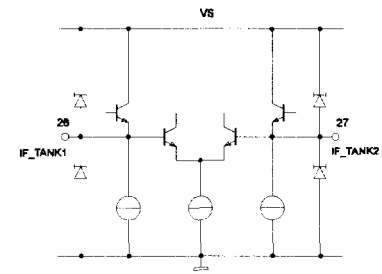
Pin Description (continued)

Pin	Symbol	Function	Configuration
8	VREG	Aux. voltage-regulator output	
9	REG_CTRL	Aux. voltage-regulator control output	
10	VS_REG	Aux. voltage-regulator supply voltage	
11	GND_CP	Charge-pump ground	
12	VS_CP	Charge-pump supply voltage	
13	CP	Charge-pump output	
14	VS_VCO	VCO voltage-regulator supply voltage	
15	VREG_VCO	VCO voltage-regulator control output	
16	GND_VCO	VCO ground	
17	VTUNE	VCO tuning voltage input	

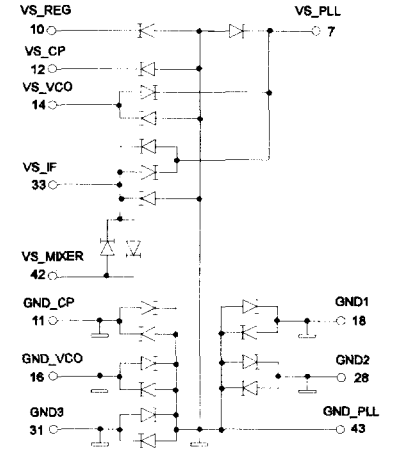
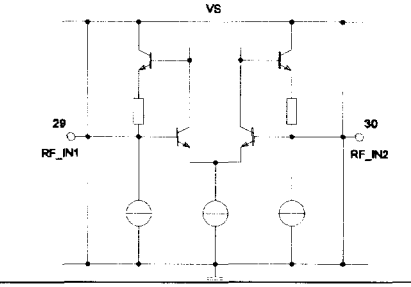
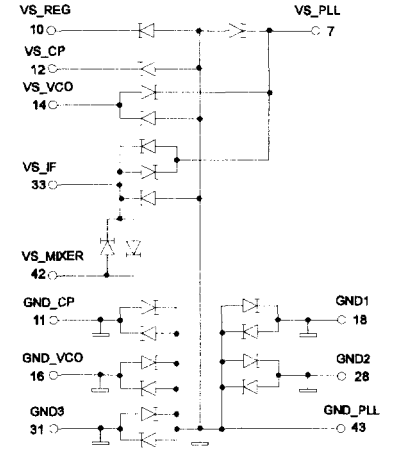
Pin Description (continued)

Pin	Symbol	Function	Configuration
18	GND1	Ground	
19	DEMOD_TANK1	Demodulator tank circuit	
20	DEMOD_TANK2	Demodulator tank circuit	
21	DAC_DEC	Decoupling PIN for VCO_DAC	
22	REG_DEC	Decoupling PIN for REG	

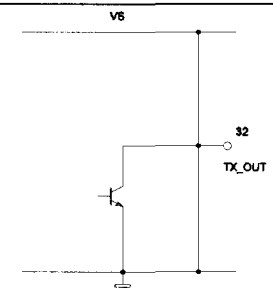
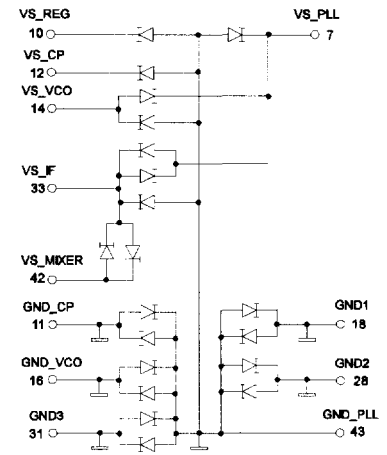
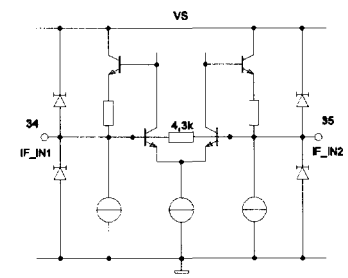
Pin Description (continued)

Pin	Symbol	Function	Configuration
23	BB_CF	Baseband filter corner-frequency control input	
24	BB_OUT	Baseband filter output	
25	RSSI	Received signal-strength indicator output	
26	IF_TANK1	IF tank circuit	
27	IF_TANK2	IF tank circuit	

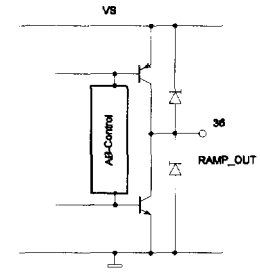
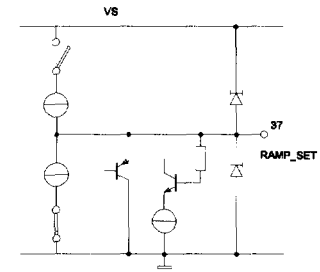
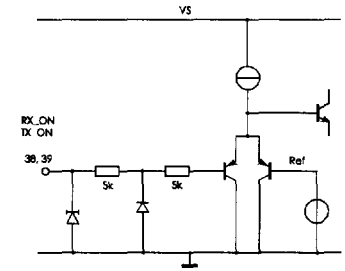
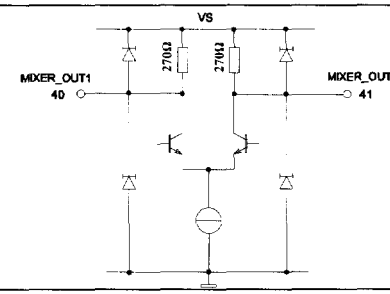
Pin Description (continued)

Pin	Symbol	Function	Configuration
28	GND2	Ground	
29	RF_IN1	Differential RF input of image reject mixer	
30	RF_IN2	Differential RF input of image reject mixer	
31	GND3	Ground	

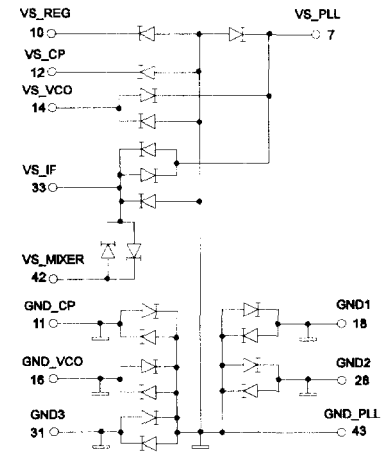
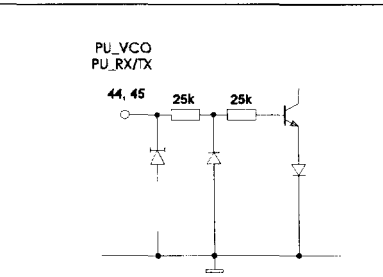
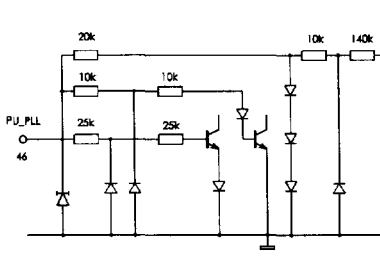
Pin Description (continued)

Pin	Symbol	Function	Configuration
32	TX_OUT	TX driver amplifier output for PA	
33	VS_IF	IF amplifier supply voltage	
34	IF_IN1	Differential IF input of IF amplifier	
35	IF_IN2	Differential IF input of IF amplifier	

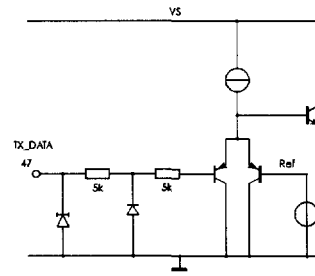
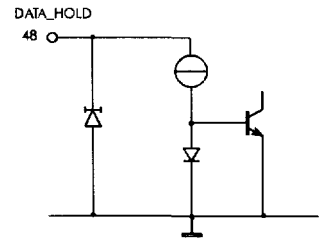
Pin Description (continued)

Pin	Symbol	Function	Configuration
36	RAMP_OUT	Ramp-generator output for PA power ramping	
37	RAMP_SET	Slew-rate setting of ramping signal	
38	RX_ON	RX control input	
39	TX_ON	TX control input	
40	MIXER_OUT1	Differential mixer output for SAW filter	
41	MIXER_OUT2	Differential mixer output for SAW filter	

Pin Description (continued)

Pin	Symbol	Function	Configuration
42	VS_MIXER	Mixer supply voltage	
43	GND_PLL	PLL ground	
44	PU_VCO	VCO power-up input	
45	PU_RX/TX	RX/TX power-up input	
46	PU_PLL	PLL power-up input	

Pin Description (continued)

Pin	Symbol	Function	Configuration
47	TX_DATA	TX data input of Gaussian filter and modulation-compensation circuit	
48	DATA_HOLD	Data-hold input to keep the latch information in power-down mode	

Functional Description

Receiver

The RF-input signal at RF_IN is fed to an image rejection mixer IR_MIXER with its differential outputs MIXER_OUT1 and MIXER_OUT2 driving an IF-SAW filter at 110 MHz or 111 MHz. The IF amplifiers IF_AMP1 and IF_AMP2 with an external IF_TANK and an integrated RSSI function feed the signal to the demodulator DEMOD working at $f = f_{IF}/2$ (55 MHz/ 55.5 MHz) and finally to an integrated baseband filter BB. For demodulator tuning in production an integrated 5-bit digital-to-analog (D/A) converter is used to control the on-chip varicap diode.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian filter GF and fed to the fully integrated VCO operating at twice the output frequency. After modulation the signal is frequency-divided by 2 and fed via a TX/RX SWITCH to the TX_DRIVER. This bus-controlled driver amplifier supplies +3 dBm output power at TX_OUT. A ramp-signal generator RAMP_GEN, providing ramp signals at RAMP_OUT for an external power amplifier, is also integrated. The slope of the ramp signal is controlled by a capacitor at RAMP_SET.

Synthesizer

The IR_MIXER, the TX_DRIVER and the programmable counter PC are driven by the fully integrated VCO (including on-chip inductors and varactors). An 3-bit digital-to-analog converter is used to pretune the frequency. The output signal is frequency-divided to supply the desired frequency to the TX_DRIVER, 0/90 degree phase shifter for the IR_MIXER and to be used by the PC for the phase detector PD (f_{PD} = 3.456 MHz). Unlimited multislot operation is possible by using the integrated advanced closed-loop modulation concept based on the modulation compensation circuit MCC.

Power Supply

For minimum interference and maximum signal isolation an integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

PLL Principle

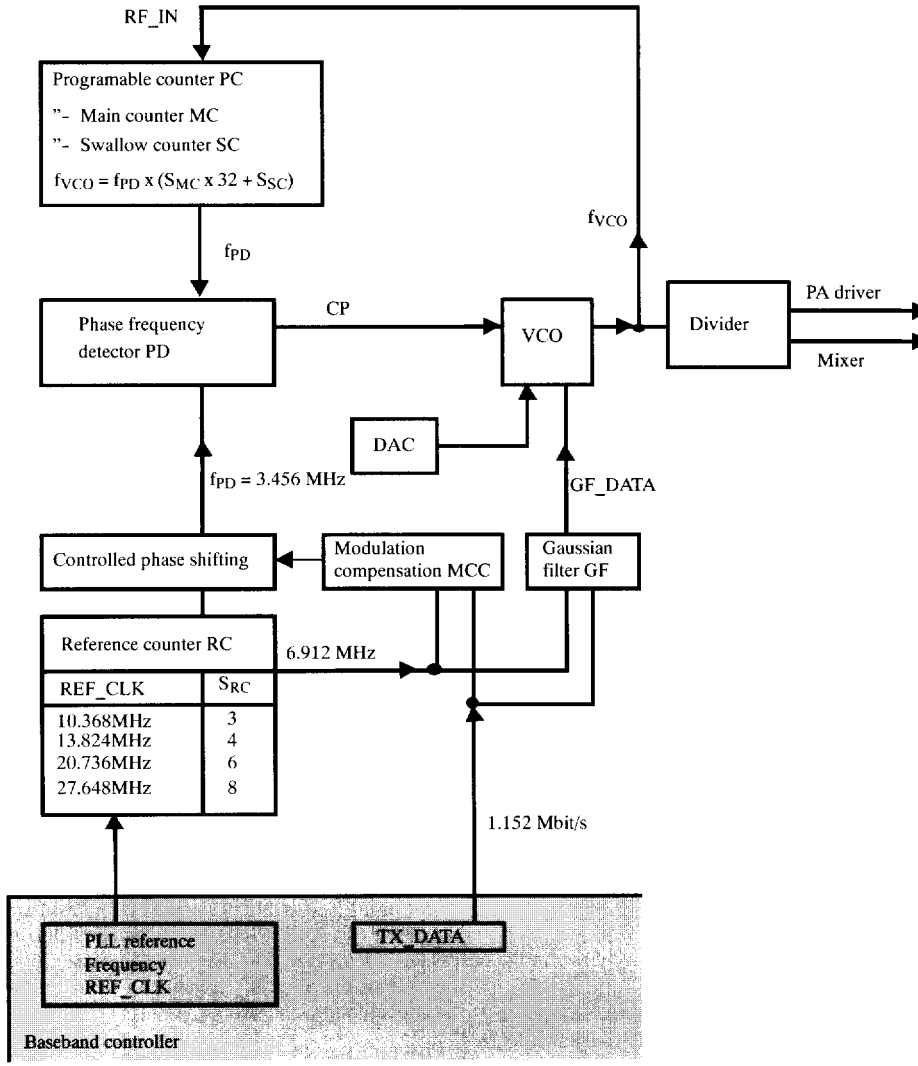


Figure 3.

The following table shows the LO frequencies for RX and TX for the DECT band plus additional channels for an optional DECT band extension. Intermediate frequencies of 110.592 and 112.32 MHz are supported.

Table 1 LO frequencies

Mode	f_{IF}/MHz	Channel	f_{ANT}/MHz	f_{VCO}/MHz	$f_{VCO}/2$/MHz	S_{MC}	S_{SC}
TX		C9	1881.792	3763.584	1881.792	34	1
		C8	1883.520	3767.040	1883.520	34	2
		...	...	...	...	...	...
		C1	1895.616	3791.232	1895.616	34	9
		C0	1897.344	3794.688	1897.344	34	10
		C10	1899.072	3798.144	1899.072	34	11
		C11	1900.800	3801.600	1900.800	34	12
		...	...	...	...	...	...
		C29	1931.904	3863.808	1931.904	34	30
		C30	1933.632	3867.264	1933.632	34	31
RX	110.952	C9	1881.792	3542.400	1771.200	32	1
		C8	1883.520	3545.856	1772.928	32	2
		...	...	...	...	...	...
		C1	1895.616	3570.048	1785.024	32	9
		C0	1897.344	3573.504	1786.752	32	10
		C10	1899.072	3576.960	1788.480	32	11
		C11	1900.800	3580.416	1790.208	32	12
		...	...	...	...	...	...
		C29	1931.904	3642.624	1821.312	32	30
		C30	1933.632	3646.080	1823.040	32	31
RX	112.320	C9	1881.792	3538.944	1769.472	32	1
		C8	1883.520	3542.400	1771.200	32	2
		...	...	...	...	...	...
		C1	1895.616	3566.592	1783.296	32	9
		C0	1897.344	3570.048	1785.024	32	10
		C10	1899.072	3573,504	1786.752	32	11
		C11	1900.800	3576.960	1788.480	32	12
		...	...	...	...	...	...
		C29	1931.904	3639.168	1819.584	32	30
		C30	1933.632	3642.624	1821.312	32	31

Table 2 Limits

Mode	f_{IF}/MHz		f_{ANT}/MHz	f_{VCO}/MHz	$f_{VCO}/2$/MHz	S_{MC}	S_{SC}
TX		fmin	1769.472	3538.944	1769.472	32	0
RX	110.592		1880.064	3538.944	1769.472	32	0
	112.320		1826.496	3538.944	1769.472	32	0
TX		fmax	1988.928	3977.856	1988.928	35	31
RX	110.592		2099.520	3977.856	1988.928	35	31
	112.320		2101.248	3977.856	1988.928	35	31

Formula

$f_{ANT\,Ci} - f_{ANT\,Ci-1} = 1.728$ MHz for TX: $f_{VCO} = 2 \times f_{ANT}$ for RX: $f_{VCO} = 2 \times (f_{ANT} - f_{IF})$

Control Signals

LD output, which is active after PLL is locked and test-mode output (according to programmed test mode)
PU_REG hardware power up --> standby of regulator
PU_VCO hardware power up --> standby of voltage controlled oscillator
PU_RX/TX hardware power up --> standby of RX/ TX part
PU_PLL hardware power up --> standby of synthesizer

Table 3

Logic	Standby	Standby Hold Register	TX Mode	RX Mode	RSSI Only
DATA_HOLD	0	1	X	X	X
PU_REG	0	0	1	1	1
PU_VCO	X	X	1	1	1
PU_RX/TX	X	X	1	1	1
PU_PLL	X	X	1	1	1
RX_ON	X	X	0	1	1
TX_ON	X	X	1	0	1
BB filter	OFF	OFF	OFF	ON	OFF
Demodulator	OFF	OFF	OFF	ON	OFF
IF amplifiers and RSSI	OFF	OFF	OFF	ON	ON
IR mixer	OFF	OFF	OFF	ON	ON
RX switch	OFF	OFF	ON	ON	ON
TX switch	OFF	OFF	ON	OFF	OFF
TX driver	OFF	OFF	ON	OFF	OFF
Ramp generator	OFF	OFF	ON	OFF	OFF
Programmable counter	OFF	OFF	ON	ON	ON
Voltage-controlled oscillator	OFF	OFF	ON	ON	ON
Gaussian filter	OFF	OFF	ON	OFF	OFF
Phase detector / charge pump	OFF	OFF	ON	ON	ON
Modulation compensation circuit	OFF	OFF	ON	OFF	OFF
Reference counter	OFF	OFF	ON	ON	ON
Current consumption / mA @ V_S = 3.2 V	<0.01	<0.1	54	85	80

Serial Programming Bus

Reference and programmable counters can be programmed by the 3-wire bus (CLOCK, DATA and ENABLE). Besides this information additional control bits as phase detector polarity and scaling of charge-pump currents as well as internal currents for Gaussian lowpass filter and modulation compensation circuit can be transferred.

After setting enable signal to low condition, on the rising edge of the clock signal, the data status is transferred bit by bit into the shift register, starting with the MSB-bit.

After enable returning to high condition the programmed information is loaded into the addressed latches, according to the addressbit condition (last bit). Additional leading bits are ignored and there is no check made how many pulses have arrived during enable-low condition. The bus then returns to a low current standby mode until the ENABLE signal changes to low again.

To keep the information in the registers of the PLL during standby DATA_HOLD must be set to high condition.

Bus Protocol Formats

MSB LSB

Data bits | Address bit

D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
RC		SC					MC		PS			GF	MCC	GFCS			VCODAC			CPCS			1
1	0	0	1	1	1	1	0	0	1	1	1	0	0	1	0	0	1	0	0	1	0	0	1

Standard bit setting: Word 1

E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	A0
DEMODDAC					MCCS			TEST			0
0	0	0	0	0	0	0	0	0	0	0	0

Word 2 →

PLL Settings

RC (Reference Divider)		
D22	**D21**	**S_{RC}**
0	0	3
0	1	4
1	0	6
1	1	8

MC (Main Divider)		
D15	**D14**	**S_{MS}**
0	0	32
0	1	33
1	0	34
1	1	35

SC (Swallow Counter)					
D20	**D19**	**D18**	**D17**	**D16**	**S_{SC}**
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...					...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Phase Settings

Phase of GF-Output (Internal Connection)	
D13	**GF-DATA**
0	Source
1	Sink

Phase of MCC-Output (Internal Connection)	
D12	**MCC-Data**
0	Inverted
1	Normal

Phase of CP (Charge Pump)			
D11	**$f_R > f_P$**	**$f_R < f_P$**	**$f_R = f_P$**
0	I_{Sink}	I_{Source}	High imp.
1	I_{Source}	I_{Sink}	High imp.

Current Savings Power up/down Settings

D10	GF (Gaussian Filter)
0	OFF
1	ON

D9	MCC (Modulation Compensation Circuit)
0	OFF
1	ON

Current Gain Settings

GFCS (Gaussian Filtered Current Settings)			
D8	D7	D6	GFCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

CPCS (Charge-Pump Current Settings) (Internal Connection)			
D2	D1	D0	CPCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

MCCS (Modulation Compensation Current Settings) (Internal Connection)			
E5	E4	E3	MCCS
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

Pretune DAC Voltage Settings

Pretune DAC Voltage (Internal Connection)			
D5	D4	D3	f_{VCO}/%
0	0	0	-5
0	0	1	...
0	1	0	...
0	1	1	...
1	0	0	...
1	0	1	...
1	1	0	...
1	1	1	5

Test Mode Settings

Test Output Pin (Lock Detect)					
D11	E2	E1	E0	Signal at lock detect output	CP mode
X	0	0	0	Lock detect	Active
0	0	0	1	RC out	Active
1	0	1	0	PC out	Active
X	0	1	1	RC out divided by 2048 (MCCTEST)	Active
X	1	0	0	CP tristate only	High imp.
0	1	0	1	RC out	High imp.
1	1	1	0	PC out	High imp.
X	1	1	1	RC out divided by 2 (GFTEST)	High imp.

DEMOD DAC Voltage Settings (DEMODDAC)

Demod DAC Voltage (Internal Connection)					
E10	E9	E8	E7	E6	$f_{IFcenter}$ %
0	0	0	0	0	-6.0
0	0	0	0	1	...
0	0	0	1	0	...
					...
1	1	1	0	1	...
1	1	1	1	0	...
1	1	1	1	1	6.0

3-Wire Bus Protocol Timing Diagram

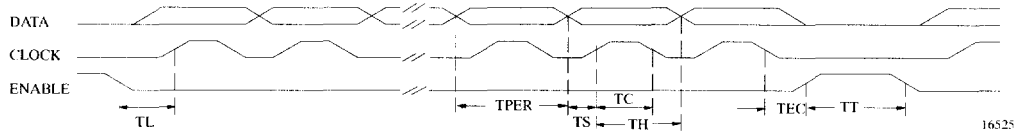


Figure 4.

Description	Symbol	Min. Value	Unit
Clock period	TPER	125	ns
Set time data to clock	TS	60	ns
Hold time data to clock	TH	60	ns
Clock pulse width	TC	125	ns
Set time enable to clock	TL	200	ns
Hold time enable to data	TEC	0	ns
Time between two protocols	TT	250	ns

Absolute Maximum Ratings

All voltages refer to GND

Parameter		Symbol	Min.	Max.	Unit
Supply voltage regulator	Pin 10	V_{S_REG}	3.2	4.7	V
Supply voltage	Pins 7, 12, 14, 33 and 42	V_S	3.0	4.7	V
Logic input voltage	Pins 1, 2, 3, 38, 39, 44, 45, 46, 47 and 48	V_{IN}	- 0.3	V_S	V
Junction temperature		T_{jmax}		150	°C
Storage temperature		T_{stg}	-40	150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	t.b.d.	K/W

Operating Range

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage regulator	Pins 10	V_S	3.2	3.6	4.6	V
Supply voltage	Pins 7, 12, 14, 33 and 42	V_S	3.0	3.0	4.6	V
Ambient temperature		T_{amb}	-25		+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Receiver						
IR mixer	**Pins 29, 30, 40 and 41**					
Input impedance	Pins 29 and 30	Z_{in}		50		Ω
Input matching	Pins 29 and 30	$VSWR_{in}$		<2:1		
Image rejection ratio	Pins 40 and 41	IRR		20		dB
DSB noise figure	Pins 40 and 41	NFDSB= NFSSB		10		dB
Conversion gain	R_{load} = 200 Ω	G_{conv}		12		dB
Output interception point	Pins 40 and 41	OIP3		10		dBm
IF amplifier	**Pins 26, 27, 34 and 35**					
Input impedance	Pins 34 and 35	Z_{in}	200		400	Ω
Lower cut-off frequency		fl_{3dB}		90		MHz
Upper cut-off frequency		fu_{3dB}		130		MHz
Power gain		Gp		85		dB
Bandwidth of external tank circuit	Pins 26 and 27	BW3dB		10		MHz
Noise figure		NF		9		dB
RSSI	**Pins 25, 34 and 35**					
RSSI sensitivity	at IF_IN1, IF_IN2 Pins 34 and 35	P_{min}		20		dBµV
RSSI compression	at IF_IN1, IF_IN2 Pins 34 and 35	P_{max}		100		dBµV
RSSI dynamic range		DR		80		dB
RSSI resolution	Slope of the RSSI has to be steady	Acc		±2		dB
RSSI rise time	P_{in} = 30 to 100 dBµV, Pin 25	t_r		1		µs
RSSI fall time	P_{in} = 100 to 30 dBµV, Pin 25	t_f		1		µs
Quiescent output current	@ P_{in} < 20 dBµV at IF_IN1, IF_IN2 Pin 25	I_{out}		30		µA
Maximum output current	@ P_{in} = 100 dBµV at IF_IN1, IF_IN2 Pin 25	I_{out}		150		µA
FM demodulator, BB-Filter	**Pins 19, 20, 23 and 24**					
Co-channel rejection ratio	@ P_{in} = -75 dBm at IR-mixer input	CCRR		10		dB
Sensitivity	Quality factor of external tank circuit approx. 20, $f_{res} = F_{IF}/2$, Pin 24	S		0.5		V/MHz
Amplitude of recovered signal	Nominal deviation of signal ± 288 kHz, Pin 24	A		288		mVss

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Corner frequency	Pin 23: C = 68 pF	f_c		680		kHz
Output voltage DC range	Pin 24	FM_{outDC}	1		Vs-1	V
Output impedance	Pin 21	Z_{out}		1.5		kΩ
AM rejection ratio	Pin 21	AMRR		t.b.d.		dB
DAC for FM demodulator (internally connected) (5-bit programming see bus protocol E5 to E10)						
DAC range		T_{DAC}		± 6		%
Transmitter/ PLL						
VCO						
Frequency range		f_{vco}	1750		2000	MHz
Tuning gain	Pin 17	G_{tune}		40		MHz/V
Frequency control voltage range	Pin 17	V_{tune}	0.4		2.8	V
DAC for VCO pretune (internally connected) (3-bit bus programming se bus protocol D3 to D5)						
DAC tuning range		$\Delta f_{vco,DAC}$		± 5		%
PLL	**Pin 4**					
Scaling factor prescaler		S_{PSC}	32 / 33			
Scaling factor main counter		S_{MC}	32 / 33 / 34 / 35			
Scaling factor swallow counter		S_{SC}	0		31	
External reference input frequency	AC coupled sinewave Pin 4	f_{REF_CLK}		13.824 27.648		MHz MHz
External reference input voltage	AC coupled sinewave Pin 4	V_{REF_CLK}	50		250	mV_{RMS}
Scaling factor reference counter		S_{RC}	3 / 4 / 6 / 8			
Charge pump (active when RX, TX)	**Pin 13**					
Output current	$V_{I\_CP\_SW}$ = '0', $V_{CP} = V_{VS\_CP} / 2$	I_{CP_1}		± 1		mA
Current scaling factor	I_{CP} = CPCS * I_{CP_TYP} (see bus protocol D0 ... D2)	CPCS	60		130	%
Leakage current		I_L		± 100		pA
Gaussian transmit filter (Gaussian shape B*T = 0.5)						
Tx data filter clock	12 taps in filter	f_{TXFCLK}		13.824		MHz
Frequency deviation	Polarity (see bus protocol D13)	GF_{FM_TYP}		±288		kHz
Frequency deviation scaling	$GF_{FM} = GF_{FM\_TYP}$ * GFCS (see bus protocol D6 ... D8)	GFCS	60		130	%

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Modulation compensation circuit						
Oversampling		OVS		6		
Digital sum variation		DSV			85	
Current scaling factor	(see bus protocol E3 ... E5)	MCCS	60		130	%
VCO switch and TX driver	**Pin 32**					
Power gain	@ P_{in} = -40 dBm	Gp		30		dB
Output impedance	Pin 32	Z_{out}		100		Ω
Maximum output power	Pin 32	P_{max}		3		dBm
Gain compression	@ TX_RF_OUT, Pin 32	P_{1dB}		1		dBm
Output interception point	Pin 32	OIP3		10		dBm
Ramp generator	**Pins 36 and 37**					
Minimum output voltage	According to RAMP_SET input	V_{min}		0.2		V
Maximum output voltage	According to RAMP_SET input	V_{max}		1.95		V
Rise time	C_{ramp} = 270 pF at Pin 37	t_r		5		µs
Fall time	C_{ramp} = 270 pF at Pin 37	t_f		5		µs
Lock detect and test mode output	**Pin 5**					
Lock detect output, test mode output	locked = '1', unlocked = '0' test modes (see bus protocol E0 ... E2)	LD				
Leakage current	V_{OH} = 4.6 V	I_L			5	µA
Saturation voltage	I_{OL} = 0.5 mA	V_{SL}			0.4	V
Auxiliary regulator	**Pins 8, 9 and 10**					
Output voltage	V_{SREG} = 3 V Pin 8	V_{REG}	2.9	3.0	3.1	V
Supply voltage rejection	$V_{Pin10} = V_{DC} + 0.1\ V_{pp}$ f_{Pin10} = 0.1 to 10 kHz C_{Pin8} = 100 nF	SVR		t.b.d.		dB
VCO regulator	**Pins 14, 15 and 12**					
Output voltage	V_{SVCO} = 3 V Pin 15	V_{REG_VCO}	2.6	2.7	2.8	V
3-wire bus						
Clock		f_{Clock}		1.152	6.912	MHz
Logic input levels (CLOCK, DATA, ENABLE, RX_ON, TX_ON, PU_VCO, TX_DATA, DATA_HOLD) Pins 1, 2, 3, 38, 39, 44, 47 and 48						
High input level	= '1'	V_{iH}	1.5			V
Low input level	= '0'	V_{iL}			0.5	V
High input current	= '1'	I_{iH}	-5		5	µA
Low input current	= '0'	I_{iL}	-5		5	µA

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Standby control	**Pins 6, 45 and 46**					
Power up PU_REG = '1' PU_RX/TX = '1' PU_PLL = '1' High input level	Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU\_RX/TX}$ V_{PU_PLL}	2.0			V
Standby PU_REG = '0' PU_RX/TX = '0' PU_PLL = '0' Low input level	Pin 6 Pin 45 Pin 46	$V_{PU\_REG,OFF}$ $V_{PU\_RX/TX,OFF}$ $V_{PU\_PLL,OFF}$			0.7	V
Power up PU_REG = '1' PU_RX/TX = '1' PU_PLL = '1' High input current	V_{PU} = 3 V Pin 6 V_{PU} = 5.5 V Pin 45 V_{PU} = 3 V Pin 46 V_{PU} = 5.5 V	I_{PU_REG} $I_{PU\_RX/TX}$ I_{PU_PLL}	20 60 100 200	30 80 125 300	40 100 150 400	µA µA µA µA
Standby PU_xxxx = '0' Low input current	V_{PU} = 0 V Pin 6, V_{PU} = 0.5 V Pins 45, 46	$I_{PU,OFF}$			0.1 1	µA µA
Settling time V_S = 0 → active operation	Switched from V_S = 0 to V_S = 3V	t_{soa}		< 10		µs
Settling time standby → active operation	Switched from PU = '0' to PU = '1'	t_{ssa}		< 10		µs
Settling time active operation → standby	Switched from PU = '1' to standby	t_{sas}		< 2		µs
Power supply	**Pins 7, 10, 12, 14, 33 and 42**					
Total supply current	RX	I_S		85		mA
	RSSI only	I_S		82		mA
	TX	I_S		54		mA
	TX (MCC, GF active)	I_S		58		mA
Standby current, mode 1	PU_RX/TX = GND	I_S		1	10	µA
mode 2	PU=GND, DATA_HOLD=V_S	I_S		50	100	µA
Supply current CP	V_{VS_CP} = 3 V, PLL in lock condition Pin 13	I_{CP}		1		µA

Typical Application Circuit

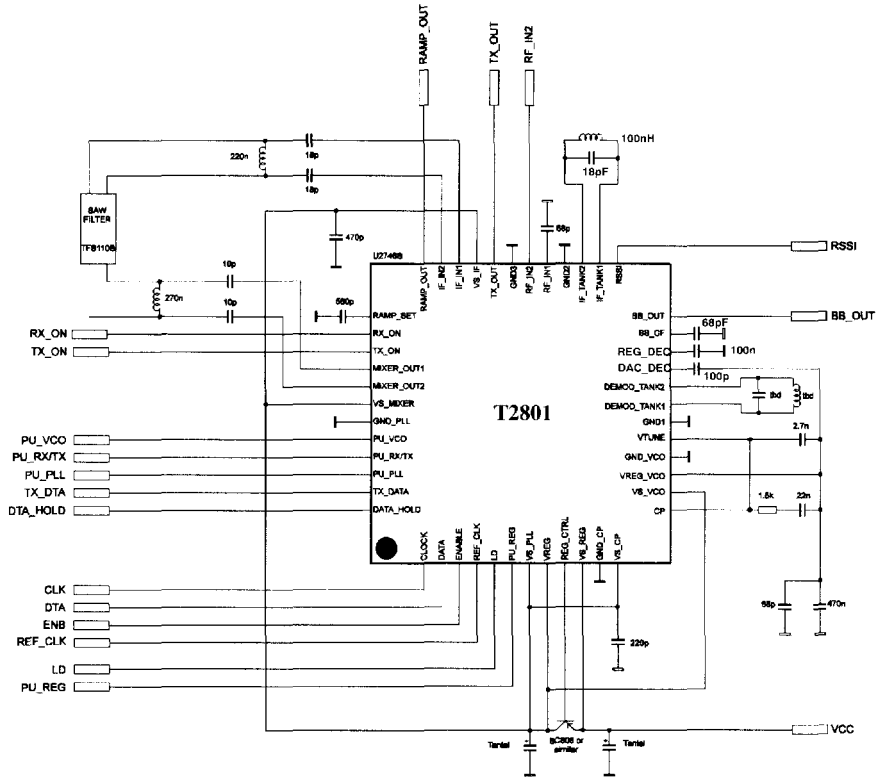


Figure 5. Typical application circuit

Package Information

Package: HP-VFQFP-N48
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm