Signetics

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Status	Product Specification
FAST Products	

FAST 74F651, 74F651A 74F652, 74F652A Transceivers/Registers

74F651/74F651A Octal Transceiver/Register, Inverting (3-State)
74F652/74F652A Octal Transceiver/Register, Non-Inverting (3-State)

FEATURES

- **Combines 'F245 and two 'F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	175MHz	110mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300mil)[1]	N74F651N, N74F652N
24-Pin Plastic Slim Dip (300mil)	N74F651AN, N74F652AN
24-Pin Plastic SOL[1]	N74F651AD, N74F652AD

NOTE 1:
Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

DESCRIPTION

The 74F651/74F651A and 74F652/74F652A Transceivers/ Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

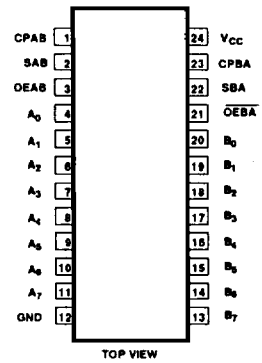
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	3.5/0.116	70μA/70μA
B_0 - B_7	B inputs	3.5/0.116	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
OEAB	A-to-B Output Enable input	1.0/0.033	20μA/20μA
$\overline{OEBA}$	B-to-A Output Enable input	1.0/0.033	20μA/20μA
A_0 - A_7, B_0 - B_7	A outputs ('F651, 'F652)	750/106.7	15mA/64mA
A_0 - A_7, B_0 - B_7	B outputs ('F651A, 'F652A)	750/80	15mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

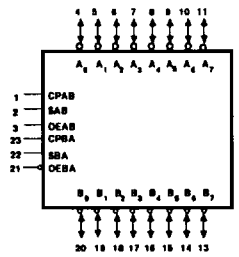
PIN CONFIGURATION

'F651/651A



LOGIC SYMBOL

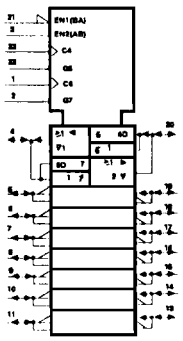
'F651/651A



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

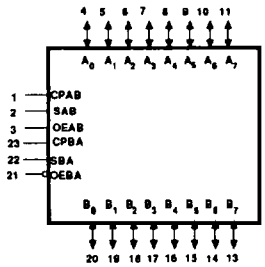
'F651/651A



The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F651/651A and 'F652/652A.
The select pins determine whether data is stored or transferred through the device in real time.
The Output Enable pins determine the direction of the data flow.

LOGIC SYMBOL

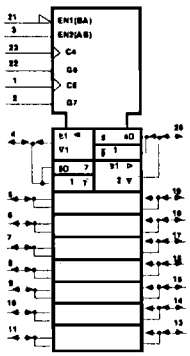
'F652/652A

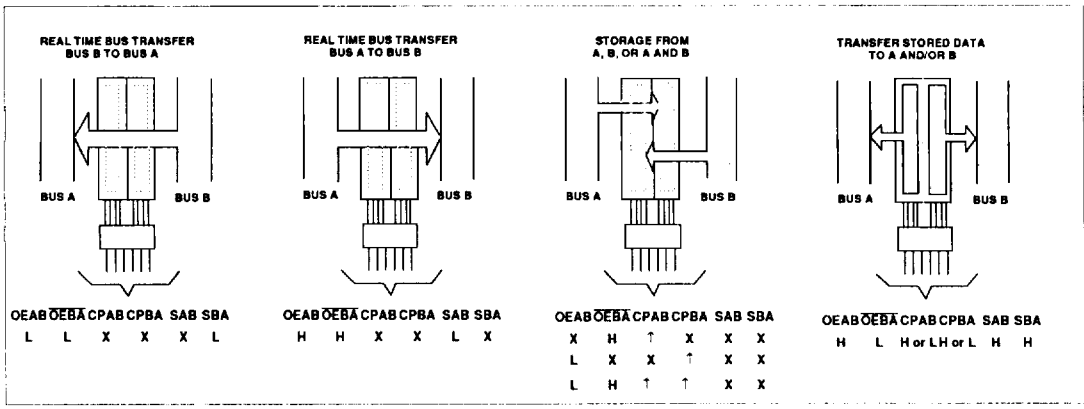


V_{CC} = Pin 24
GND = Pin 12

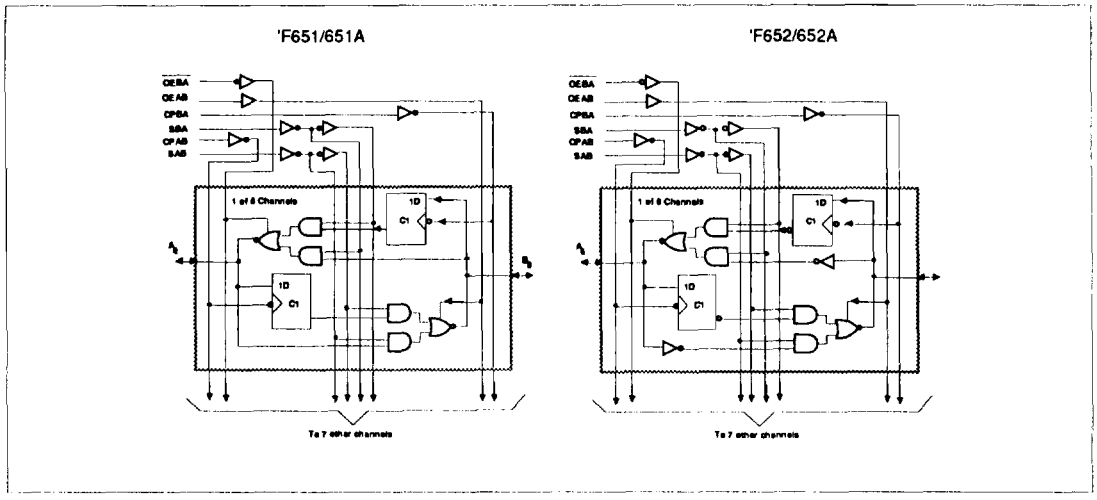
LOGIC SYMBOL(IEEE/IEC)

'F652/652A





LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_n	B_n	'651/651A	'652/652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
								Stored $\overline{B}$ data to A bus	Stored B data to A bus

NOTES:
H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	'F651, 'F652	128	mA
		'F651A, 'F652A	72	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	'F651, 'F652			64	mA
		'F651A, 'F652A			48	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage	others	V_{CC} =0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} =5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA	V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} =MAX, V_I = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_I= 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	74F651 74F652	V_{CC} =MAX			-100		-225	mA
I_O	Output current[4]	74F651A 74F652A	V_{CC} =MAX, V_O=2.25V			-60		-160	mA
I_{CC}	Supply current (total)	74F651 74F652	I_{CCH}	V_{CC} =MAX			110 / 140[5]	155 / 185[5]	mA
			I_{CCL}				155 / 165[5]	200 / 240[5]	mA
			I_{CCZ}				130	175	mA
		74F651A 74F652A	I_{CCH}				105	145	mA
			I_{CCL}				115	165	mA
			I_{CCZ}				115	160	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).
5. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

AC SETUP REQUIREMENTS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS for 74F651A/74F652A

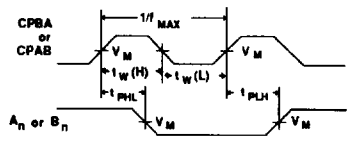
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	155	175		140		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	'F651A	Waveform 1	4.5 5.5	7.0 7.5	10.0 10.5	4.0 5.0	11.0 11.0	ns
		'F652A		5.0 5.0	7.5 7.0	10.0 10.0	4.5 4.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	'F651A	Waveform 2, 3	2.5 4.0	4.5 6.5	7.5 9.0	2.0 4.0	8.5 10.0	ns
		'F652A		4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	'F651A	Waveform 2, 3	4.0 5.0	7.0 7.0	10.0 10.0	3.5 4.5	12.0 10.0	ns
		'F652A		4.5 4.0	7.0 8.0	10.0 10.0	4.0 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n		Waveform 7 Waveform 8	3.0 3.5	5.0 6.0	8.0 8.5	2.5 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n		Waveform 7 Waveform 8	1.5 2.5	4.0 6.0	7.0 8.5	1.0 2.0	7.5 9.0	ns

AC SETUP REQUIREMENTS for 74F651A/74F652A

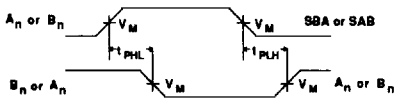
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 3.5			4.5 4.0		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

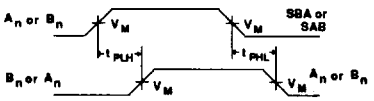
AC WAVEFORMS



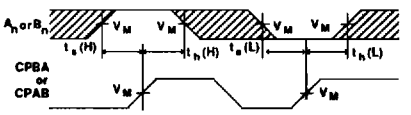
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



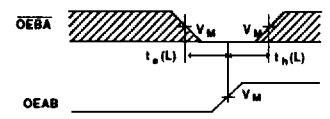
Waveform 2. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn



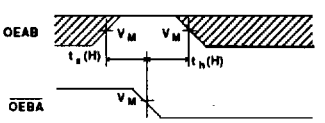
Waveform 3. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn



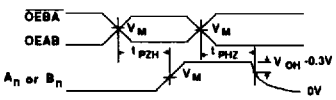
Waveform 4. Data Setup and Hold Times



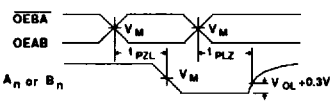
Waveform 5. OEBA to OEAB Setup and Hold Times



Waveform 6. OEAB to OEBA Setup and Hold Times



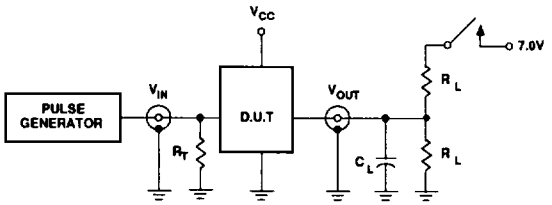
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level



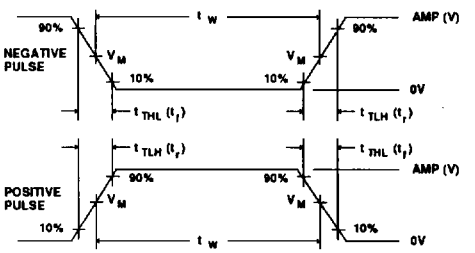
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns