Preliminary

OKI Semiconductor

MSM51V18160A

1,048,576-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51V18160A is a 1,048,576-word x 16-bit Dynamic RAM fabricated in OKI's CMOS silicon gate technology.
The MSM51V18160A achieve high integration, high-speed operation, and low-power consumption, due to quadruple polysilicon double metal CMOS.
The MSM51V18160A is available in a 42-pin SOJ or 50/44-pin plastic TSOP.

FEATURES

- 1,048,576-word x 16-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTL compatible, low input capacitance
- Output : LVTTL compatible, tristate
- Refresh : 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability

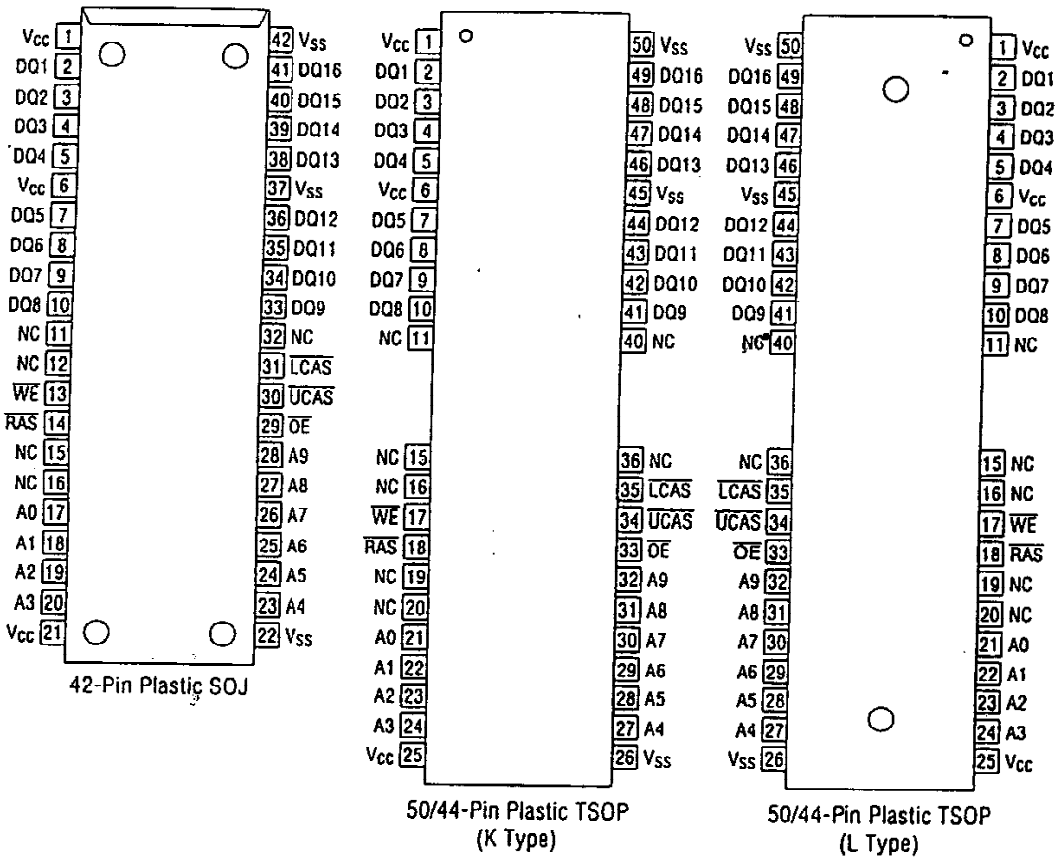
- Package:

42-Pin 400 mil Plastic SOJ	(SOJ42-P-400)	(Product : MSM51V18160A-xxJS)
50/44-Pin 400 mil Plastic TSOP	(TSOP50/44-P-400/0.8-K)	(Product : MSM51V18160A-xxTS-K)
	(TSOP50/44-P-400/0.8-L)	(Product : MSM51V18160A-xxTS-L)
		xx indicates speed rank.

PRODUCT FAMILY

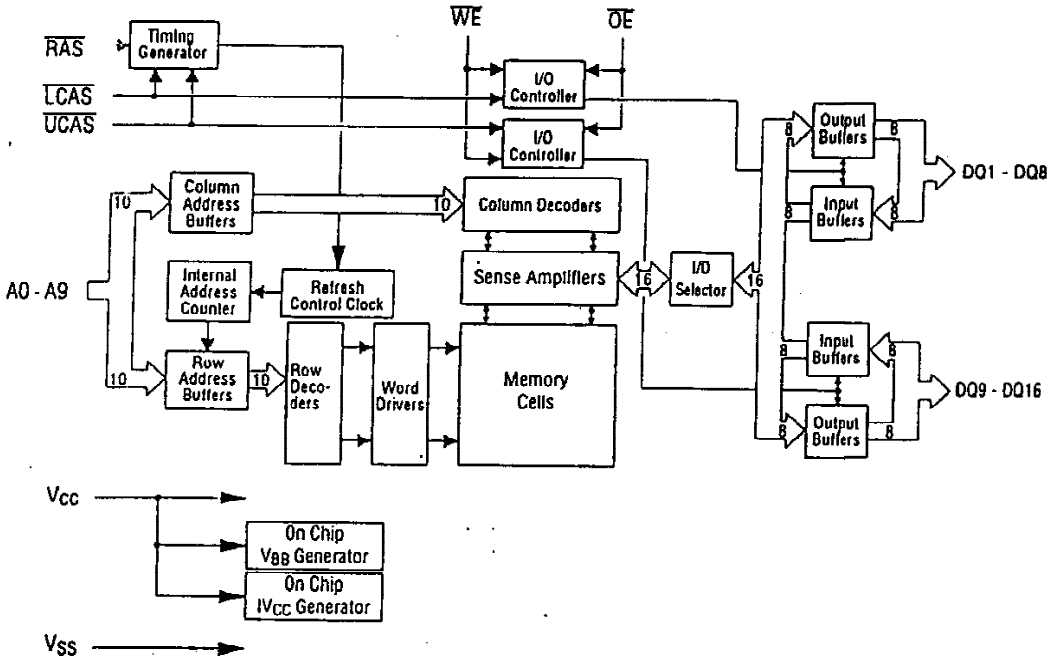
Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM51V18160A - 60	60 ns	30 ns	15 ns	15 ns	110 ns	684mW	3.6 mW
MSM51V18160A - 70	70 ns	35 ns	20 ns	20 ns	130 ns	648mW	
MSM51V18160A - 80	80 ns	40 ns	20 ns	20 ns	150 ns	612mW	

PIN CONFIGURATION (TOP VIEW)



Pin Name	Function
A0 - A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Lower Byte Column Address Strobe
$\overline{UCAS}$	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	Power Supply (3.3 V)
Vss	Ground (0 V)
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ1 - DQ8	DQ9 - DQ16	
H	•	•	•	•	High-Z	High-Z	Standby
L	H	H	•	•	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

Capacitance

(V_{CC} = 3.3 V ± 0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM51V18160A -60		MSM51V18160A -70		MSM51V18160A -80		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = −1.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 1.0 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ V_{CC} + 0.3 V; All other pins not under test = 0 V	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	DQ disable 0 V ≤ V_O ≤ 3.6 V	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	190	—	180	—	170	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2 V	—	1	—	1	—	1	mA	1
Average Power Supply Current ($\overline{RAS}$-only Refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	190	—	180	—	170	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	—	190	—	180	—	170	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	170	—	160	—	150	mA	1, 3

Notes : 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 0.3 V ±3.3 V, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51V18160A-60		MSM51V18160A-70		MSM51V18160A-80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	ns	
Read Modify Write Cycle Time	t_{RWC}	150	—	180	—	200	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	80	—	95	—	100	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	—	40	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	ns	4, 12
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	20	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	15	0	15	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	15	0	15	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	10	—	ns	14
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{RHCP}	35	—	40	—	45	—	ns	12
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	11
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	ns	11
Column Address Hold Time from $\overline{RAS}$	t_{AR}	50	—	55	—	60	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	11
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8, 11
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 0.3 V ±3.3 V, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM51V18160A -60		MSM51V18160A -70		MSM51V18160A -80		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9, 11
Write Command Hold Time	t_{WCH}	10	—	15	—	15	—	ns	11
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	45	—	55	—	60	—	ns	
Write Command Pulse Width	t_{WP}	10	—	15	—	15	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15	—	20	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	ns	13
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10, 11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	ns	10, 11
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	50	—	55	—	60	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	15	—	15	—	15	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	ns	9
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	ns	9
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	55	—	65	—	70	—	ns	9
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	5	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	—	5	—	5	—	ns	11
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	15	—	15	—	ns	12
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	20	—	30	—	40	—	ns	14

Notes:

1. A start-up delay of 200 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T = 5 ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 1 TTL loads and 100 pF. Output timing reference levels are V_{OH} = 2.0 V and V_{OL} = 0.8 V.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.
7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.) the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.) the cycle is read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
10. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a $\overline{OE}$ control write cycle or a read modify write cycle.
11. These parameters are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
12. These parameters are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
13. t_{CWL} should be satisfied by both $\overline{UCAS}$ or $\overline{LCAS}$.
14. t_{CP} and t_{CPT} are determined by the time that both $\overline{UCAS}$ or $\overline{LCAS}$ are high.

See ADDENDUM A for AC Timing Waveforms

TIMING WAVEFORM A

for **MSM5116160A**

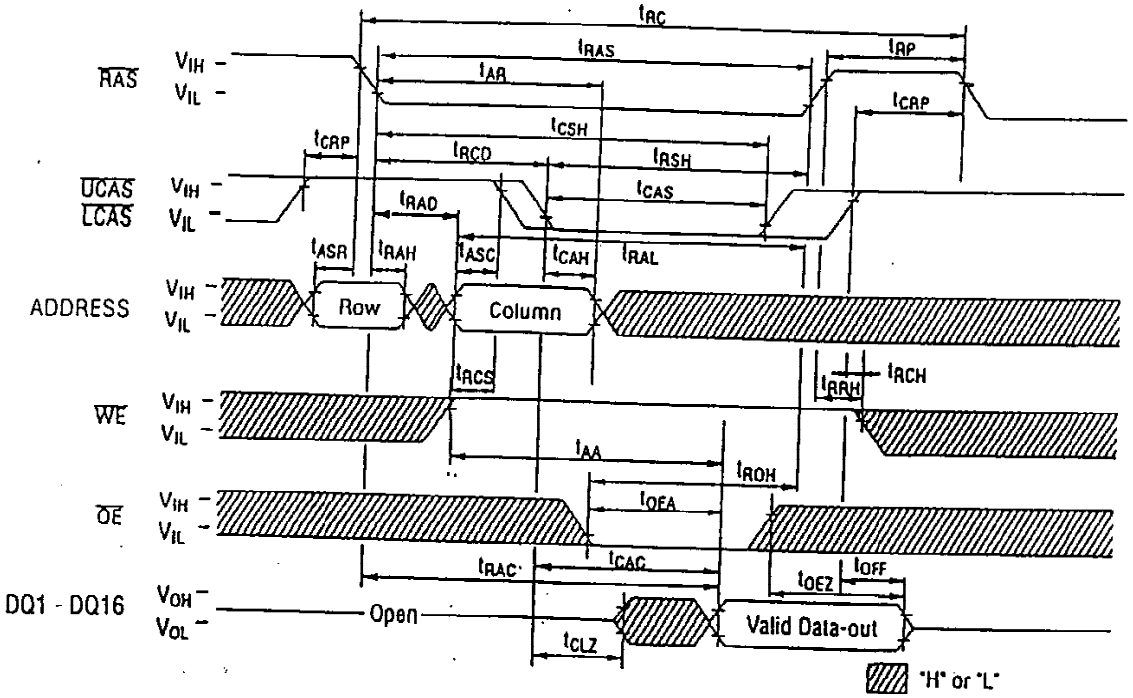
MSM5118160A

MSM51V16160A

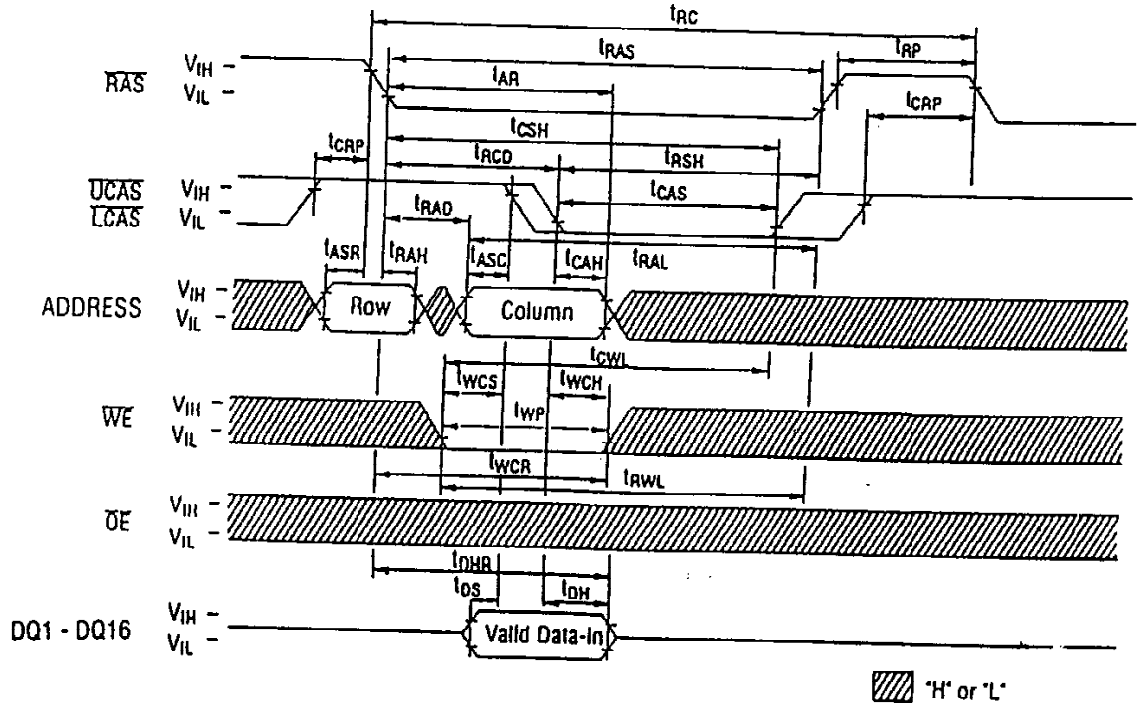
MSM51V18160A

TIMING WAVEFORM

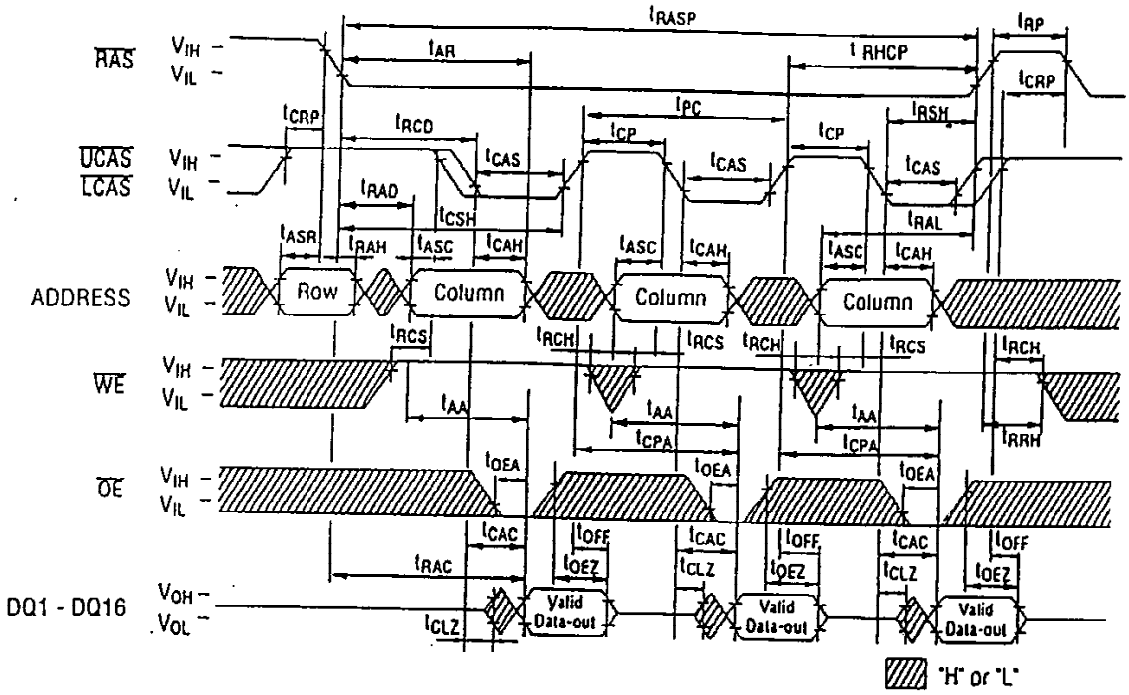
Read Cycle



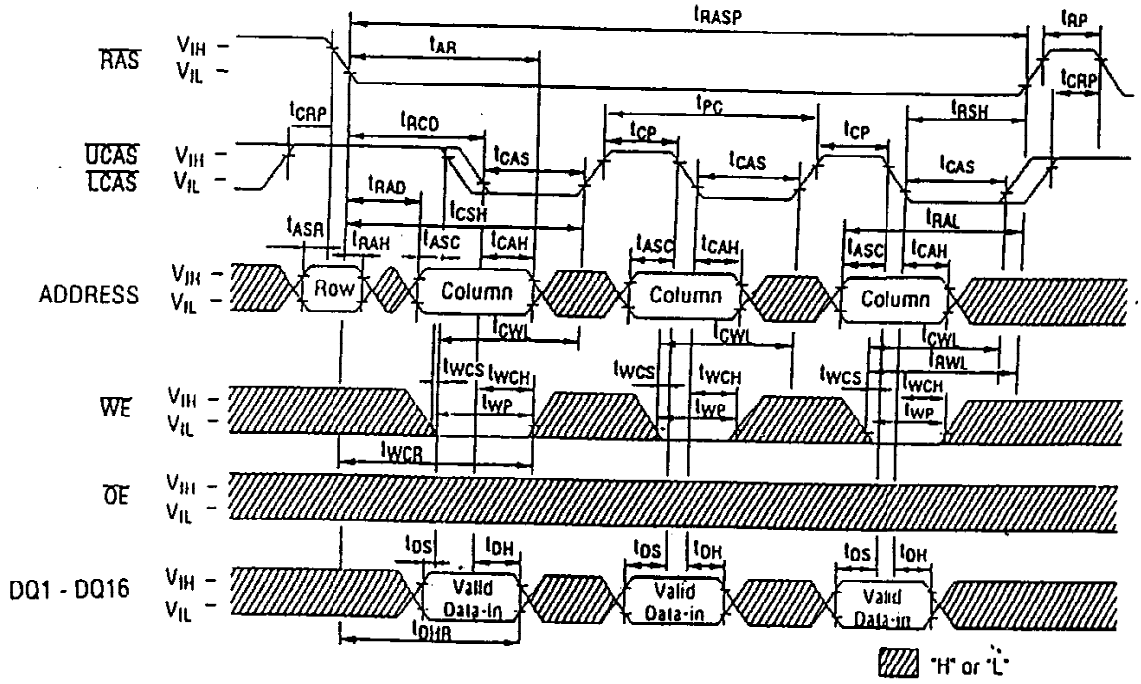
Write Cycle (Early Write)



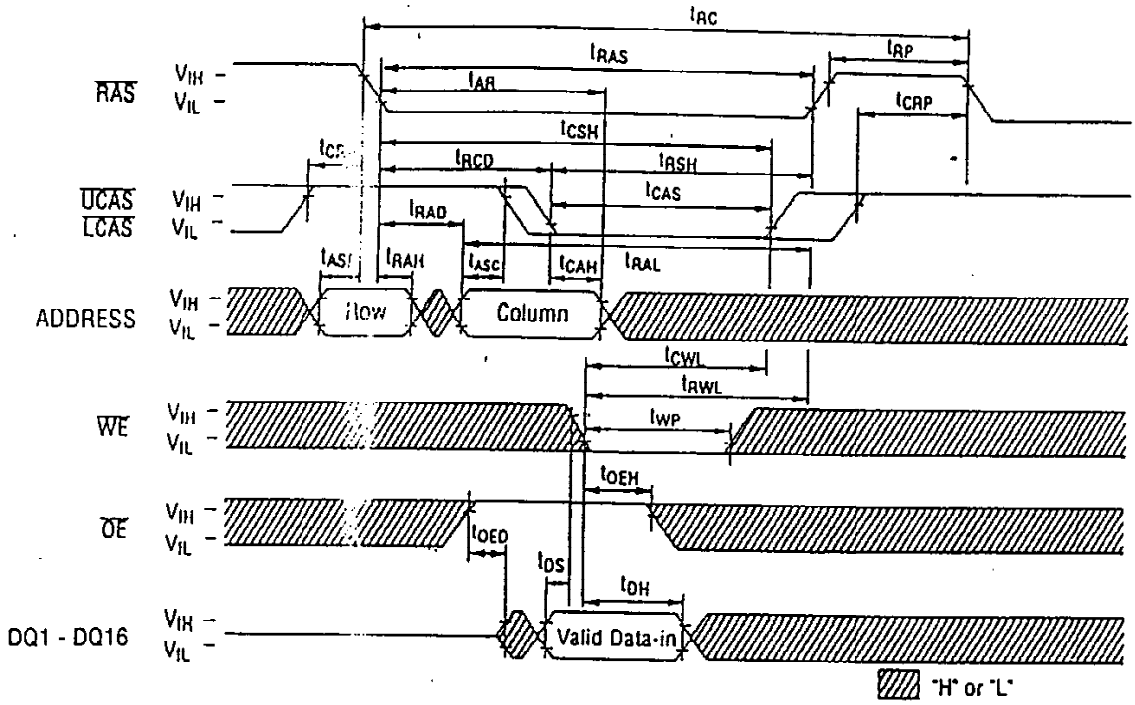
Fast Page Mode Read Cycle



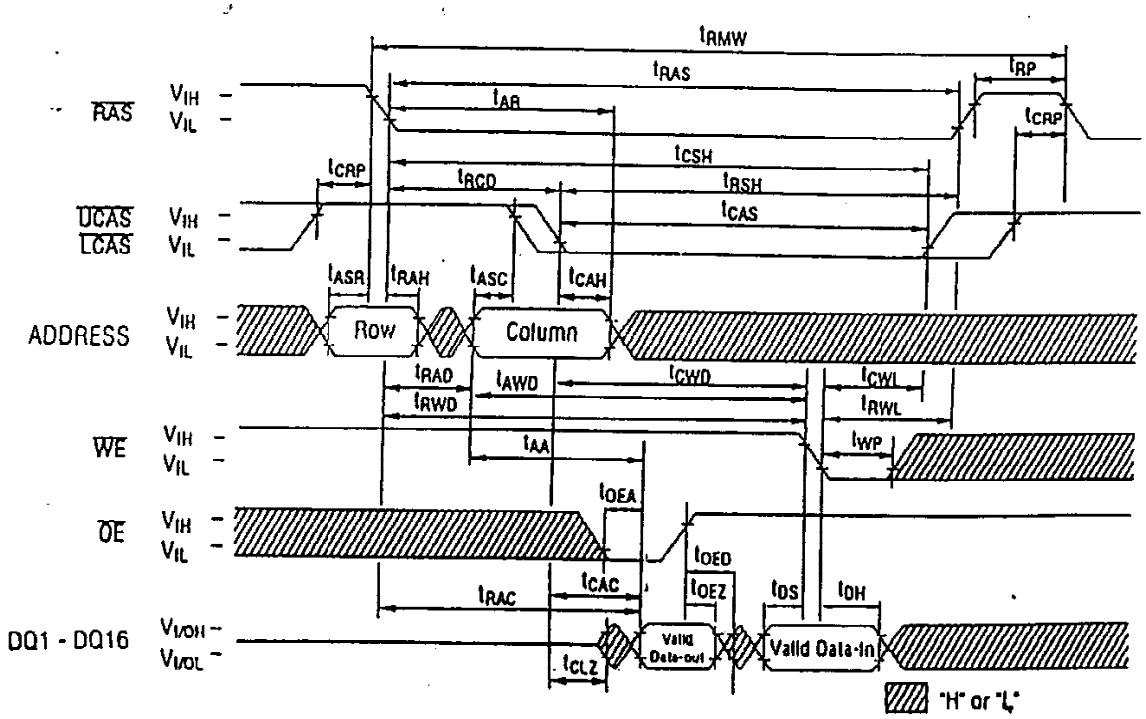
Fast Page Mode Write Cycle (Early Write)



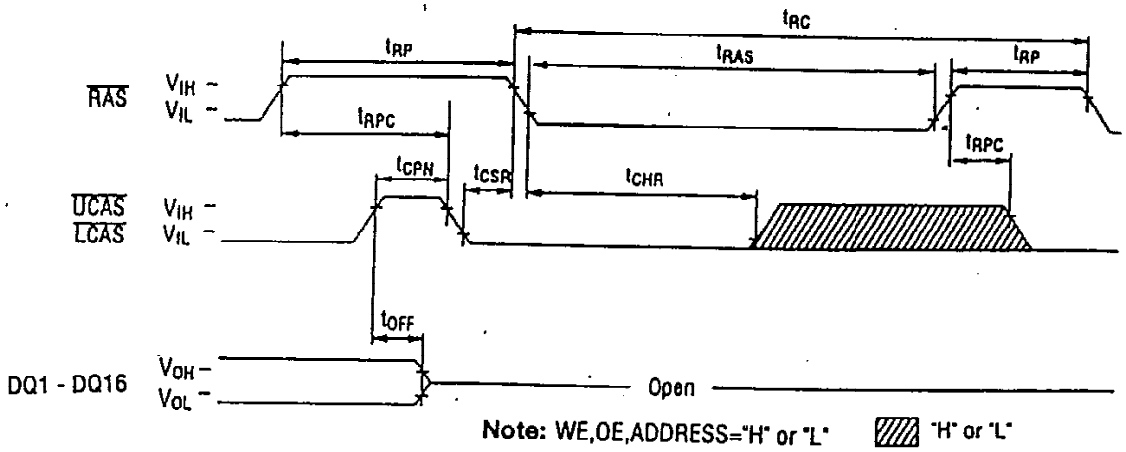
Write Cycle ($\overline{OE}$ Control Write)



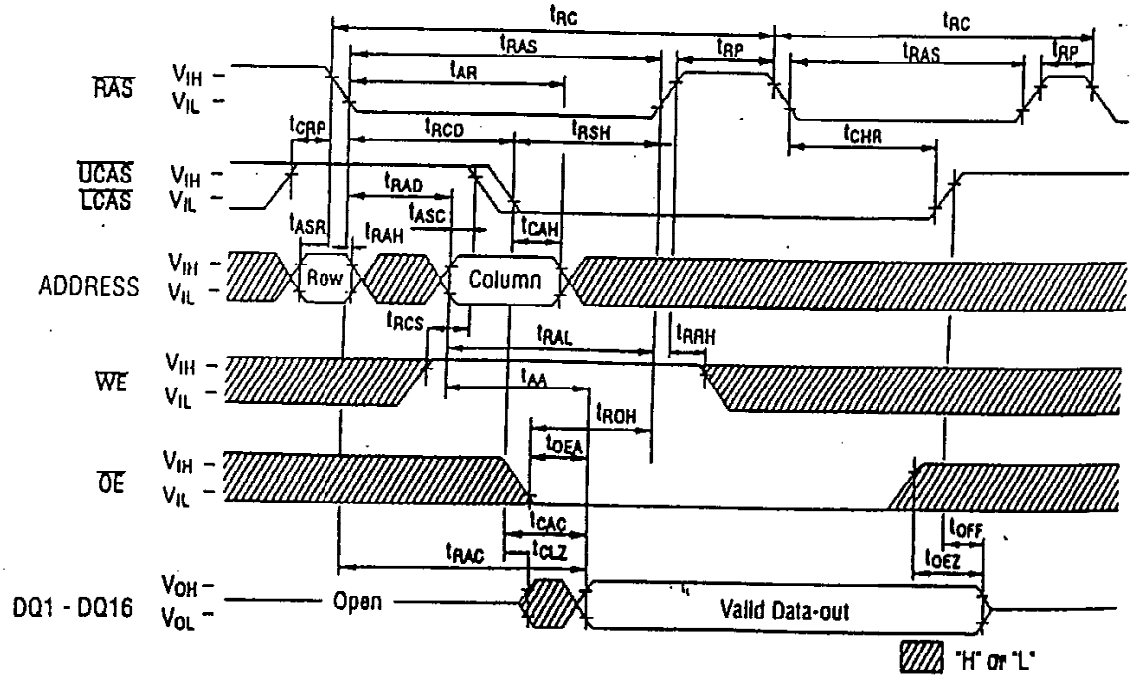
Read Modify Write Cycle



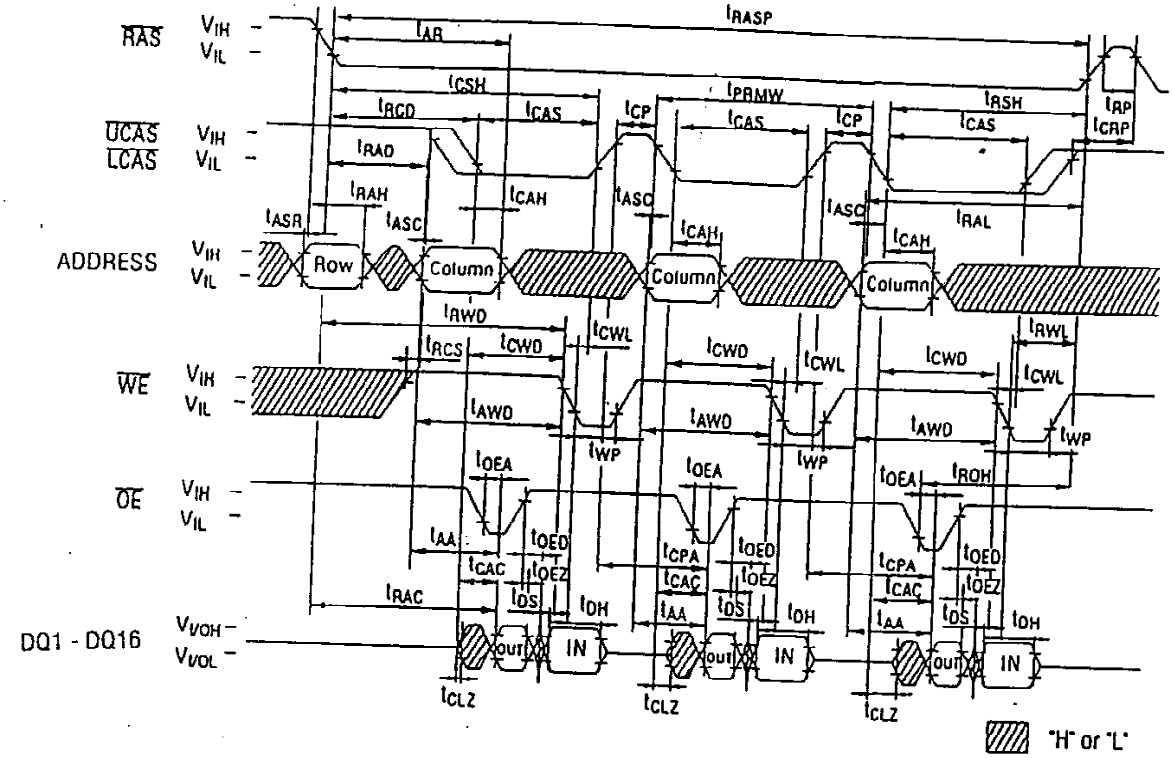
$\overline{CAS}$ Before $\overline{RAS}$ Auto Refresh Cycle



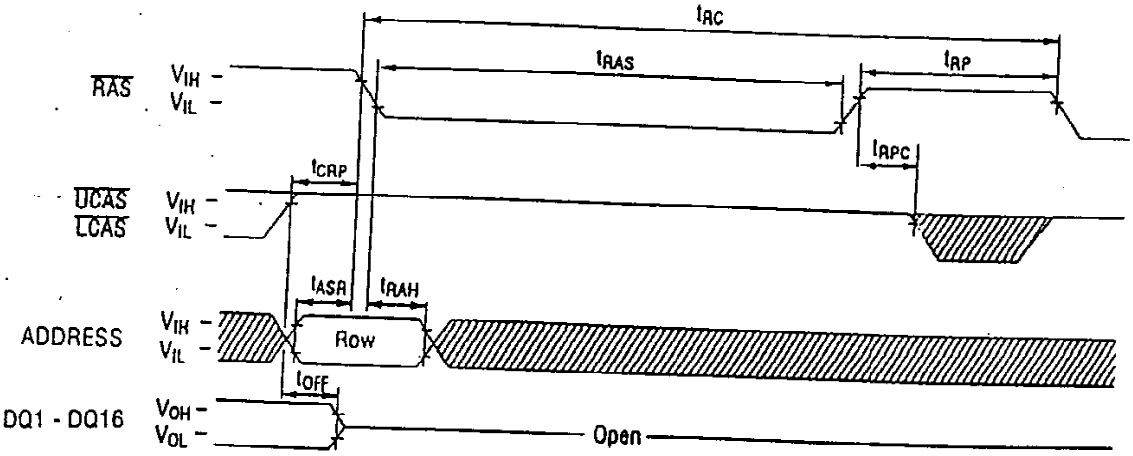
Hidden Refresh Read Cycle



Fast Page Mode Read Modify Write Cycle

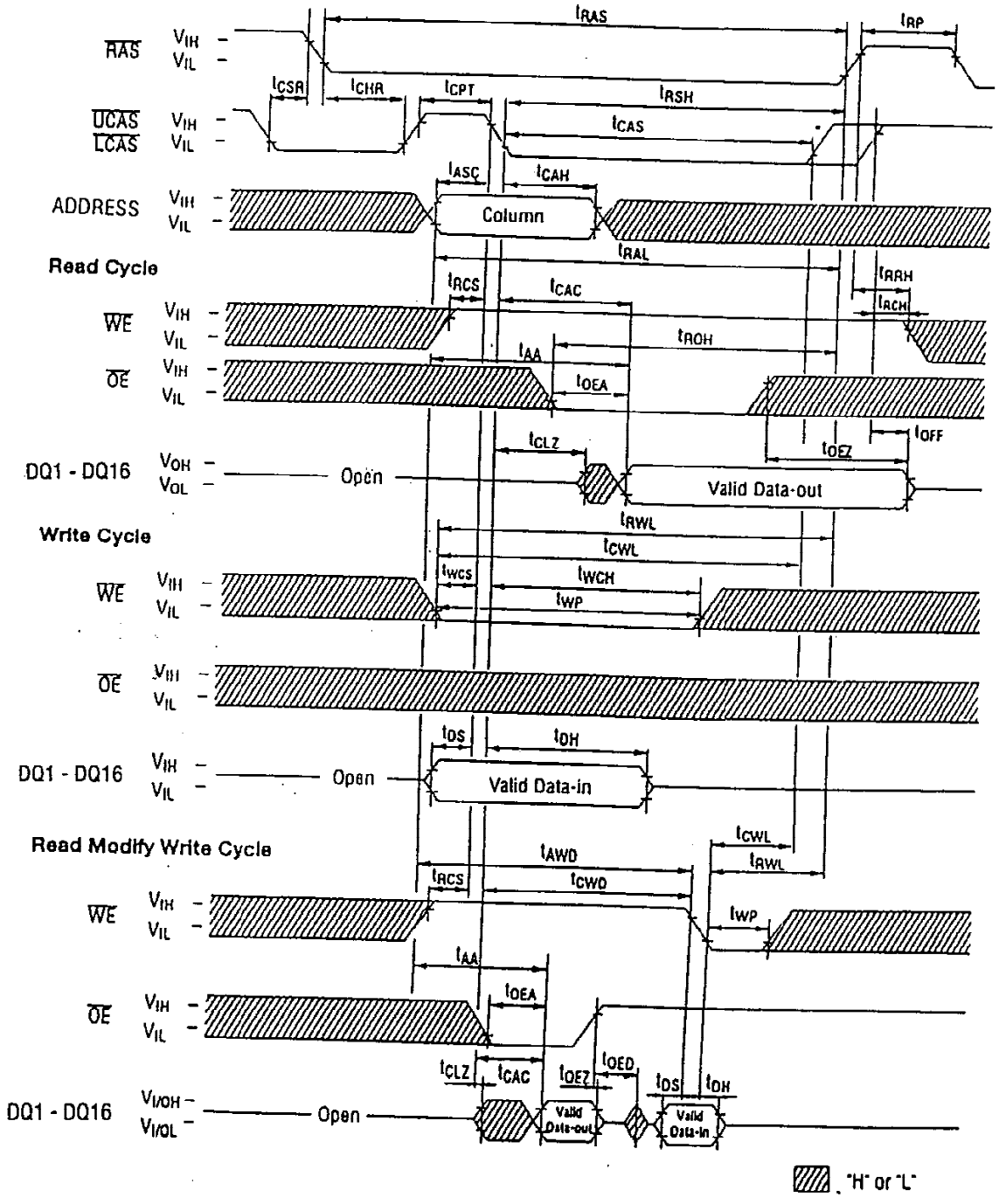


RAS-only Refresh Cycle



Note: WE, OE = "H" or "L" "H" or "L"

CAS Before RAS Refresh Counter Test Cycle



Hidden Refresh Write Cycle