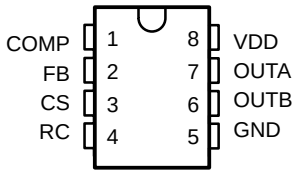
UCC2808–1, UCC2808–2, UCC3808–1, UCC3808–2
LOW POWER CURRENT MODE PUSH–PULL PWM

SLUS168D – APRIL 1999 – REVISED AUGUST 2002

- **Dual Output Drive Stages in Push-Pull Configuration**
- **130-μA Typical Starting Current**
- **1-mA Typical Run Current**
- **Operation to 1-MHz**
- **Internal Soft Start**
- **On Chip Error Amplifier With 2-MHz Gain Bandwidth Product**
- **On Chip VDD Clamping**
- **Output Drive Stages Capable Of 500-mA Peak Source Current, 1-A Peak Sink Current**

D OR N PACKAGE
(TOP VIEW)



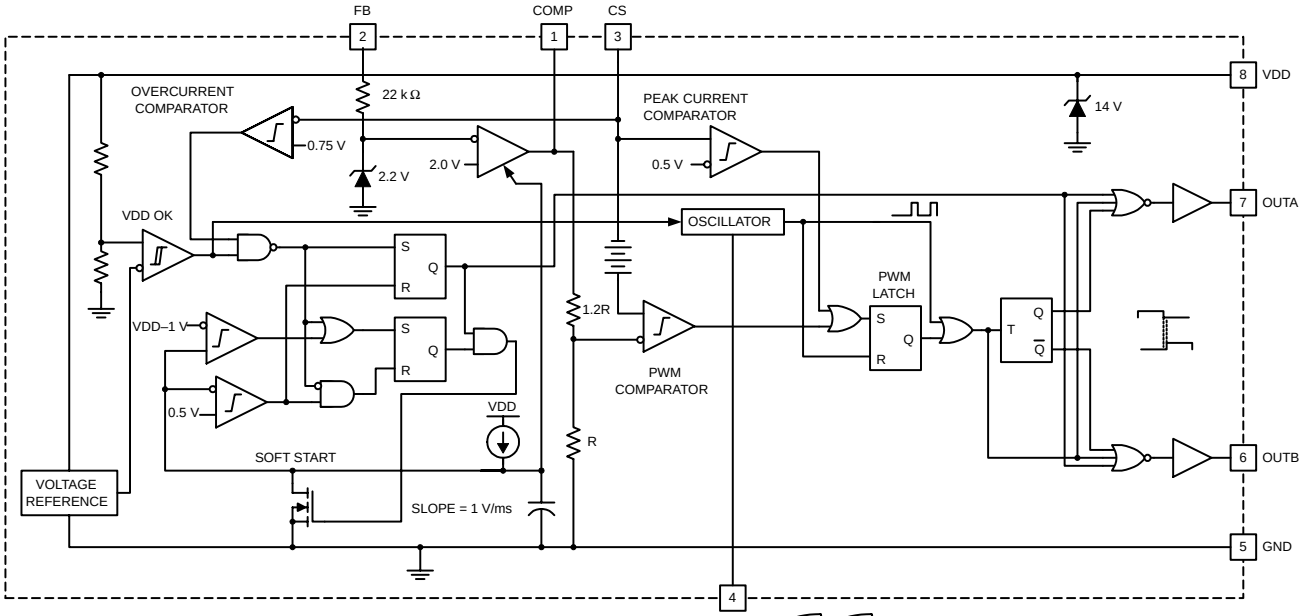
PW PACKAGE
(TOP VIEW)

description

The UCC3808 is a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCC3808 contains all of the control and drive circuitry required for off-line or dc-to-dc fixed frequency current-mode switching power supplies with minimal external parts count.

The UCC3808 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60 ns to 200 ns depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%. (continued)

block diagram



Note: Pinout shown is for SOIC and PDIP packages. TSSOP pinout is different.

UDG-02116

description (continued)

The UCC3808 family offers a variety of package temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the table below.

Table 1.

Part Number	Turn on Threshold	Turn off Threshold
UCCx808–1	12.5 V	8.3 V
UCCx808–2	4.3 V	4.1 V

ORDERING INFORMATION

$T_A = T_J$	Packaged Devices			
	UVLO Option	SOIC (D)	PDIP (N)	TSSOP (PW)
–40°C to 85°C	12.5 V/8.3 V	UCC2808D–1	UCC2808N–1	UCC2808PW–1
	4.3 V/4.1 V	UCC2808D–2	UCC2808N–2	UCC2808PW–2
0°C to 70°C	12.5 V/8.3 V	UCC3808D–1	UCC3808N–1	UCC3808PW–1
	4.3 V/4.1 V	UCC3808D–2	UCC3808N–2	UCC3808PW–2

† D (SOIC–8) and PW (TSSOP–8) packages are available taped and reeled. Add TR suffix to device type (e.g. UCC3808DTR–1) to order quantities of 2500 devices per reel for SOIC-8 and 2000 devices per reel for TSSOP-8.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (IDD ≤ 10 mA) . . . . . 15 V
Supply current . . . . . 20 mA
OUTA/OUTB source current (peak) . . . . . –0.5 A
OUTA/OUTB sink current (peak) . . . . . 1.0 A
Analog inputs (FB, CS) . . . . . –0.3 V to VDD+0.3 V, not to exceed 6 V
Power dissipation at T_A = 25°C (N Package) . . . . . 1 W
Power dissipation at T_A = 25°C (D Package) . . . . . 650 mW
Power dissipation at T_A = 25°C (PW Package) . . . . . 400 mW
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10 sec.) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)* for thermal limitations and considerations of packages.

electrical characteristics, T_A = 0°C to 70°C for the UCC3808–x, –40°C to 85°C for the UCC2808–x and –55°C to 125°C for the UCC1808–x, VDD = 10 V (See Note 6), 1 μF capacitor from VDD to GND, R = 22 kΩ, C = 330 pF, $T_A = T_J$, (unless otherwise specified)

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/VDD	See Note 1	0.44	0.5	0.56	V/V

error amplifier section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage	COMP = 2 V	1.95	2	2.05	V
Input bias current		–1		1	μA
Open loop voltage gain		60	80		dB
COMP sink current	FB = 2.2 V, COMP = 1 V	0.3	2.5		mA
COMP source current	FB = 1.3 V, COMP = 3.5 V	–0.2	–0.5		mA

PWM section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
Minimum duty cycle	COMP = 0 V			0%	

current sense section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain	See Note 2	1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5 V, See Note 3	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5 V, CS from 0 to 600 mV		100	200	ns
CS source current		–200			nA
Over current threshold		0.7	0.75	0.8	V
COMP to CS offset	CS = 0 V	0.35	0.8	1.2	V

NOTES: 1. Measured at RC. Signal amplitude tracks VDD.

2. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}, 0 \le V_{CS} \le 0.4\ V,$

3. Parameter measured at trip point of latch with FB at 0V.
4. Start threshold and zener shunt threshold track one another.
5. For UCCx808–1, set VDD above the start threshold before setting at 10 V.
6. Does not include current in the external oscillator network.

electrical characteristics, T_A = 0°C to 70°C for the UCC3808–x, –40°C to 85°C for the UCC2808–x and –55°C to 125°C for the UCC1808–x, VDD = 10 V (See Note 6), 1 μF capacitor from VDD to GND, R = 22 kΩ, C = 330 pF, $T_A = T_J$, (unless otherwise specified)

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUT low level	I = 100 mA		0.5	1	V
OUT high level	I = –50 mA, VDD – OUT		0.5	1	V
Rise time	C_L = 1 nF		25	60	ns
Fall time	C_L = 1 nF		25	60	ns

undervoltage lockout section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold	UCCx808–1, See Note 6	11.5	12.5	13.5	V
	UCCx808–2	4.1	4.3	4.5	V
Minimum operating voltage after start	UCCx808–1	7.6	8.3	9	V
	UCCx808–2	3.9	4.1	4.3	V
Hysteresis	UCCx808–1	3.5	4.2	5.1	V
	UCCx808–2	0.1	0.2	0.3	V

soft start section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
COMP rise time	FB = 1.8 V, rise from 0.5 V to 4 V		3.5	20	ms

overall section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Startup current	VDD < start threshold		130	260	μA
Operating supply current	FB = 0 V, CS = 0 V, See Note 5 and 6		1	2	mA
VDD zener shunt voltage	IDD = 10 mA, See Note 4	13	14	15	V

NOTES: 1. Measured at RC. Signal amplitude tracks VDD.

2. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}, 0 \le V_{CS} \le 0.4\ V,$

3. Parameter measured at trip point of latch with FB at 0V.
4. Start threshold and zener shunt threshold track one another.
5. For UCCx808–1, set VDD above the start threshold before setting at 10 V.
6. Does not include current in the external oscillator network.

pin descriptions

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC3808, a low impedance circuit board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak source current, and 1-A peak sink current.

The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

RC: The oscillator programming pin. The UCC3808's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 1 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula:

$$f_{OSCILLATOR} = \frac{1.41}{RC}$$

where frequency is in hertz, resistance in ohms, and capacitance in farads. The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ should be avoided.

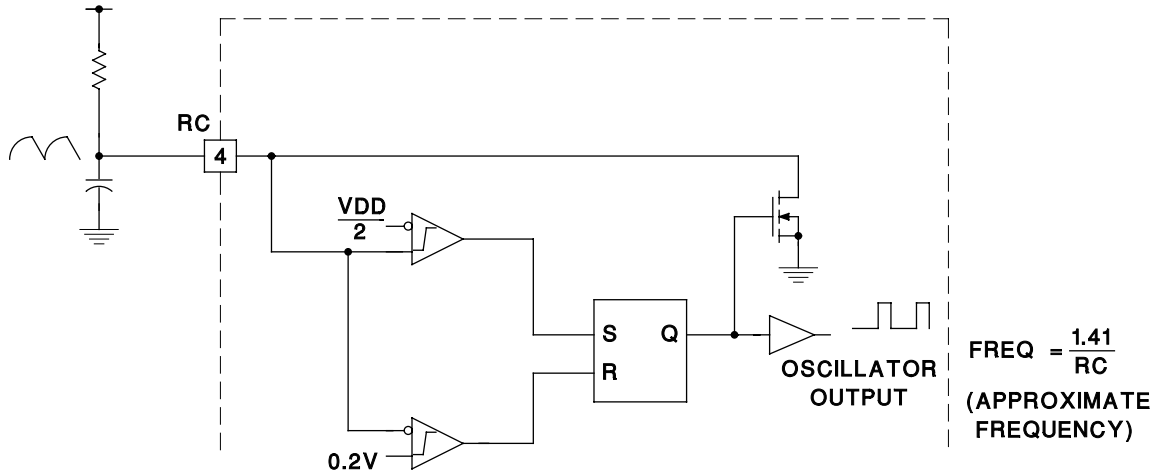
For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F, \text{ where F is frequency}$$

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1-μF decoupling capacitor is recommended.

pin descriptions (continued)



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NOTE: The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a ½ the oscillator frequency, with guaranteed duty cycle of < 50% for both outputs.

Figure 1. Block Diagram for Oscillator

APPLICATION INFORMATION

A 200-kHz push-pull application circuit with a full wave rectifier is shown in Figure 2. The output, V_O, provides 5 V at 75 W maximum and is electrically isolated from the input. Since the UCC3808 is a peak current mode controller the 2N2222A emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and a 1 µF is suggested as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the UC3965 Precision Reference with Low Offset Error Amplifier. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanicall strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer is a low profile design, EFD size 25, using Magnetics Inc. P material which is a good choice at this frequency and temperature. The input voltage may range from 36 V dc to 72 V dc.

APPLICATION INFORMATION

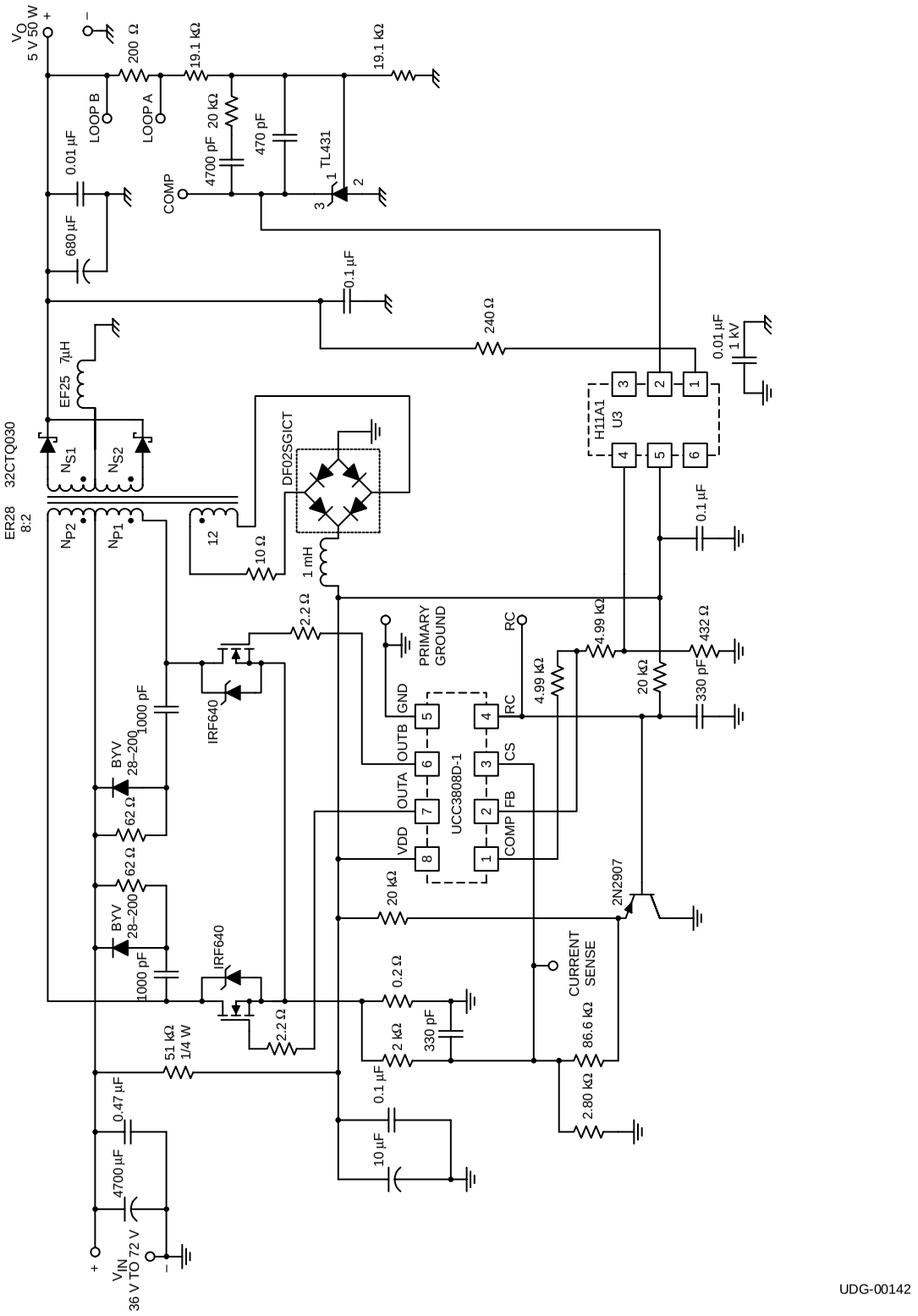


Figure 2. Typical Application Diagram: 48-V In, 5-V, 50-W Output

APPLICATION INFORMATION

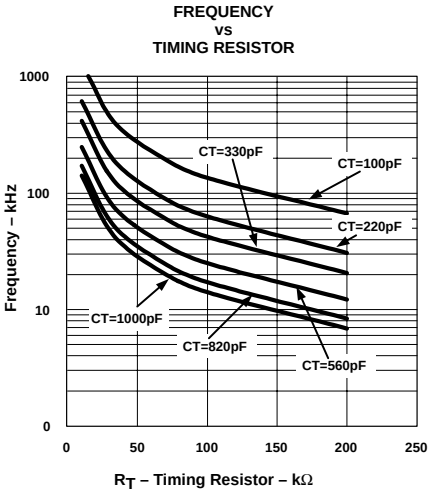


Figure 3

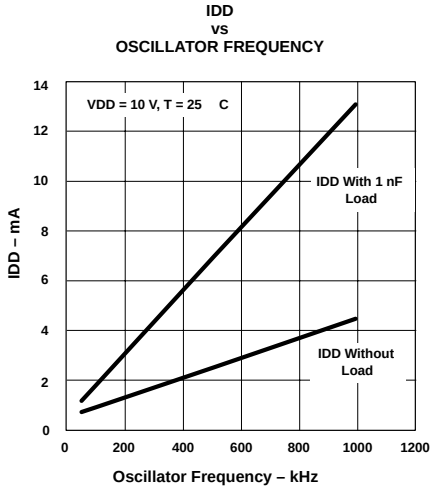


Figure 4

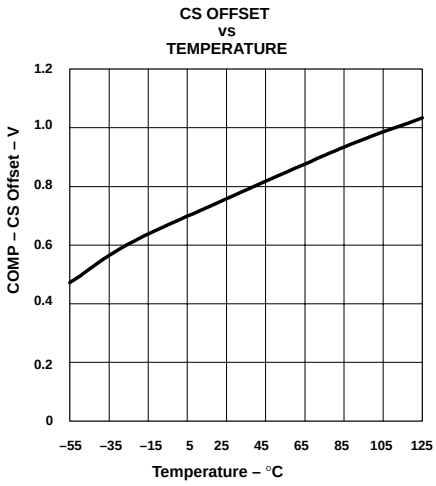


Figure 5

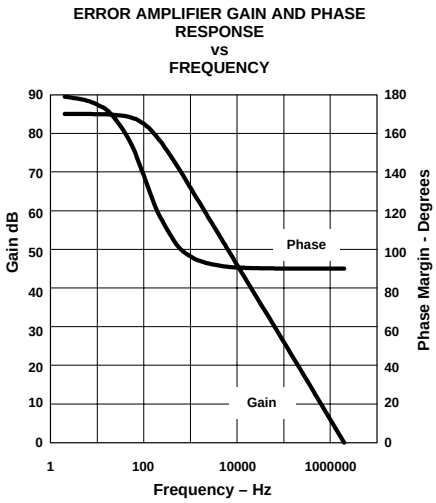


Figure 6

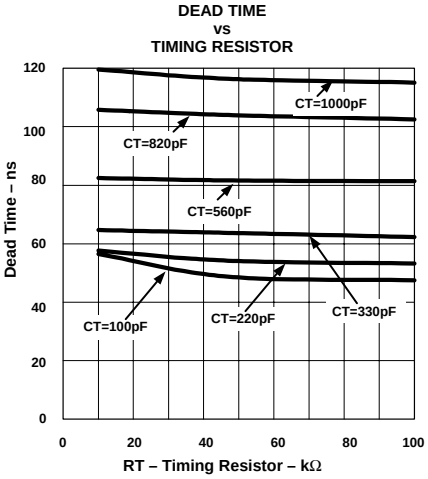


Figure 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC2808D-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808D-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808D-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808D-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808DTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808DTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808DTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808DTR-2G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2808N-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2808N-1G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2808N-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2808N-2G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3808D-1	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808D-1G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808D-2	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808D-2G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808DTR-1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808DTR-1G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808DTR-2	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808DTR-2G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC3808N-1	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3808N-1G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3808N-2	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3808N-2G4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

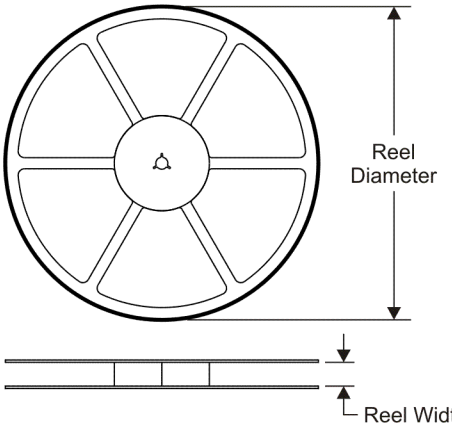
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF UCC3808-2 :
- Military: UCC1808-2

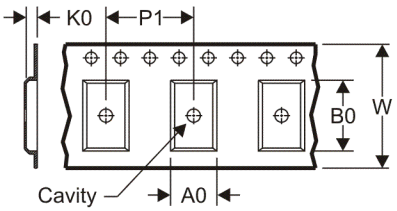
NOTE: Qualified Version Definitions:
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

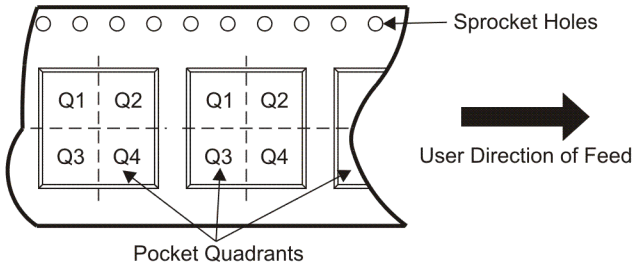


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

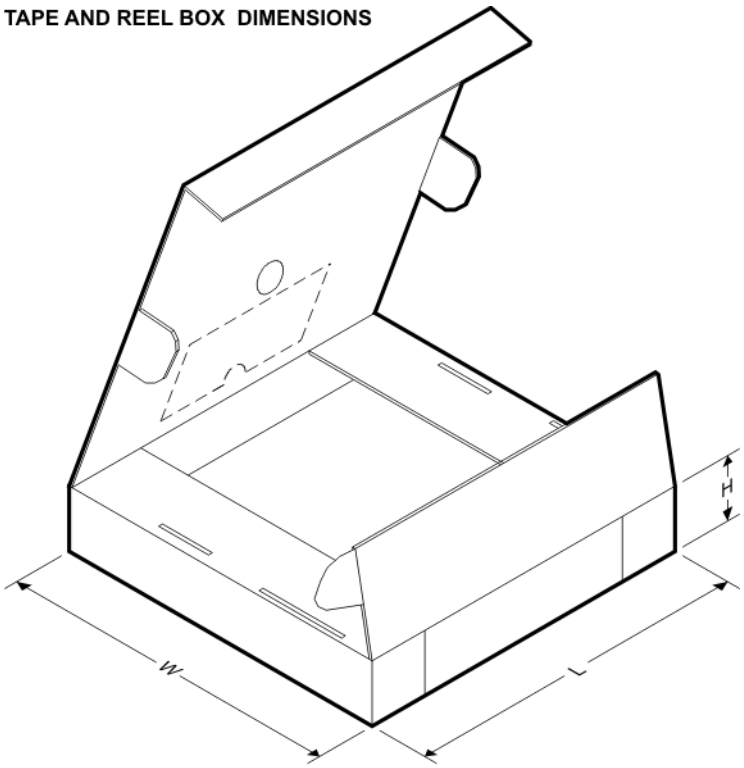
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

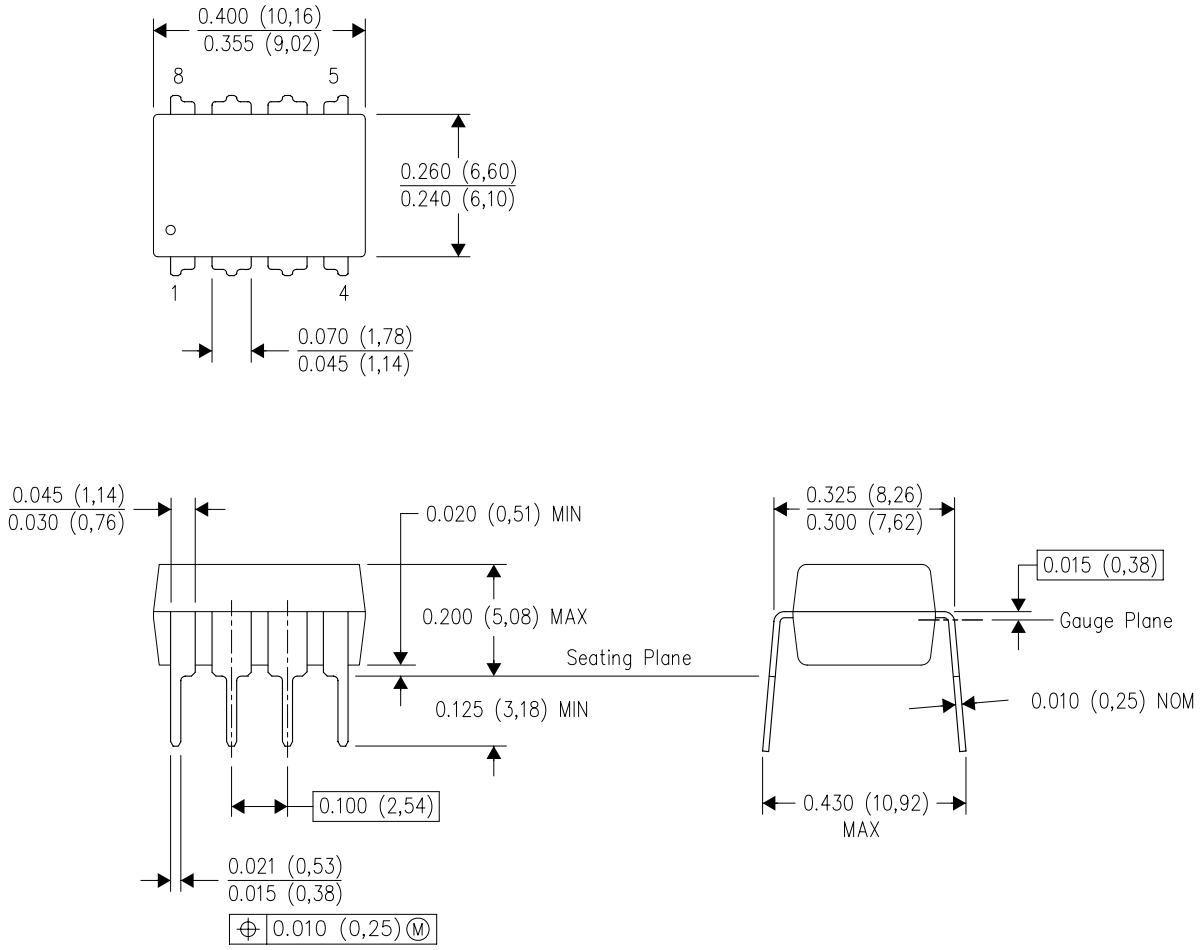
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

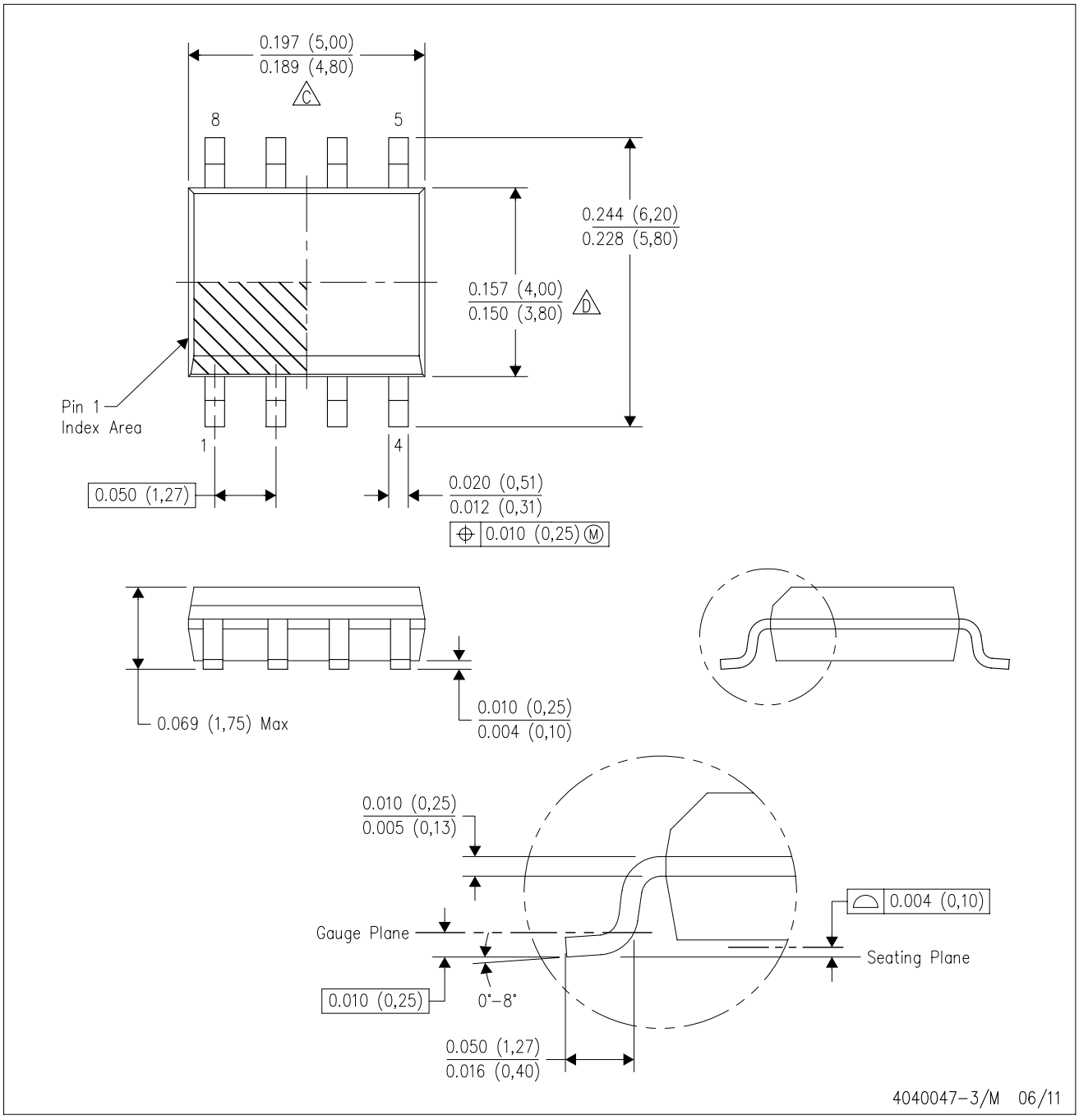
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808DTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808DTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808DTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808DTR-2	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



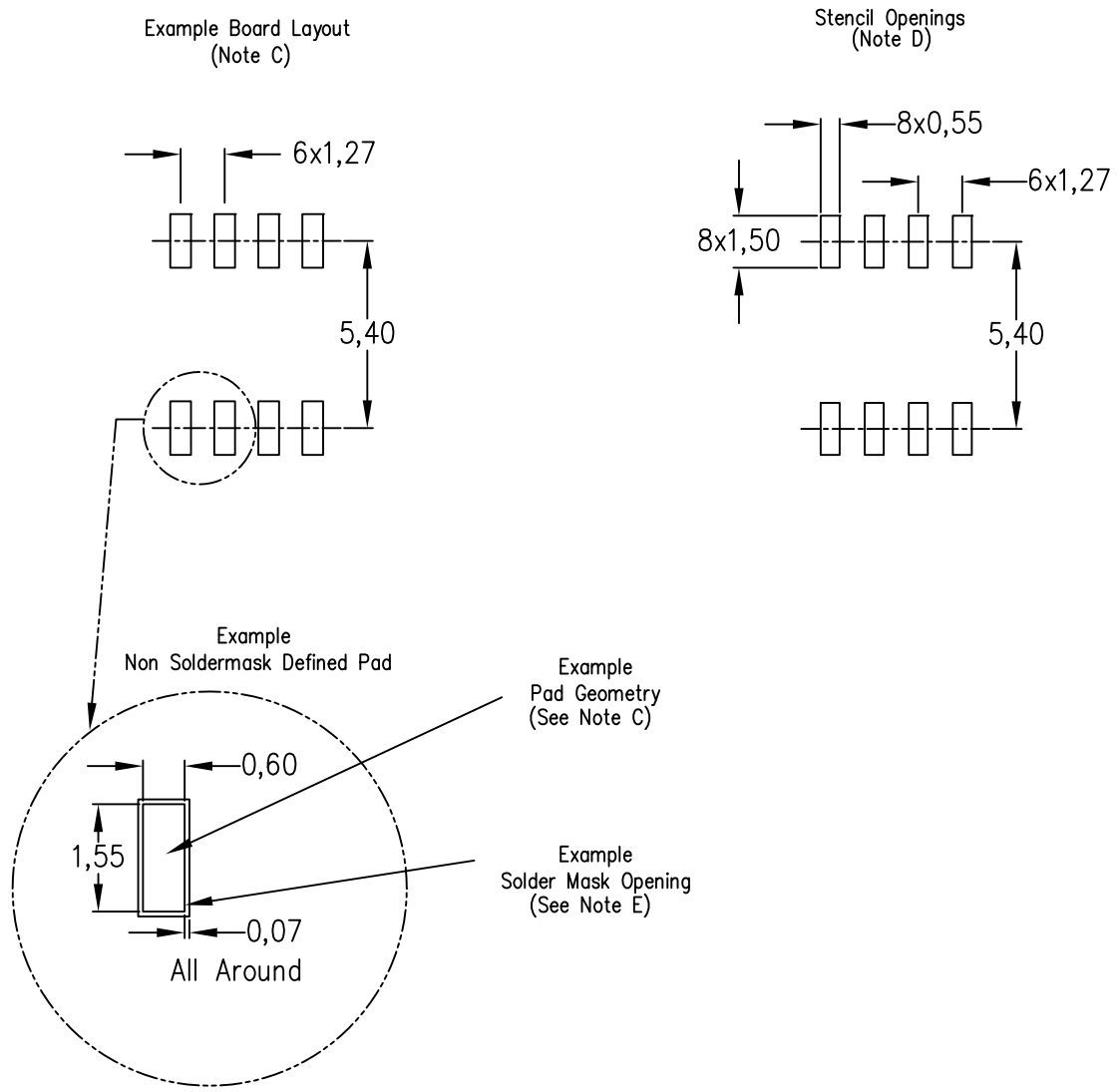
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



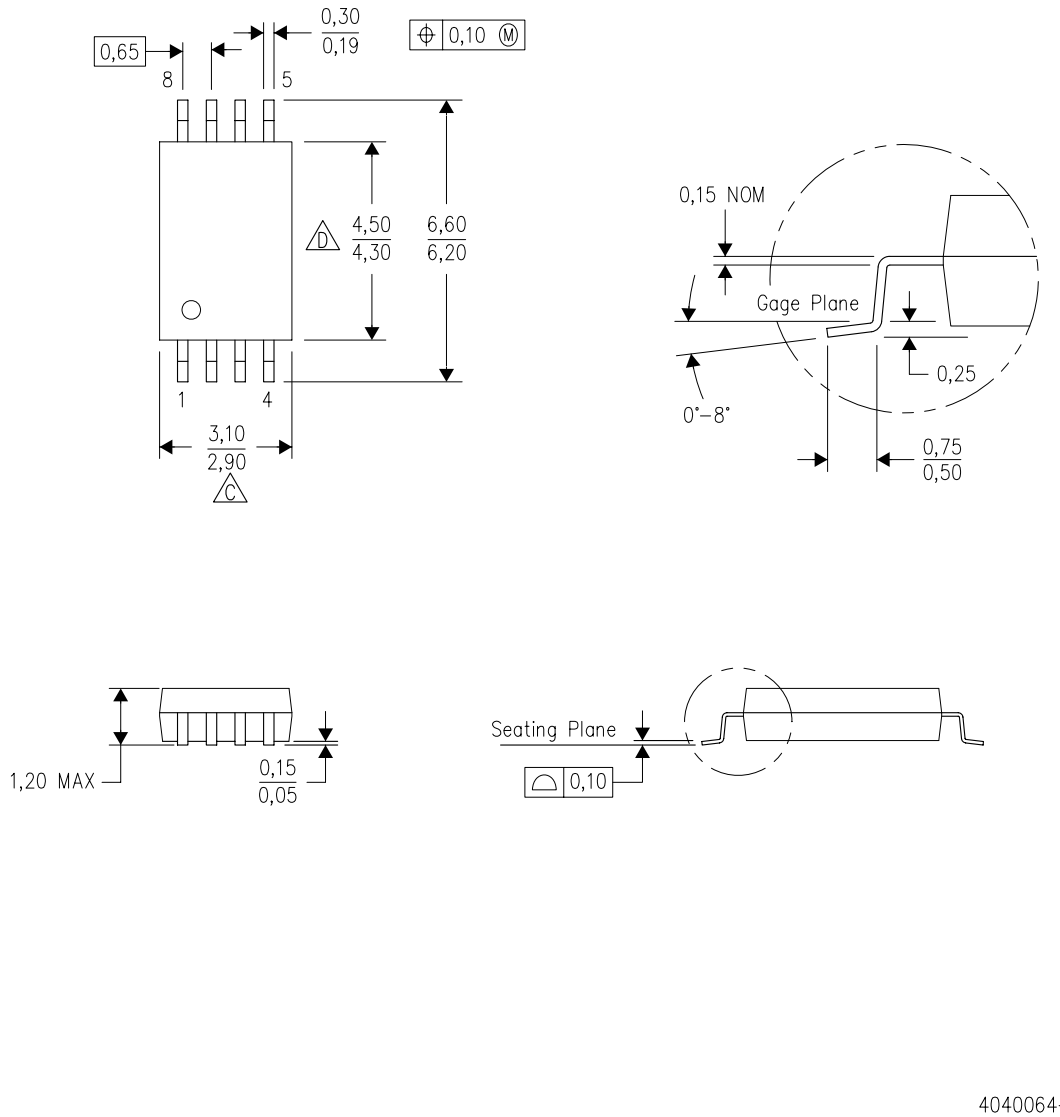
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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