

133 MHz Clock Generation for Pentium II/III Processors

Features

- Four copies of CPU Clock @ 133/100 MHz
- Eight copies of PCI Clock (Synchronous w/CPU Clock) including one free running PCI clock.
- Two copies of fixed frequencies 3.3V Clock @ 66 MHz
- Three copies of APIC Clock @ 16.667 MHz, synchronous to CPU Clock
- One copy of 48 MHz Clock
- Two copies of Ref. Clock @ 14.13818 MHz
- Ref. 14.31818 MHz Xtal Oscillator Input
- CPU Clock Frequency selection pin for selecting 133 MHz or 100 MHz operation
- Power Management Control Input Pins
- Supports Reliance (RCC) chip set
- Spread Spectrum enable/disable pin
- 56-pin SSOP (V56) package

Pin Configuration

VSS	1	56	VDD2V
REF0	2	55	APIC2
REF1	3	54	APIC1
VDD3V	4	53	APIC0
XTAL_IN	5	52	VSS
XTAL_OUT	6	51	VDD2V
VSS	7	50	NC
PCICLK_F	8	49	NC
PCICLK1	9	48	VSS
VDD3V	10	47	VDD2V
PCICLK2	11	46	CPUCLK3
PCICLK3	12	45	CPUCLK2
VSS	13	44	VSS
PCICLK4	14	43	VDD2V
PCICLK5	15	42	CPUCLK1
VDD3V	16	41	CPUCLK0
PCICLK6	17	40	VSS
PCICLK7	18	39	VDD3V
VSS	19	38	VSS
VSS	20	37	PCISTOP#
3V66_0	21	36	CPUSTOP#
3V66_1	22	35	PWRDWN#
VDD3V	23	34	SPREAD#
VSS	24	33	SEL1
NC	25	32	SEL0
NC	26	31	VDD3V
VDD3V	27	30	48MHz
SEL133/100#	28	29	VSS

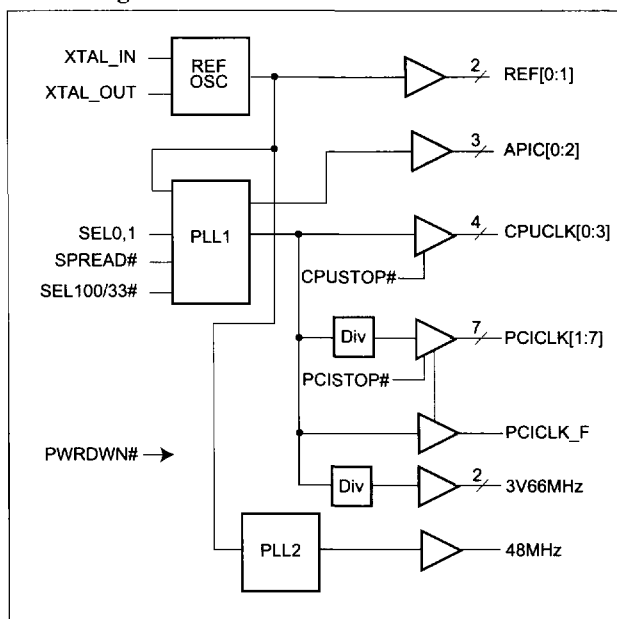
Description

The PI6C133, a low-skew, low-jitter 133 MHz clock generator, is specifically designed to meet all the clocking requirements for 133 MHz and 100 MHz desktops with high-performance and lower-power features.

Split power supplies of 2.5V and 3.3V are used to reduce power consumption, minimize noise and to ensure CPU independence. The 2.5V supply is used to power CPUCLK clocks to the processor module. 2.5V signalling is compliant to JEDEC standard 8-X. The rest of the circuitry is powered by a 3.3V supply.

Key features, such as power-management and spread-spectrum functions, are fully supported. PWRDWN# signal will turn off all internal circuits and keep all outputs to a low state, making the power consumption less than 100µA. For less stringent power requirements, CPUSTOP# will turn off CPUCLK and 3V66 outputs instantaneously. Spread spectrum function can be optionally disabled by pulling SPREAD# pin to a HIGH state.

Block Diagram



Pin Description

Pin	Symbol	I/O	Functional Description
2,3	REF [0:1]	O	3.3V 14.318 MHz clock output
5	XTAL_IN	I	14.318 MHz Crystal input
6	XTAL_OUT	O	14.318 MHz Crystal output
8	PCICLK_F	O	3.3V Free Running PCI clock
9,11,12,14,15,17,18	PCICLK[1-7]	O	3.3V PCI Clock Outputs
21,22	3V66 [0-1]	O	3.3V Fixed 66 MHz Clock Outputs
28	SEL133/100#	I	3.3 LVTTTL compatible input for 133 MHz or 100 MHz CPU Outputs. H = 133 MHz L = 100 MHz
30	48MHz	O	3.3V Fixed 48 MHz Clock output
32,33	SEL[0-1]	I	3.3 LVTTTL compatible input for logic selection function
34	SPREAD#	I	3.3 LVTTTL compatible input. Enables spread spectrum mode when held LOW
35	PWRDWN#	I	3.3 LVTTTL compatible input. Device Enters Powerdown mode when held LOW
36	CPUSTOP#	I	3.3 LVTTTL compatible input. Stops all CPUCLK and 3V66 clocks when held LOW.
37	PCISTOP#	I	3.3 LVTTTL compatible input. Stops all PCI clocks except PCICLK_F when held LOW.
41,42,45,46	CPUCLK[0-3]	O	2.5V Host Bus Clock output. 133 MHz or 100 MHz depending on state of SEL133/100#.
53,54,55	APIC[0-2]	O	2.5V Clock outputs running divide synchronous with the CPU (Host bus) clock frequency. Fixed 16.67 MHz limit. If CPU = 133 MHz, APIC = CPU/8 If CPU = 100 MHz, APIC = CPU/6
4,10,16,23,27,31,39	V _{DD3V}	3.3V Power	3.3V power supply
1,7,13,19,20,24,29 38,40,44,48,52	V _{SS}	V _{SS}	Ground
43,47,51,56	V _{DD2V}	2.5V Power	2.5V power
25,26,49,50	NC		Unused

APIC and PCI Clock Outputs Must Be Synchronous with CPUCLK

PCICLK outputs tracks CPUCLK very closely. The CPUCLKs lead the PCICLKs by 1.5 - 4.0ns with assuming they are fully loaded with the appropriate loads. The frequency of PCICLK is fixed at 33.33MHz. PCICLK is CPUCLK divided by four @ 133.33MHz, or CPUCLK divided by three @ 100.0 MHz.

APIC clocks are now synchronous with the CPUCLK outputs. The IOAPIC voltage will track that of the Host bus and will have maximum frequency of 16.67 MHz. APIC clocks will be derived by dividing the CPUCLK outputs by eight when the Host bus is 133.33 MHz, and by six when the Host bus is 100 MHz. APIC clocks will lag the Host bus clocks by 1.5 - 4.0ns at the maximum device load of 20pF.

PI6C133-03 Select Functions

SEL133/100#	SEL1	SEL0	Function
0	0	0	All outputs Tri-State
0	0	1	(Reserved)
0	1	0	Active 100 MHz, 48 MHz PLL inactive
0	1	1	Active 100 MHz, 48 MHz PLL active
1	0	0	Test Mode
1	0	1	(Reserved)
1	1	0	Active 133 MHz, 48 MHz PLL inactive
1	1	1	Active 133 MHz, 48 MHz PLL active

PI6C133-03 Truth Table

SEL 133/100#	SEL1	SEL0	CPU	3V66	PCI	48 MHz	REF	APIC	Notes
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1
0	0	1	n/a	n/a	n/a	n/a	n/a	n/a	
0	1	0	100 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	2
0	1	1	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	3,6,7
1	0	0	TCLK/2	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	4,5
1	0	1	n/a	n/a	n/a	n/a	n/a	n/a	
1	1	0	133 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	2
1	1	1	133 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	3,6,7

Notes:

1. Required for board-level "bed of nails" testing.
2. 48 MHz PLL disabled to reduce component jitter.
48 MHz outputs are held H-Z instead of driven to a LOW state.
3. "Normal" mode of operation.
4. TCLK is a test clock over driven on the XTAL_IN input during test mode. TCLK mode is based on 133 MHz CPU select logic.
5. For DC output impedance verification.
6. Range of reference frequency allowed is min = 14.316 nominal = 14.31818 MHz, max = 14.32 MHz.
7. Frequency accuracy of 48 MHz must be +167PPM to match USB default.

The power-down controller provides a signal that is latched with its own copy of the PCI clock.

Clock sequencing always guarantees full clock timing parameters after the system has initially powered up, except where noted. During power-up and power-down operations using the PWRDWN# select pin, partial clocks are not allowed and all clock timing parameters are met except for the following: the first clock pulse coming out of a stopped clock condition could be slightly distorted because of the other clock network charging requirements: it is also understood that board routing and signal loading have a large impact on the initial clock distortion.

V_{DD}3V Power-Down Removal

The PI6C133-03 device meets the following requirement to allow for a common design across multiple platforms.

To allow for multiple devices in platforms to share voltage regulators, the PI6C133-03 allows the removal of power from the V_{DD}3V voltage pins during the following specific condition. (Leakage currents from the V_{DD}3V and V_{DD}2V pins are not allowed to violate existing powerdown# specifications.)

Going to Powerdown Mode:

1. Assert the PWRDWN# signal to the PI6C133-03.
2. Remove power from the 3.3V pins of the PI6C133-03.
3. All input pins of PI6C133-03 will be either powered down or driven to ground.
4. V_{DD}3 power plane will be pulled to or discharge to < 250mV.
5. The 2.5V pins will remain powered at 2.5V.

To Restore Power:

1. Apply 3.3V to the PI6C133-03.
2. Wait 200-2000ms.
3. De-assert the PWRDWN# signal.
4. Wait 1ms longer than lock time specified for the device.
5. Continue operation as normal

PI6C133-03 Clock Enable Configuration

CPUSTOP#	PWRDWN#	PCISTOP#	CPUCLK	APIC	3V66	PCI	PCI_F	REF, 48 MHz	Osc	VCOs
X	0	X	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
0	1	0	LOW	ON	LOW	LOW	ON	ON	ON	ON
0	1	1	LOW	ON	LOW	ON	ON	ON	ON	ON
1	1	0	ON	ON	ON	LOW	ON	ON	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON	ON

Notes:

1. LOW means outputs held static LOW as per latency requirement below.
2. ON means active.
3. PWRDWN# pulled LOW, impacts all outputs including REF and 48 MHz outputs.
4. All 3V66 as well as all CPU clocks should stop cleanly when CPUSTOP# is pulled LOW.
5. APIC, REF, 48 MHz signals are not controlled by the CPUSTOP# functionality and are enabled all in all conditions except PWRDWN# = LOW.

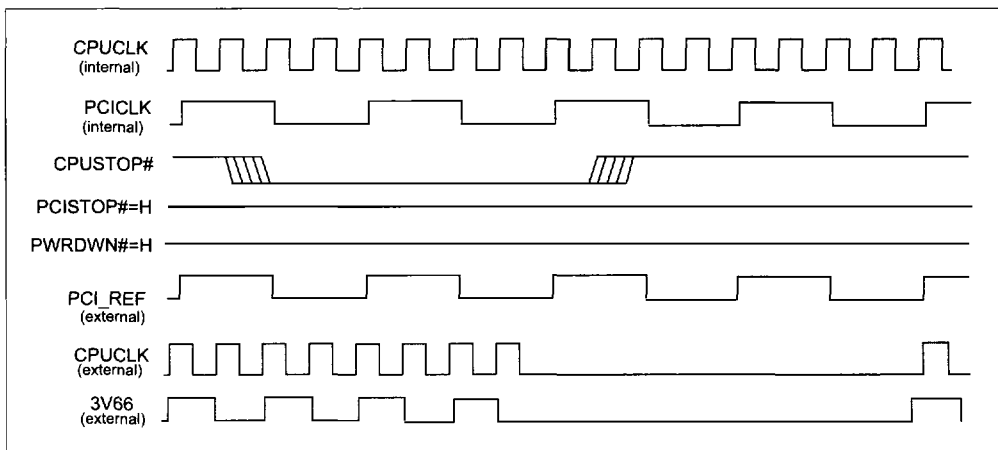
PI6C133-03 Power Management Requirements

Signal	Signal State	Latency
		No. of rising edges of PCICLK
CPUSTOP#	0 (Disabled)	1
	1 (Enabled)	1
PCISTOP#	0 (Disabled)	1
	1 (Enabled)	1
PWRDWN#	1 (Normal Operation)	3ms
	0 (Power Down)	2 max.

Notes:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWRDWN# goes inactive (high) to when the first valid clocks are driven from the device.

CPUSTOP# is an input to the clock synthesizer. It is used to turn off the CPU and 3V66 clocks for low power operation. CPUSTOP# is asserted asynchronously by the external clock control logic with the rising edge of the free running PCI clock (and hence CPU clock) and must be internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. **ONLY one rising edge of the PCI_F is allowed** after the clock control logic switched for both the CPU and 3V66 outputs to become enabled/disabled.

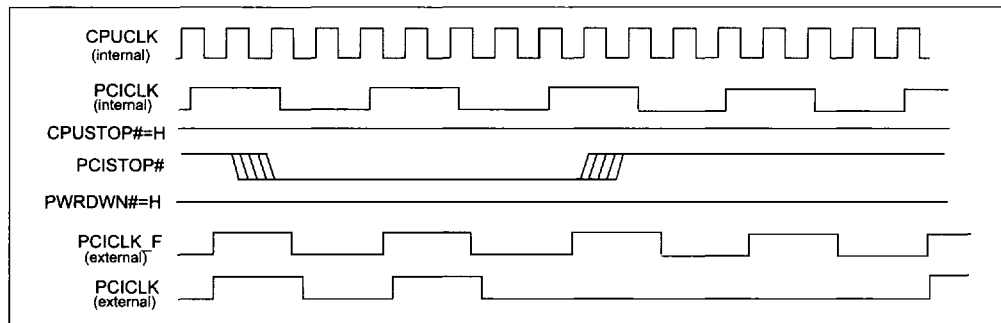


PI6C133-03 CPUSTOP# Timing Diagram

Notes:

1. All internal timing is referenced to the CPUCCLK
2. The internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. CPUSTOP# signal is an input signal that must be made synchronous to free running PCI_F
4. 3V66 clocks also stop/start before
5. PWRDWN# and PCISTOP# are shown in a high state.
6. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

PCISTOP# is an input to the clock synthesizer and is made synchronous to the clock driver PCI_F output. It is used to turn off the PCI clocks for low-power operation. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. **ONLY one rising edge of PCI_F is needed** after the clock control logic switched for the PCI outputs to become enabled/disabled.

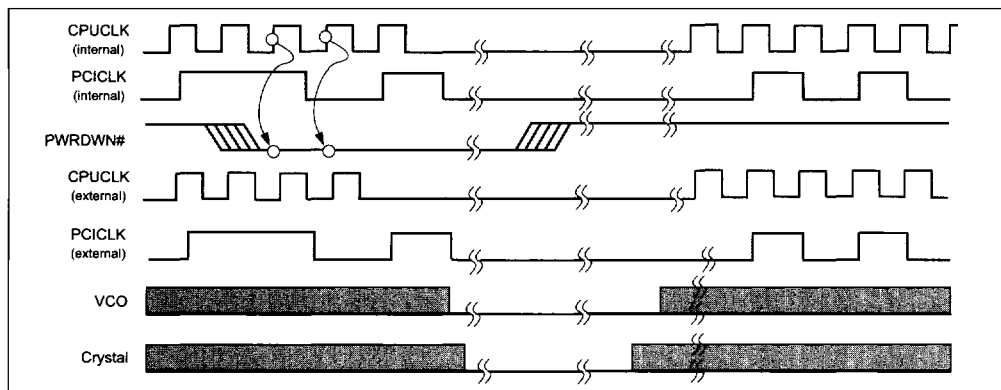


PI6C133-03 PCISTOP# Timing Diagram

Notes:

1. All internal timing is referenced to the CPUCLK
2. PCISTOP# signal is an input signal which is made synchronous to PCI_F output.
3. Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PWRDWN# and CPUSTOP# are shown in a high state.
6. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

The power-down selection is used to put the part into a very low power state without turning off the power to the part. PWRDWN# is an asynchronous active low input. The signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PWRDWN# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PWRDWN# is active low all clocks need to be driven to a low value and held prior to turning off the VCO's and the crystal. The power-up latency is less than 3ms. The power-down latency is short and conforms to the sequence requirements shown below. PCISTOP# and CPUSTOP# are considered to be don't cares during power-down operations. REF and 48 MHz clocks are expected to be stopped in the LOW state as soon as possible. Owing to the state of internal logic stopping and holding REF clock outputs in the LOW state, more than one clock cycle may be required to complete.



PI6C133-03 PWRDWN# Timing Diagram

Notes:

1. All internal timing is referenced to the CPUCLK
2. Internal means inside the chip.
3. PWRDWN# is an asynchronous input and metastable conditions could exist.
This signal is required to be synchronized inside the part.
4. The shaded sections on the VCO and the crystal signals indicate an active clock.
5. Diagrams shown with respect to 133 MHz. Similar operation when CPU is 100 MHz.

DC Specifications

DC parameters must be sustainable under steady state (DC) conditions

Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units
Vdd3V Vdd2V	Supply Voltage	-0.5	4.6	V
T _S	Storage Temperature	-65	150	°C

Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units
V _{IH3} ⁽¹⁾	3.3V Input High Voltage	-0.5	4.6	V
V _{IL3}	3.3V Input Low Voltage	-0.5		
ESD prot. ⁽²⁾	Input ESD protection	2000		

Notes:

1. Maximum V_{IH} is not to exceed maximum V_{DD}.
2. Human body model.

DC Operating Requirements

Symbol	Parameter	Condition	Min.	Max.	Units
Vdd3V	3.3 Supply Voltage ⁽⁴⁾	3.3V ±5%	3.135	3.465	V
Vdd2V	2.5V Supply Voltage ⁽⁴⁾	2.5V ±5%	2.375	2.625	
Vdd3V = 3.3V ±5%					
V _{IH3}	3.3V Input High Voltage ⁽⁷⁾	Vdd3	2.0	Vdd+0.3	V
V _{IL3}	3.3V Input Low Voltage ⁽⁷⁾		V _{SS} -0.3	0.8	
I _{IL}	Input Leakage Current ^(3,7)	0 < V _{IN} < Vdd3V	-5	+5	µA
Vdd2V = 2.5V ±5%					
V _{OH2}	2.5V Output High Voltage ⁽¹⁾	I _{OH} = -1mA	2.0		V
V _{OL2}	2.5V Output Low Voltage ⁽¹⁾	I _{OL} = 1mA		0.4	
Vdd3V = 3.3V ±5%					
V _{OH3}	3.3V Output High Voltage ⁽¹⁾	I _{OH} = -1mA	2.4		V
V _{OL3}	3.3V Output Low Voltage ⁽¹⁾	I _{OL} = 1mA		0.4	

DC Operating Requirements (continued)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{DD3V} = 3.3V ± 5%					
V _{POH}	PCI Bus Output High Voltage ⁽¹⁾	I _{OH} = -1mA	2.4		V
V _{POL}	PCI Bus Output Low Voltage ^(1,4)	I _{OL} = 1mA		0.55	
C _{IN}	Input Pin Capacitance			5	pF
C _{XTAL}	Xtal Pin Capacitance ⁽⁵⁾		13.5	22.5	
C _{OUT}	Output Pin Capacitance			6	
L _{PIN}	Pin Inductance			7	nH
T _A	Ambient Temperature	No Airflow	0	70	°C

Notes:

1. Signal edge is required to be monotonic when transitioning through this region.
2. Input leakage Current does not include inputs with Pull-up or Pull-down resistors.
3. No power sequencing is implied or allowed to be required in the system.
4. Conforms to 5V PCI Signaling specification.
5. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal.
6. All inputs referenced to 3.3V power supply.

Buffer Specifications

Buffer Name	V _{CC} Range (V)	Impedance (Ohms)	Buffer Type
CPU, APIC	2.375 - 2.625	13.5 - 45	Type 1
48MHz, REF	3.135 - 3.465	20 - 60	Type 3
PCI, 3V66	3.135 - 3.465	12 - 55	Type 5

Type 1 Buffer Characteristics
Operating Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{OHMIN}	Pull-Up Current ⁽¹⁾	V _{OUT} = 1.0V	-27			mA
I _{OHMAX}	Pull-Up Current ⁽¹⁾	V _{OUT} = 2.375V			-27	
I _{OLMIN}	Pull-Down Current ⁽¹⁾	V _{OUT} = 1.2V	27			
I _{OLMAX}	Pull-Down Current ⁽¹⁾	V _{OUT} = 0.3V			30	
T _{RH}	2.5V Type1 Output Rise Edge Rate ⁽²⁾	2.5V ±5% @ 0.4V -2.0V	1/1		4/1	V/ns
T _{FH}	2.5V Type1 Output Fall Edge Rate ⁽²⁾	2.5V ±5% @ 2.0V-0.4V	1/1		4/1	

Notes:

1. Production testing is expected to be a subset of characterization testing.
2. Output Rise and Fall time.
3. Receiver logic thresholds are V_{IL} = 0.7 and V_{IH} = 1.7V
4. R_{ON} 13.5-45 Ohm with a 29 Ohm nominal driver impedance.
5. R_{ON} = V_{OUT}/I_{OH}, V_{OUT}/I_{OL} measured at V_{CC}/2.

Type 3 Buffer Characteristics
Operating Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{OHMIN}	Pull-Up Current ⁽¹⁾	V _{OUT} = 1.0V	-29			mA
I _{OHMAX}	Pull-Up Current ⁽¹⁾	V _{OUT} = 3.135V			-23	
I _{OLMIN}	Pull-Down Current ⁽¹⁾	V _{OUT} = 1.95V	29			
I _{OLMAX}	Pull-Down Current ⁽¹⁾	V _{OUT} = 0.4V			27	
T _{RH}	3.3V Type 3 Output Rise Edge Rate ⁽²⁾	3.3V ±5% @ 0.4V -2.4V	0.5		2.0	V/ns
T _{FH}	3.3V Type 3 Output Fall Edge Rate ⁽²⁾	3.3V ±5% @ 2.4 - 0.4V	0.5		2.0	

Notes:

1. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time.
3. Receiver logic thresholds are V_{IL} = 0.8 and V_{IH} = 2.0V.
4. R_{ON} 20 -60 Ohm with a 40 Ohm nominal driver impedance.
5. R_{ON} = V_{OUT}/I_{OH}, V_{OUT}/I_{OL} measured at V_{CC}/2.

Type 5 Buffer Characteristics
Operating Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{OHMIN}	Pull-Up Current ⁽¹⁾	V _{OUT} = 1.0V	-33			mA
I _{OHMAX}	Pull-Up Current ⁽¹⁾	V _{OUT} = 3.135V			-33	
I _{OLMIN}	Pull-Down Current ⁽¹⁾	V _{OUT} = 1.95V	30			
I _{OLMAX}	Pull-Down Current ⁽¹⁾	V _{OUT} = 0.4V			38	
T _{RH}	3.3V Type 4 Output Rise Edge Rate ⁽²⁾	3.3V ±5% @ 0.4V -2.4V	1/1		4/1	V/ns
T _{FH}	3.3V Type 4 Output Fall Edge Rate ⁽²⁾	3.3V ±5% @ 2.4V -0.4V	1/1			

Notes:

1. Production testing is expected to be a subset of characterization testing.
2. Output Rise and Fall time.
3. Output rise and fall time must be guaranteed across V_{CC}, process and temperature range.
4. Receiver logic thresholds are V_{IL} = 0.8 and V_{IH} = 2.0 Volts
5. R_{ON} 12 -55 Ohm with a 30 Ohm nominal driver impedance.
6. R_{ON} = V_{OUT}/I_{OH}, V_{OUT}/I_{OL} measured at V_{CC}/2.
7. See PCI specification for additional PCI details



AC Timing

Host Bus AC Timing Requirements

Symbol	Parameter	133 MHz Host		100 MHz Host		Units
		Min.	Max.	Min.	Max.	
TPeriod	Host /CPU CLK Period ^(1,8)	7.5	8.0	10.0	10.5	ns
THIGH	Host /CPU CLK High Time ^(4,9)	1.87	N/A	3.0	N/A	
TLOW	Host /CPU CLK Low Time ^(5,9)	1.67	N/A	2.8	N/A	
TRISE	Host /CPU CLK Rise Time ⁽⁷⁾	0.4	1.6	0.4	1.6	
TFALL	Host /CPU CLK Fall Time ⁽⁷⁾	0.4	1.6	0.4	1.6	
TPeriod	APIC CLK Period ^(1,8)	60.0	64.0	60.0	64.0	ns
THIGH	APIC CLK High Time ^(4,9)	25.5	N/A	25.5	N/A	
TLOW	APIC CLK Low Time ^(5,9)	25.3	N/A	25.3	N/A	
TRISE	APIC CLK Rise Time ⁽⁷⁾	0.4	1.6	0.4	1.6	
TFALL	APIC CLK Fall Time ⁽⁷⁾	0.4	1.6	0.4	1.6	
TPeriod	3V66 CLK Period ^(1,3,8)	15.0	16.0	15.0	16.0	ns
THIGH	3V66 CLK High Time ^(4,9)	5.25	N/A	5.25	N/A	
TLOW	3V66 CLK Low Time ^(5,9)	5.05	N/A	5.05	N/A	
TRISE	3V66 CLK Rise Time ⁽⁷⁾	0.4	1.6	0.4	1.6	
TFALL	3V66 CLK Fall Time ⁽⁷⁾	0.4	1.6	0.4	1.6	
TPeriod	PCI CLK Period ^(1,2,8)	30.0	N/A	30.0	N/A	ns
THIGH	PCICLK High Time ^(4,9)	12.0	N/A	12.0	N/A	
TLOW	PCI CLK Low Time ^(5,9)	12.0	N/A	12.0	N/A	
TRISE	PCI CLK Rise Time ⁽⁷⁾	0.5	2.0	0.5	2.0	
TFALL	PCI CLK Fall Time ⁽⁷⁾	0.5	2.0	0.5	2.0	
tpZL, tpZH	Output Enable Delay (All outputs)	1.0	10.0	1.0	10.0	ns
tpLZ, tpZH	Output Disable Delay (All outputs)	1.0	10.0	1.0	10.0	
tstable	All Clock Stabilization from Power -Up ⁽⁶⁾		3		3	ns

Notes:

1. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @1.5V for 3.3V clocks.
2. The PCICLK clock is the Host clock divided by four at Host = 133 MHz. 3V66 clock internal VCO frequency divided by three for Host = 100 MHz
3. 3V66 is internal VCO frequency divided by four for Host = 133 MHz. 3V66 Clock is internal VCO frequency divided by three for Host = 100 MHz
4. T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
5. T_{LOW} is measured at 0.4V for all outputs.
6. The time specified is measured from when V_{DDQ} achieves its nominal operating level (typical condition V_{DDQ} = 3.3V) until the frequency output is stable and operating with in specification.
7. T_{RISE} and T_{FALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.0V (1mA) JEDEC Specification.
8. The average period over any 1μs period of time is greater than the minimum specified period.
9. Calculated at minimum edge rate(1V/ns) to guarantee 45/55% duty-cycle. Pulsewidth is required to be wider at faster edge-rate to ensure duty cycle specification is met.

Group Skew and Jitter Limits

Output Group	Pin-Pin Skew	Cycle-Cycle Jitter	Duty Cycle	Nom Vdd	Skew, Jitter Measure Point
CPU	175ps	150ps	45/55	2.5V	1.25V
APIC	500ps	250ps	45/55		
48MHz	N/A	500ps	45/55	3.3V	1.5V
3V66	250ps	500ps	45/55		
PCI	500ps	500ps	45/55		
REF	N/A	1000ps	45/55		

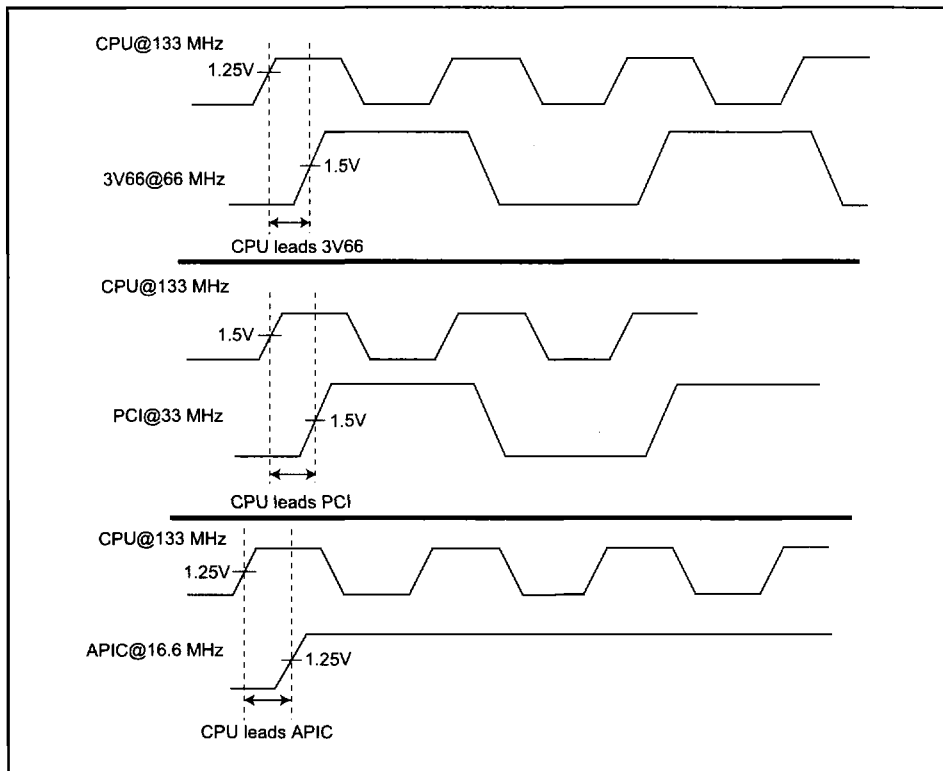
Group Offset Limits

Group	Offset	Measurement Loads (Lumped)	Measure Points
CPU to 3V66	0.0-1.5ns CPU Leads	CPU@20pF, 3V66@30pF	CPU@1.25V, 3V66@1.5V
CPU to PCI	1.5-4.0ns CPU Leads	3V66@30pF, CPU@30pF	3V66@1.5V, PCI@1.5V
CPU to APIC	1.5-4.0ns CPU Leads	CPU@20pF, APIC@20pF	CPU@1.25V, APIC@1.5V

Notes:

1. All offsets are to be measured at rising edges

Only offset specifications listed above are guaranteed/tested. The specification is treated as ANY output within the first specified bank to ANY output of the specified bank. Pin-pin skew is implied within offset specification, jitter is not. Previous offset specifications such as CPU to PCI offset are no longer required.



Group Offset Waveforms

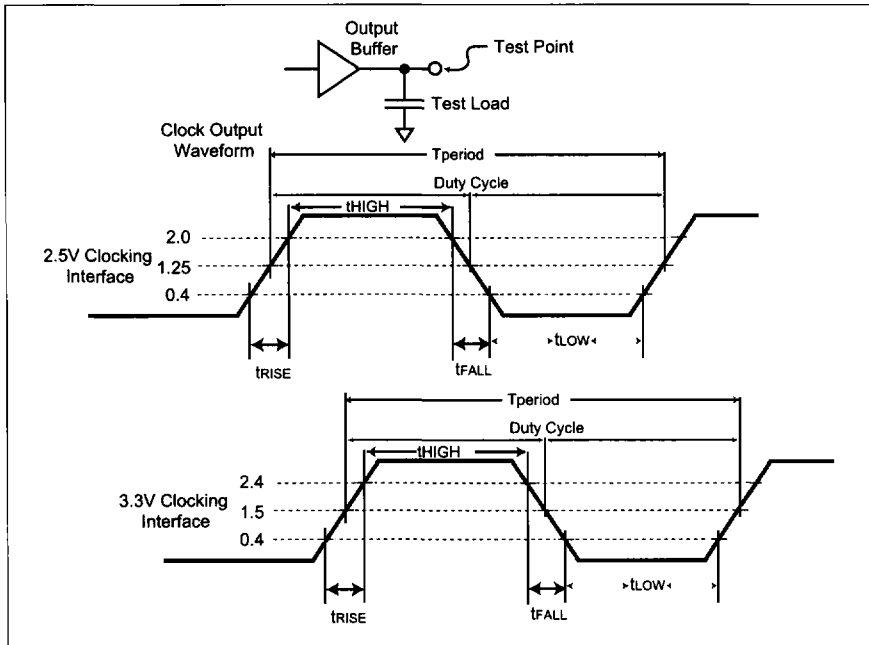
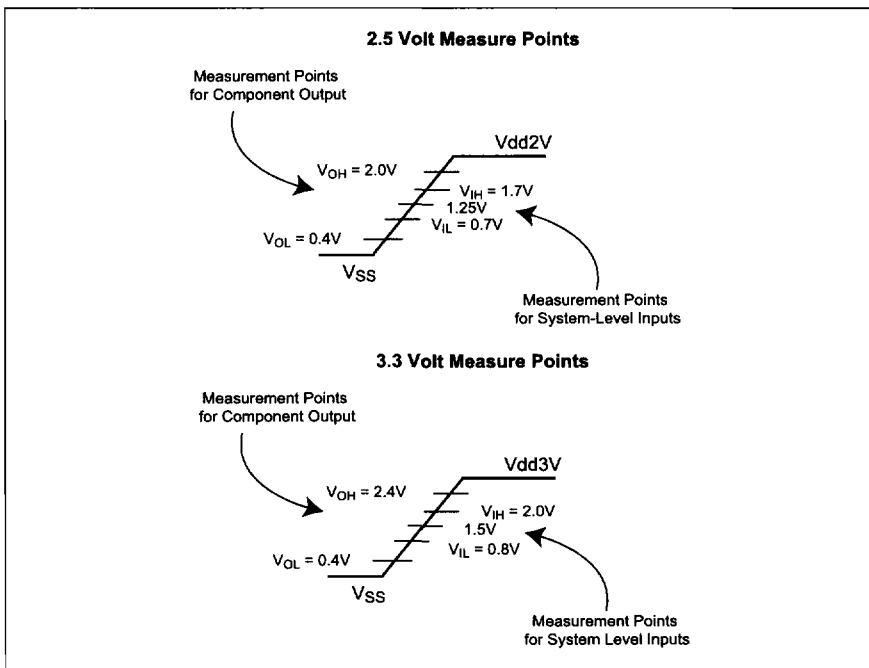
Test and Measurement

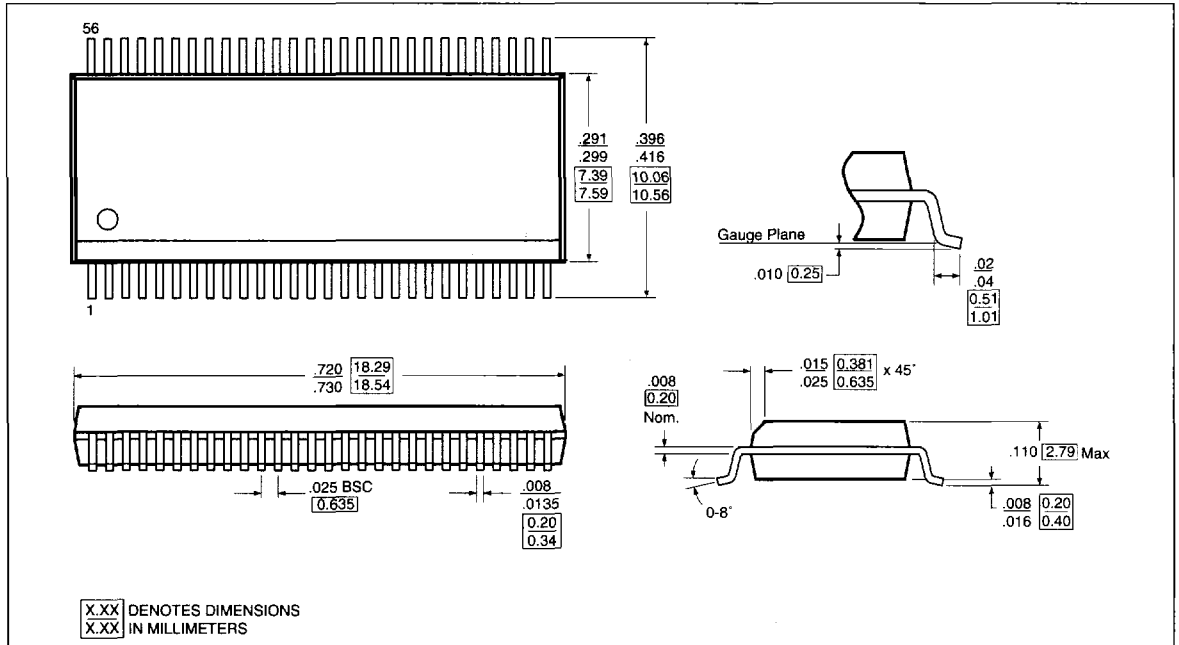
Minimum and Maximum Lumped Capacitive Test Loads

Clock	Min. Load	Max. Load	Units	Notes
CPUCLK	10	20	pF	1 device load, possible 2 loads
PCICLK		30		Must meet PCI 2.1 requirements
3V66		30		1 device load, possible 2 loads
48MHz Clock		20		1 device load
REF		20		1 device load
APIC		20		1 device load

Notes:

1. Maximum rise/fall times are guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. Testing may be done with an additional 500Ω resistor in parallel, if properly correlated with the capacitive load.


PI6C133-03 Clock Waveforms

PI6C133-03 Component versus System Measure Points

56-pin SSOP Package Data

Ordering Information

Pin Number	Description
PI6C133-03V	56-pin SSOP Package