Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841/2841AT/BT/CT/DT

FEATURES:

- **Common features:**
  - A, B, C and D speed grades
  - Low input and output leakage ≤1µA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT841T:**
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for FCT2841T:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise

DESCRIPTION:

The IDT54/74FCT8xx series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT841AT/BT/CT/DT bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841/2841AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '373 function. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT8xx high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

The IDT54/74FCT2841AT/BT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall-times-reducing the need for external series terminating resistors. The IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

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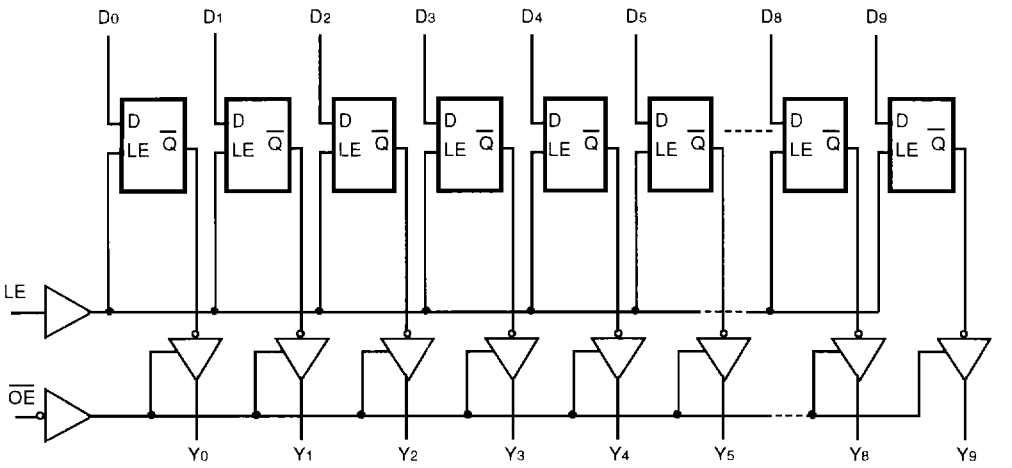
FUNCTIONAL BLOCK DIAGRAM



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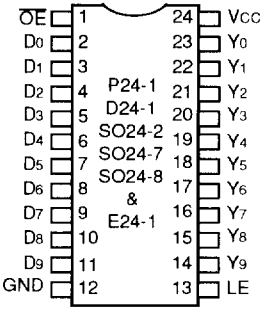
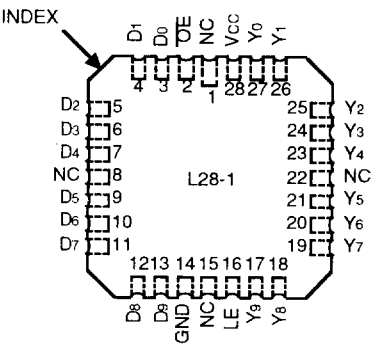
PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

2571 drw 02



LCC
TOP VIEW

2571 drw 03

PIN DESCRIPTION

Name	I/O	Description
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs V_I are in high-impedance (off) state.

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FUNCTION TABLE[1]

Inputs			Internal	Output	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE:
2571 tbl 02

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:
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1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
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1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT2841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
				FCTxxxT	—	1.8	4.5	
				FCT2xxxT		0.9	3.2	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	3.0	6.0[5]	
				FCT2xxxT	—	1.2	3.4[5]	
				FCTxxxT	—	5.0	14.0[5]	
				FCT2xxxT	—	3.2	11.4[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT841AT FCT2841AT				FCT841BT FCT2841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tSU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	ns
tW	LE Pulse Width HIGH[3]		4.0	—	5.0	—	4.0	—	4.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT841CT FCT2841CT				FCT841DT FCT2841DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	4.2	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	8.0	—	—	
tPLH tPHL	Propagation Delay LE to YI	CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	4.0	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	15.0	1.5	16.0	1.5	8.0	—	—	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.8	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	CL = 5pF[4] RL = 500Ω	1.5	5.7	1.5	6.0	1.5	4.0	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	6.3	1.5	4.0	—	—	
tSU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	2.5	—	2.5	—	1.5	—	—	—	ns
tH	Data to LE Hold Time		2.5	—	2.5	—	1.0	—	—	—	ns
tW	LE Pulse Width HIGH[3]		4.0	—	4.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

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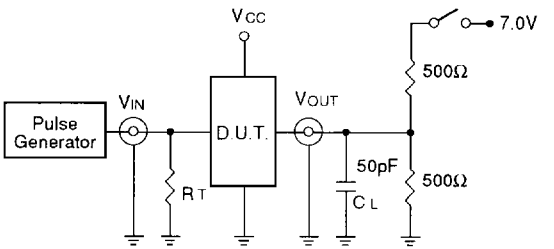
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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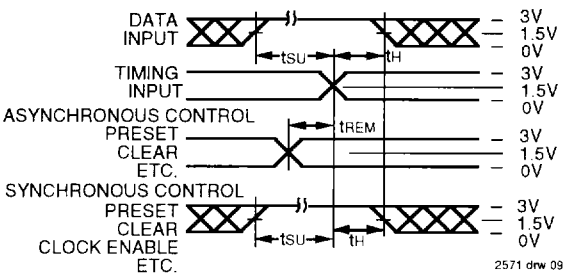
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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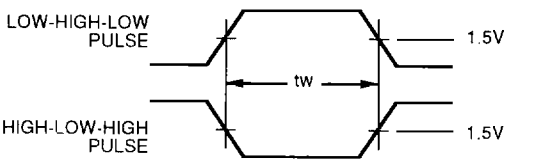
PULSE WIDTH



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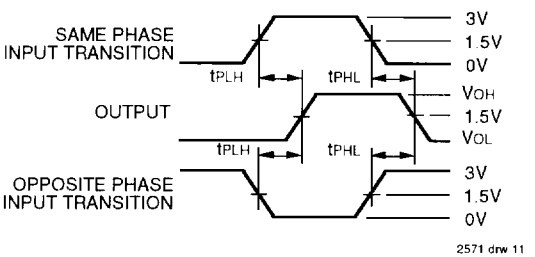
PROPAGATION DELAY



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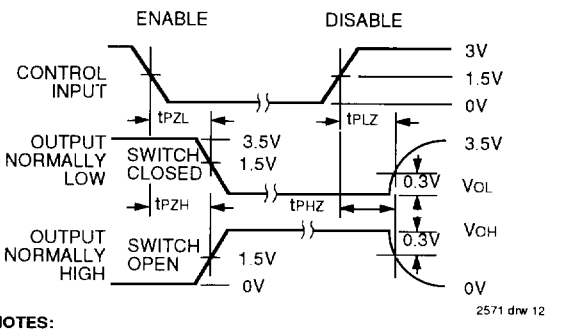
ENABLE AND DISABLE TIMES



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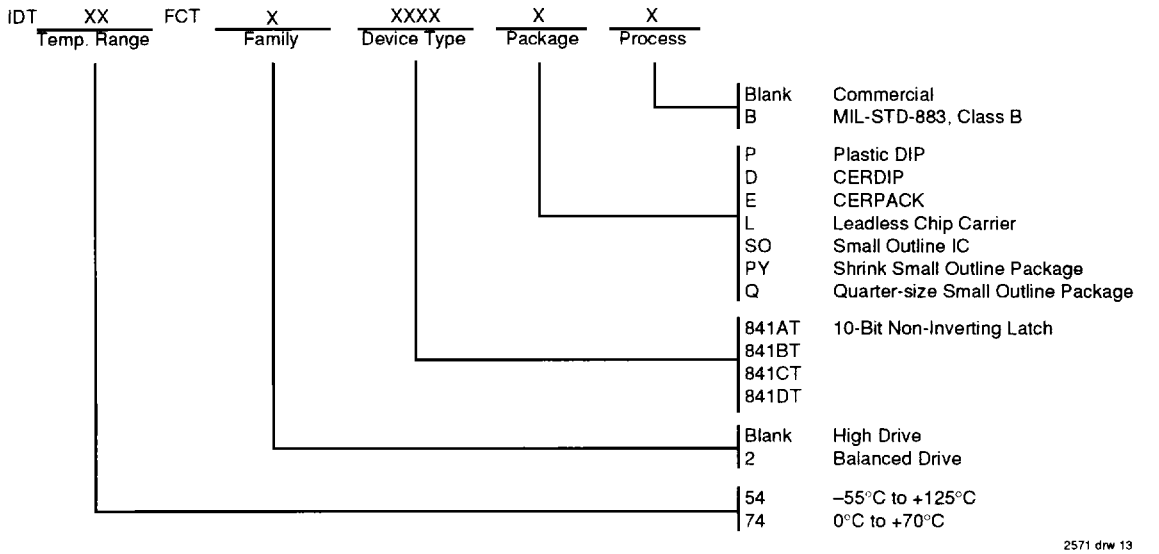
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



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