512Kx8 MONOLITHIC SRAM, SMD 5962-95613

FEATURES

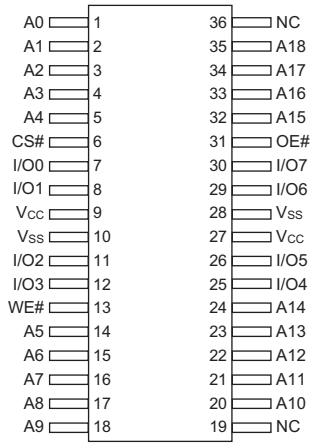
- Access Times 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 36 lead Ceramic SOJ (Package 100)
  - 36 lead Ceramic Flat Pack (Package 226)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Thinpack™ Flat Pack (Package 321)
- 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
- Commercial, Industrial and Military Temperature Range
- 5V Power Supply
- Low Power CMOS
- Low Power Data Retention for Battery Back-up Operation
- TTL Compatible Inputs and Outputs

*This product is subject to change without notice.

REVOLUTIONARY PINOUT

36 FLAT PACK
36 CSOJ

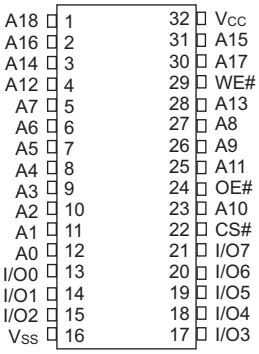
TOP VIEW



EVOLUTIONARY PINOUT

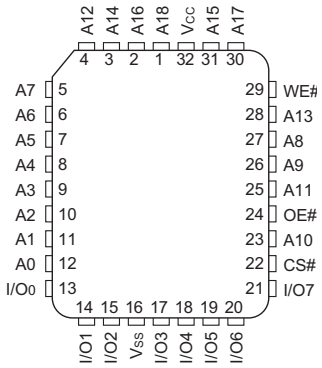
32 DIP
32 CSOJ (DE)
32 FLAT PACK (FF)

TOP VIEW



32 CLCC

TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O 0-7	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
VCC	+5.0V Power
GND	Ground

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature Range	T_{STG}	-65	+150	°C
Signal Voltage Range to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage Range (V_{CC})	V_{CC}	-0.5	7.0	V

Truth Table

CS#	OE#	WE#	MODE	DATA I/O	POWER
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Acvive

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil)	T_A	-55	+125	°C

Capacitance

(T_A = +25°C)

Parameter	Symbol	Conditions	Package	Speed (ns)	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz	32 pin CSOJ, DIP, Flat Pack Evolutionary	15 to 55	20	pF
			32 pin CLCC	15 to 55	15	pF
			36 pin CSOJ & Flat Pack Revolutionary	15 to 35	12	pF
				45 to 55	20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz	32 pin CSOJ, DIP, Flat Pack Revolutionary	15 to 55	20	pF
			36 pin CSOJ & Flat Pack Revolutionary	15 to 35	12	pF
				45 to 55	20	pF

This parameter is guaranteed by design but not tested.

DC Characteristics – CMOS Compatible

(V_{CC} = 5.0V, GND = 0V, -55°C ≤ TA ≤ 125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND TO V_{CC}		10	µA
Operating Supply Current*	I_{CC}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5,		160	mA
Standby Current	I_{SS}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		0.45	mA
Output Low Voltage	V_{OL}	I_{OL} = 6mA for 17 - 35ns, I_{OL} = 2.1mA for 45 - 55ns, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA for 17 - 35ns, I_{OH} = 1.0mA for 45 - 55ns, V_{CC} = 4.5	2.4		V

Data retention characteristics for low power "I" version

Parameter	Symbol	Conditions	Min	Max	Unit
Data Retention Supply Voltage	V_{DR}	CS#[3] V_{CC} -0.2V	2.0	5.5	V
Low Power Data Retention	I_{CCDR1}	V_{CC} = 3V		7	mA
Low Power Data Retention	I_{CCDR2}	V_{CC} = 2V		2	mA

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AC Characteristics

(V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t_{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		8		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t_{CLZ1}	2		2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t_{OLZ1}	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ1}		8		9		10		12		15		20		20	ns
Output Disable to Output in High Z	t_{OHZ1}		8		9		10		12		15		20		20	ns

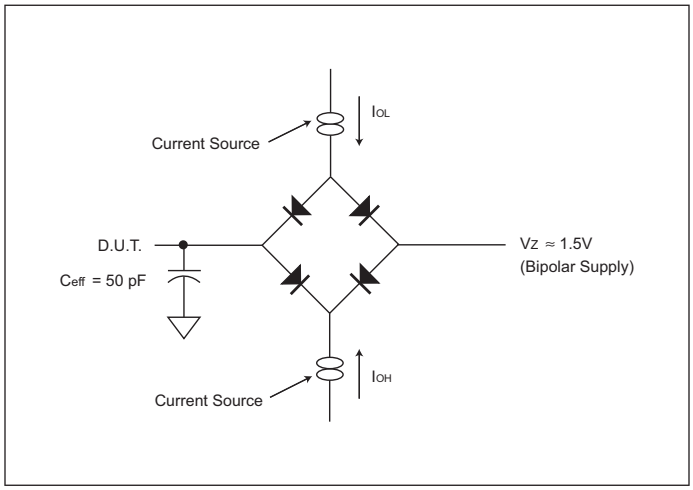
AC Characteristics

(V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ 125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	13		14		14		15		25		35		50		ns
Address Valid to End of Write	t_{AW}	13		14		14		15		25		35		50		ns
Data Valid to End of Write	t_{DW}	8		9		10		10		20		25		25		ns
Write Pulse Width	t_{WP}	13		14		14		15		25		35		40		ns
Address Setup Time	t_{AS}	2		2		2		2		2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		0		0		5		5		ns
Output Active from End of Write	t_{OW1}	2		2		3		4		4		5		5		ns
Write Enable to Output in High Z	t_{WHZ1}		8		9		9		10		15		20		25	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC Test Circuit



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

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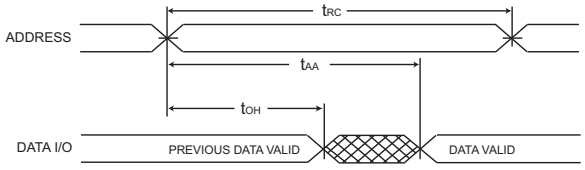
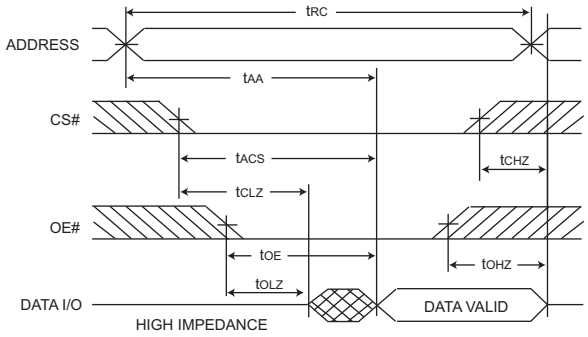
Rev. 14

TIMING WAVEFORM – READ CYCLE

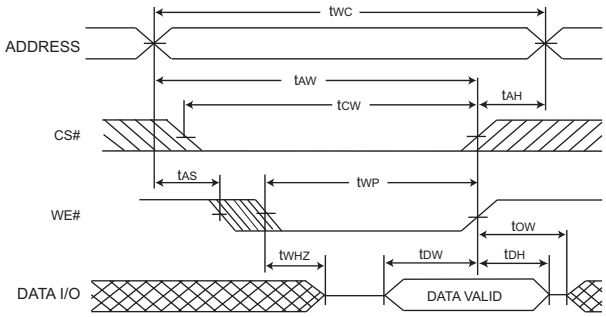


READ CYCLE 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



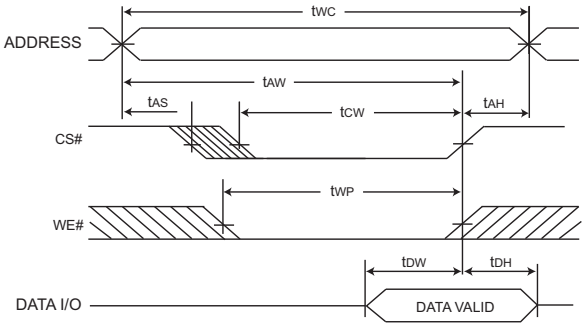
READ CYCLE 2 (WE# = V_{IH})

WRITE CYCLE – WE# CONTROLLED



WRITE CYCLE 1, WE# CONTROLLED

WRITE CYCLE – CS# CONTROLLED



WRITE CYCLE 2, CS# CONTROLLED

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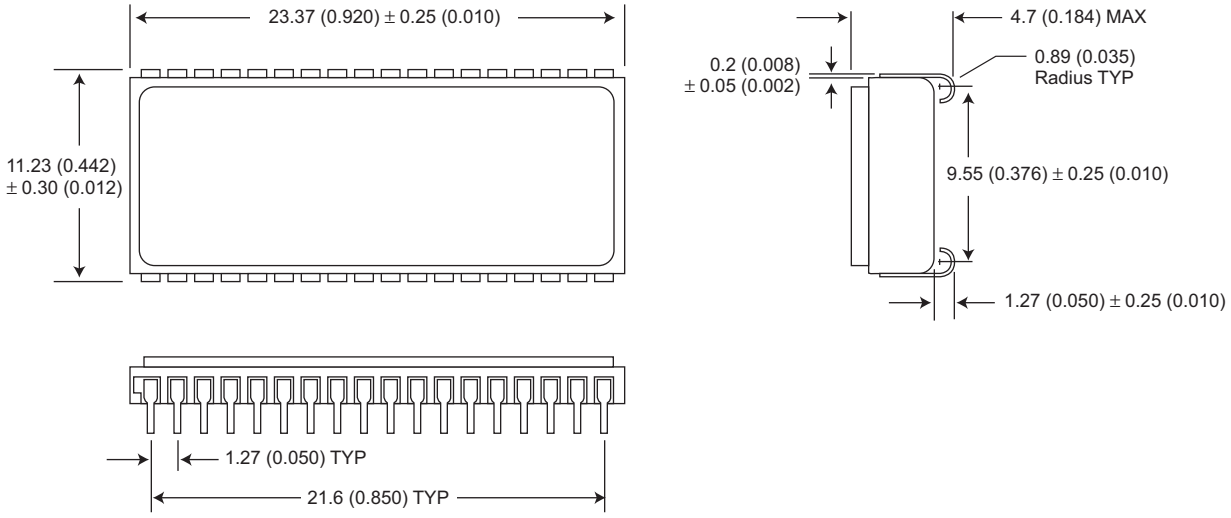
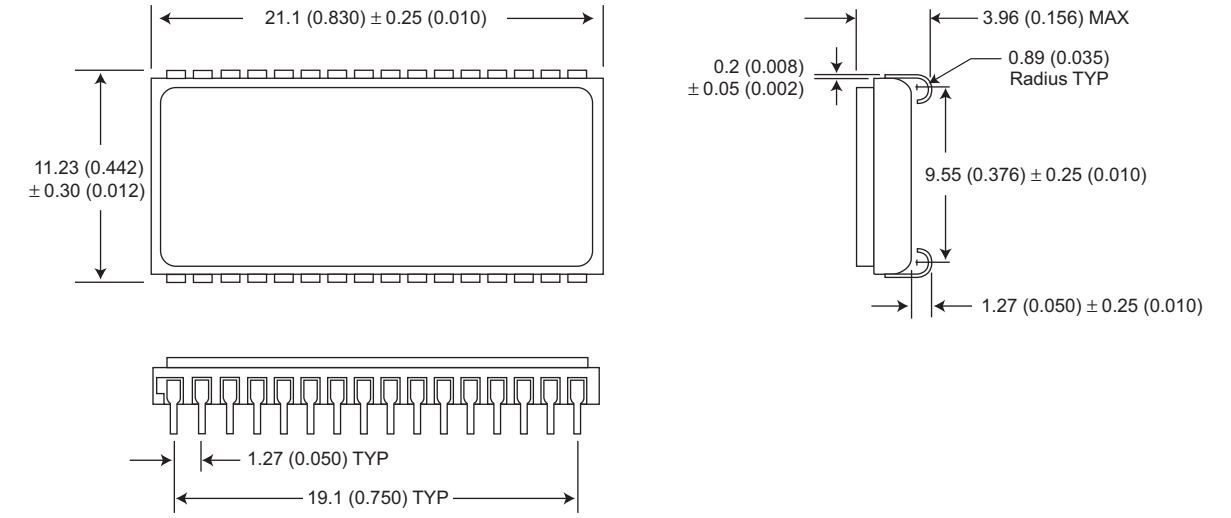
PACKAGE 100: 36 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 101: 32 LEAD, CERAMIC SOJ



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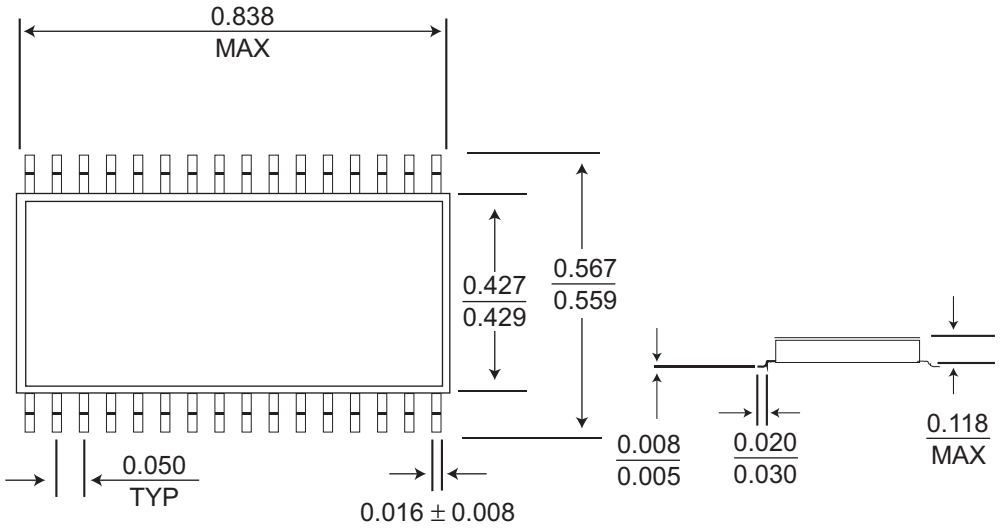
PACKAGE 321: 32 PIN CERAMIC THINPACK™ FLATPACK



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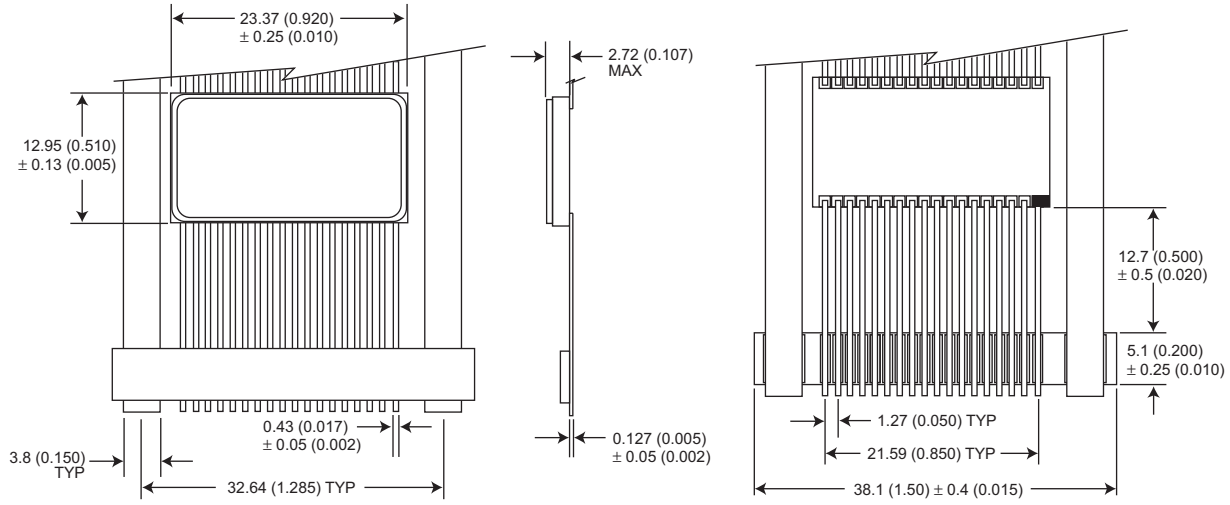
PACKAGE 226: 36 LEAD, CERAMIC FLAT PACK



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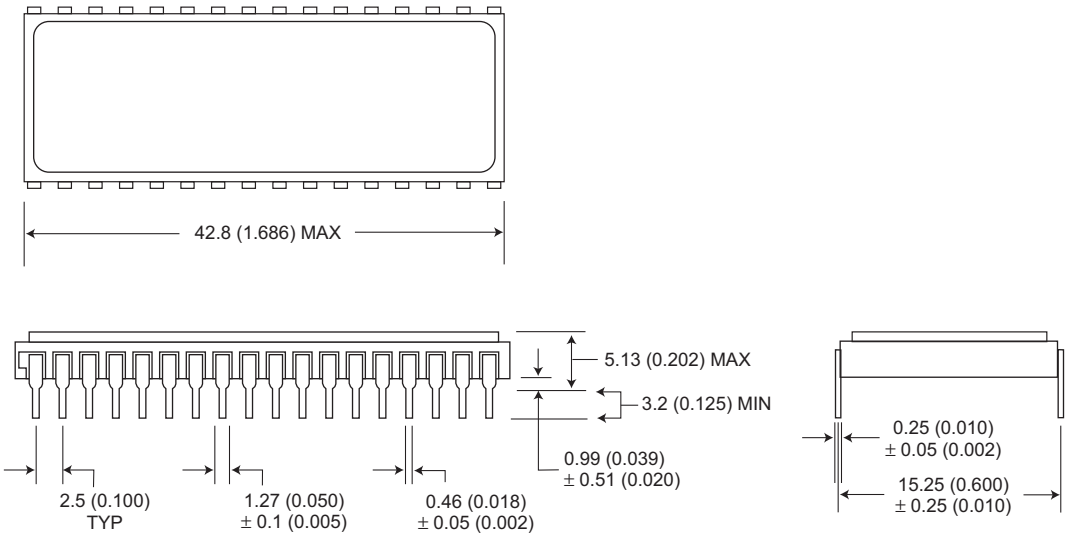
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

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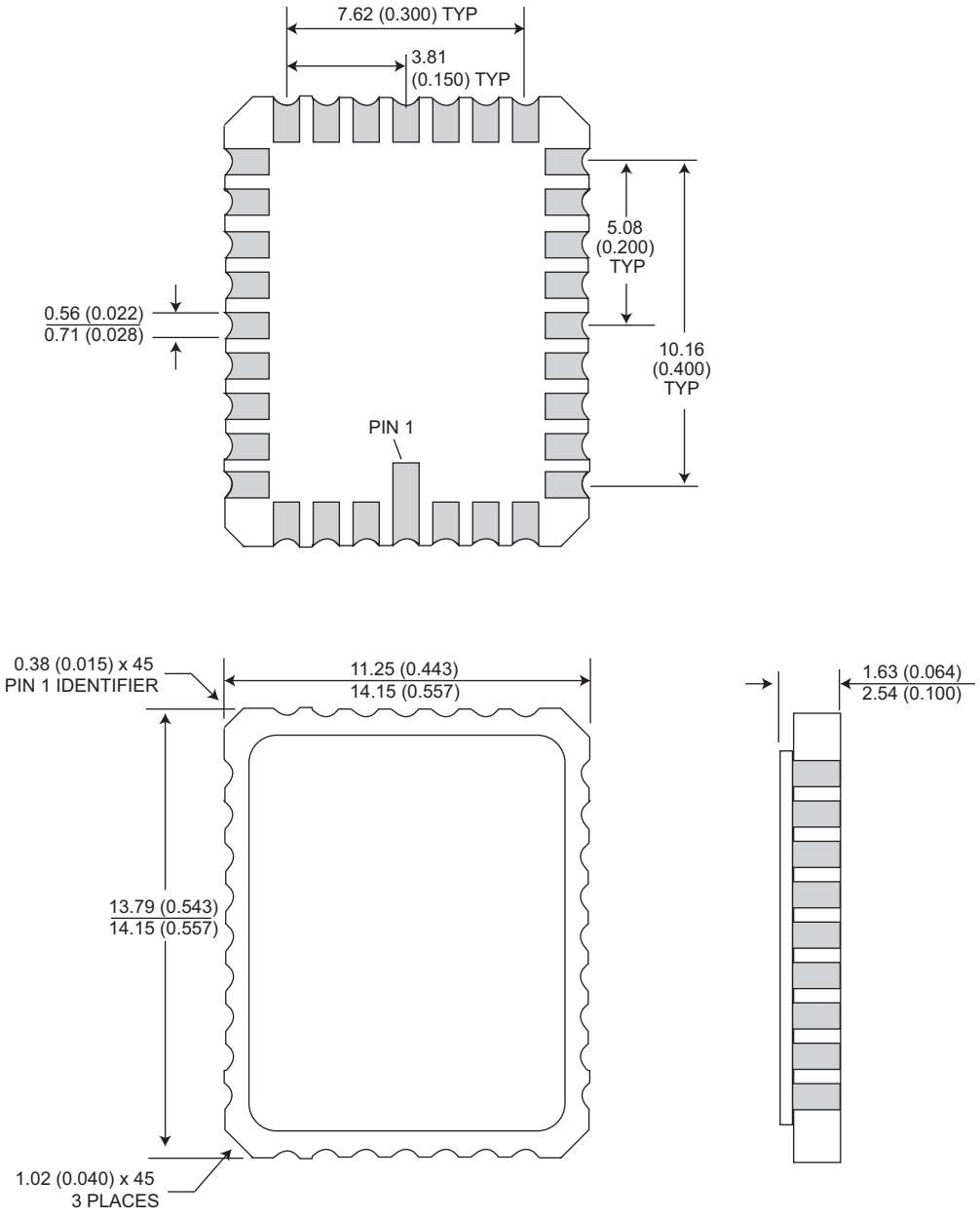
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

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ORDERING INFORMATION

W M S 512K 8 X - XXX X X X

MICROSEMI CORPORATION

MONOLITHIC

SRAM

ORGANIZATION, 512K x 8

IMPROVEMENT MARK:
- Blank = Standard
- L = Low Power Data Retention

ACCESS TIME (ns)

PACKAGE:
- C = 32 pin Ceramic 0.600” DIP (Package 300)
- CL = 32 pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
- DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
- DJ = 36 Lead Ceramic SOJ (Package 100)
- F = 36 Lead Ceramic Flat Pack (Package 226)
- FF = 32 Lead Ceramic Thinpack™ Flat Pack (Package 321)

DEVICE GRADE:
- Q = MIL-PRF-38534 Class H Compliant
- M = Military Screened -55°C ≤ T_A ≤ 125°C
- I = Industrial -40°C ≤ T_A ≤ 85°C
- C = Commercial 0°C ≤ T_A ≤ 70°C

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

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DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 8 SRAM Monolithic	55ns	32 pin DIP (C)	5962-95613 05HYX
512K x 8 SRAM Monolithic	45ns	32 pin DIP (C)	5962-95613 06HYX
512K x 8 SRAM Monolithic	35ns	32 pin DIP (C)	5962-95613 07HYX
512K x 8 SRAM Monolithic	25ns	32 pin DIP (C)	5962-95613 08HYX
512K x 8 SRAM Monolithic	20ns	32 pin DIP (C)	5962-95613 09HYX
512K x 8 SRAM Monolithic	17ns	32 pin DIP (C)	5962-95613 10HYX
512K x 8 SRAM Monolithic	15ns	32 pin DIP (C)	5962-95613 14HYX
512K x 8 SRAM Monolithic	55ns	32 lead SOJ Evol (DE)	5962-95613 05HTX
512K x 8 SRAM Monolithic	45ns	32 lead SOJ Evol (DE)	5962-95613 06HTX
512K x 8 SRAM Monolithic	35ns	32 lead SOJ Evol (DE)	5962-95613 07HTX
512K x 8 SRAM Monolithic	25ns	32 lead SOJ Evol (DE)	5962-95613 08HTX
512K x 8 SRAM Monolithic	20ns	32 lead SOJ Evol (DE)	5962-95613 09HTX
512K x 8 SRAM Monolithic	17ns	32 lead SOJ Evol (DE)	5962-95613 10HTX
512K x 8 SRAM Monolithic	15ns	32 lead SOJ Evol (DE)	5962-95613 14HTX
512K x 8 SRAM Monolithic	55ns	36 lead SOJ (DJ)	5962-95613 05HZX
512K x 8 SRAM Monolithic	45ns	36 lead SOJ (DJ)	5962-95613 06HZX
512K x 8 SRAM Monolithic	35ns	36 lead SOJ (DJ)	5962-95613 07HZX
512K x 8 SRAM Monolithic	25ns	36 lead SOJ (DJ)	5962-95613 08HZX
512K x 8 SRAM Monolithic	20ns	36 lead SOJ (DJ)	5962-95613 09HZX
512K x 8 SRAM Monolithic	17ns	36 lead SOJ (DJ)	5962-95613 10HZX
512K x 8 SRAM Monolithic	15ns	36 lead SOJ (DJ)	5962-95613 14HZX
512K x 8 SRAM Monolithic	55ns	36 lead Flatpack (F)	5962-95613 05HXX
512K x 8 SRAM Monolithic	45ns	36 lead Flatpack (F)	5962-95613 06HXX
512K x 8 SRAM Monolithic	35ns	36 lead Flatpack (F)	5962-95613 07HXX
512K x 8 SRAM Monolithic	25ns	36 lead Flatpack (F)	5962-95613 08HXX
512K x 8 SRAM Monolithic	20ns	36 lead Flatpack (F)	5962-95613 09HXX
512K x 8 SRAM Monolithic	17ns	36 lead Flatpack (F)	5962-95613 10HXX
512K x 8 SRAM Monolithic	15ns	36 lead Flatpack (F)	5962-95613 14HXX

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Document Title

512Kx8 MONOLITHIC SRAM, SMD 5962-95613

Revision History

Rev #	History	Release Date	Status
Rev 12	Changes (Pg. 1-11) 12.1 Change document layout from White Electronic Designs to Microsemi 12.2 Add document Revision History page	March 2011	Final
Rev 13	Changes (Pg. 2) 13.1 Correct typo in Absolute Maximum Ratings – Signal Voltage Range to Ground Max from V_{CC}-0.5 to V_{CC}+0.5 13.1 Correct typo in DC Characteristics – CMOS Compatible - Operating Supply Current Conditions from CS# = V_{IH} to CS# = V_{IL}	April 2012	Final
Rev 14	Change (Pg. 9) 14.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final

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