54F/74F620 • 54F/74F623

Inverting Octal Bus Transceiver With 3-State Outputs

Description

The 'F623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The outputs are capable of sinking 64 mA and sourcing up to 15 mA, providing very good capacitive drive characteristics. The 'F620 is an inverting version of the 'F623.

These octal bus transceivers are designed for asynchronous two-way data flow between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

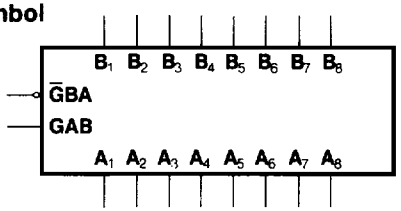
The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (sixteen in all) will remain at their last states.

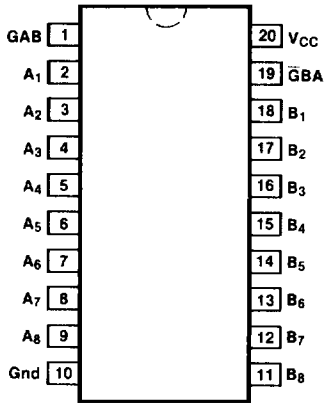
- **Octal Bidirectional Bus Interface**
- **3-State Buffer Outputs Sink 64 mA**
- **15 mA Source Current**
- **'F620 Inverting Option of 'F623**

Ordering Code: See Section 5

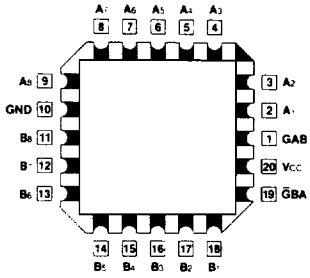
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

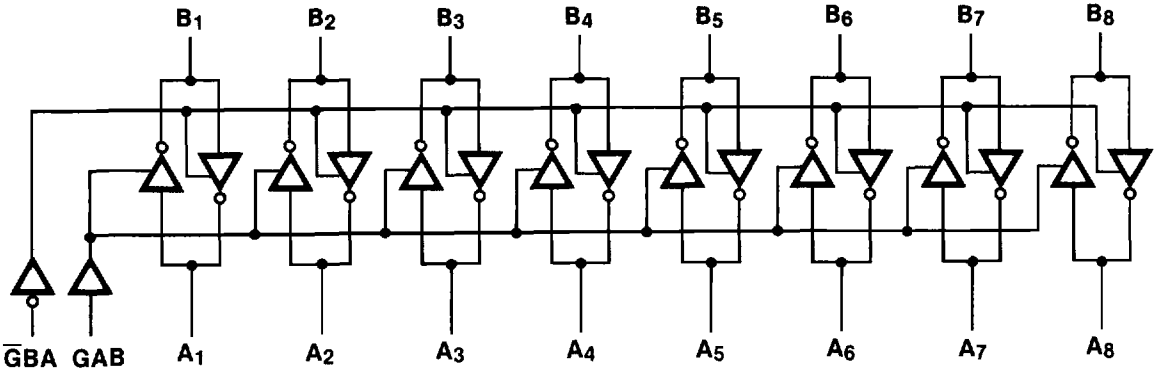
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{G}$BA,GAB	Enable Inputs	0.5/0.375
A_1-A_8	A Inputs or	1.75/0.406
	3-State Outputs	75/15 (12.5)
B_1-B_8	B Inputs or	1.75/0.406
	3-State Outputs	75/40(30)

Function Table

Enable Inputs		Operation	
$\overline{G}BA$	GAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus, A data to B bus	B data to A bus, $\overline{A}$ data to B bus

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			143	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output ('F620)		8.0 9.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output ('F620)		8.0 9.0						ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output ('F623)		6.5 7.0						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output ('F623)		6.5 7.0						ns	3-1 3-4
t_{PZH} t_{PZL}	Enable Time $\overline{G}$BA Input to A Output		8.0 11.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time $\overline{G}$BA Input to A Output		7.5 6.0							
t_{PZH} t_{PZL}	Enable Time GAB Input to B Output		8.0 11.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Disable Time GAB Input to B Output		7.5 6.0							