

DESCRIPTION

The Hyundai HY5DU56822 is a 268,435,456-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY5DU56822 is organized as 4 banks of 8,388,608x8.

HY5DU56822 offers fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the clock(falling edges of the $\overline{\text{CLK}}$), Data(DQ), Data strobes(DQS) and Write data masks(DM) inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

Mode register set options include the length of pipeline ($\overline{\text{CAS}}$ latency of 2 / 2.5 / 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 2 / 4 / 8), the burst count sequence(sequential or interleave), DQ FET Control (/QFC) and Output Driver types (Full / Half Strength Driver). Because data rate is doubled through reading and writing at both rising and falling edges of the clock, 2X higher data bandwidth can be achieved than that of traditional (single data rate) Synchronous DRAM.

FEATURES

- 2.5V VDD and VDDQ power supply
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Fully differential clock operations(CLK & $\overline{\text{CLK}}$) with 125MHz/133MHz/143MHz
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Data(DQ) and Write masks(DM) latched on both rising and falling edges of the Data Strobe
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Delay Locked Loop(DLL) installed with DLL reset mode
- Write mask byte controlled by DM
- Programmable $\overline{\text{CAS}}$ Latency 2 / 2.5 / 3 supported
- Write Operations with 1 Clock Write Latency
- /QFC & Half Strength Driver controlled by EMRS
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal four banks operation with single pulsed $\overline{\text{RAS}}$
- Auto refresh and self refresh supported
- 8192 refresh cycles / 64ms

ORDERING INFORMATION

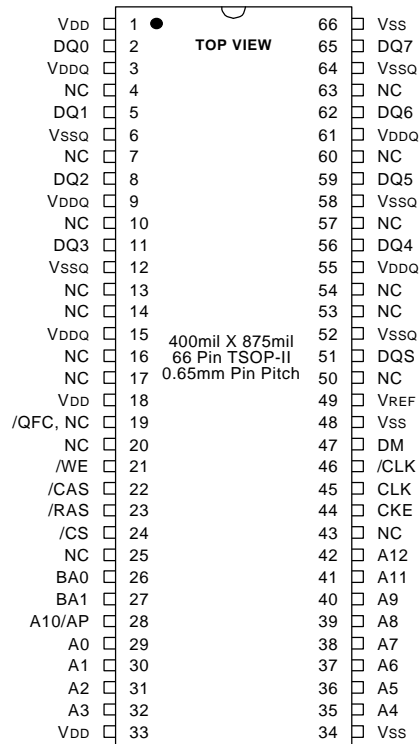
Part No.	Power Supply	Clock Frequency	Organization	Interface	Package
HY5DU56822(L)T-K	VDD=2.5V VDDQ=2.5V	143MHz (*PC266A)	4Banks x 8Mbit x 8	SSTL_2	400mil 66pin TSOP II
HY5DU56822(L)T-H		133MHz (*PC266B)			
HY5DU56822(L)T-L		125MHz (*PC200)			

* JEDEC Standard compliant

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Rev. 0.1/Mar.00

PIN CONFIGURATION

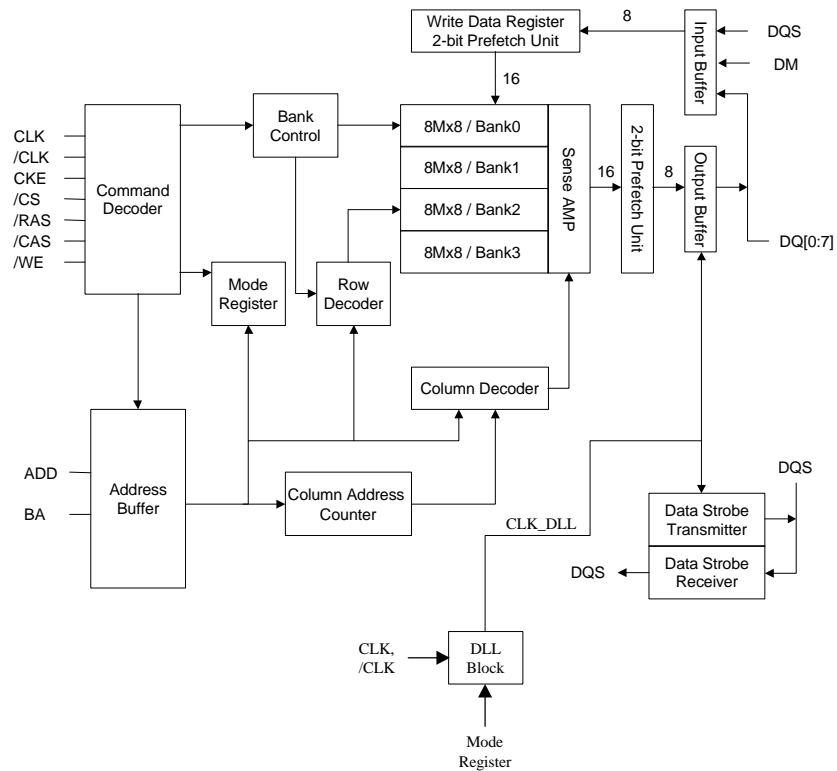


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK, $\overline{\text{CLK}}$	Differential Clock Input	The system clock input. All of the inputs are latched on the rising edges of the clock except DQ, DQS and DM that are sampled on the both.
CKE	Clock Enable	Controls internal clock signal. When deactivated, the DDR SDRAM will be one of the states among power down or self refresh.
$\overline{\text{CS}}$	Chip Select	Enables or disables all inputs except CLK/ $\overline{\text{CLK}}$, CKE, DQS and DM.
BA0, BA1	Bank Select Address	Selects bank to be activated during either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ activity. Selects bank to be read/written during either RAS or CAS activity.
A0 ~ A12	Address	Row Address : A0 ~ A12, Column Address : A0 ~ A9, AP Flag : A10
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operations. Refer function truth table for details.
DM	Write Mask	Masks input data in write mode.
DQS	Data Input/Output Strobe	Active on the both edges for Data Input and Output.
DQ0 ~ DQ7	Data Input/Output	Multiplexed Data input / output pin.
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers for Noise immunity.
VREF	Reference Voltage	Reference voltage for inputs for SSTL interface.
/QFC (optional)	DQ FET Switch Control	Controls FET Switches on DQs used for reduction of impedance.
NC	No Connection	No connection.

FUNCTIONAL BLOCK DIAGRAM

4banks x 8Mbit x 8 I/O Double data rate Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.3	2.5	2.7	V	
Power Supply Voltage	VDDQ	2.3	2.5	2.7	V	1
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	1.15	1.25	1.35	V	3

Note :

- VDDQ must not exceed the level of VDD.
- VIL (min) is acceptable -1.5V AC pulse width with ≤ 5 ns of duration.
- The value of VREF is approximately equal to 0.5VDDQ.

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31	-	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)	-	VREF - 0.31	V	
Input Differential Voltage, CLK and /CLK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CLK and /CLK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :

- VID is the magnitude of the difference between the input level on CLK and the input on CLK.
- The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

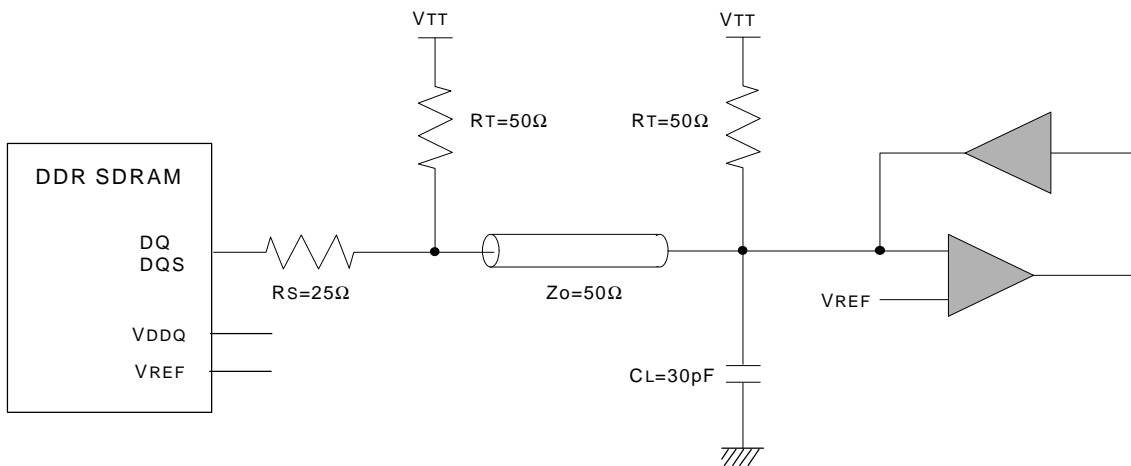
CAPACITANCE (TA=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A12, BA0 ~ BA1, $\overline{\text{CKE}}$, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	CIN	2.0	3.0	pF
Clock Capacitance	CLK, $\overline{\text{CLK}}$	CCLK	2.0	3.0	pF
Data Input / Output Capacitance	DQ0 ~ DQ7, DQS, DM	CIO	4.0	5.0	pF

Note :

1. VDD, VDDQ = 2.3V to 2.7V, VODC = VDDQ/2, VOpeak-to-peak = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-5	5	uA	1
Output Leakage Current	ILO	-5	5	uA	2
Output High Voltage	VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage	VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note :

- VIN = 0 to 2.7V, All other pins are not tested under VIN =0V
- DOUT is disabled, VOUT=0 to 2.7V

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Test Condition	Speed			Unit	Note	
			-K	-H	-L			
Operating Current	IDD1	Burst length=2, One bank active tRC ≥ tRC(min), IOL=0mA	TBD	TBD	TBD	mA	1	
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = min	TBD			mA		
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), \overline{CS} ≥ VIH(min), tCK = min Input signals are changed one time during 2clks	TBD			mA		
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = min	TBD			mA		
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), \overline{CS} ≥ VIH(min), tCK = min Input signals are changed one time during 2clks	TBD			mA		
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=2.5	TBD	TBD	TBD	mA	1
			CL=2	TBD	TBD	TBD		
			CL=2	TBD	TBD	TBD		
Auto Refresh Current	IDD5	tRC ≥ tRFC(min), All banks active	TBD			mA	2	
Self Refresh Current	IDD6	CKE ≤ 0.2V	TBD			mA	3	
			TBD			mA	4	

Note :

- IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.
- Min. of tRFC (Auto Refresh Row Cycle Time) is shown at AC CHARACTERISTICS.
- HY5DU56822
- HY5DU56822(L), Self Refresh low power

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter	Symbol	-K(PC266A)		-H(PC266B)		-L(PC200)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row Cycle Time	tRC	65	-	65	-	70	-	ns		
Auto Refresh Row Cycle Time	tRFC	75	-	75	-	80	-	ns		
Row Active Time	tRAS	45	120K	48	120K	50	120K	ns		
Row Address to Column Address Delay	tRCD	20	-	20	-	20	-	ns		
Row Active to Row Active Delay	tRRD	15	-	15	-	15	-	ns		
Column Address to Column Address Delay	tCCD	1	-	1	-	1	-	CLK		
Row Precharge Time	tRP	20	-	20	-	20	-	ns		
Write Recovery Time	tWR	15	-	15	-	15	-	ns		
Last Data-In to Read Command	tDRL	1	-	1	-	1	-	CLK		
Auto Precharge Write Recovery + Precharge Time	tDAL	35	-	35	-	35	-	ns		
System Clock Cycle Time	tCK	CAS Latency = 3	7	15	7.5	15	8	15	ns	
		CAS Latency = 2.5	7	15	7.5	15	8	15	ns	
		CAS Latency = 2	7.5	15	10	15	10	15	ns	
Clock High Level Width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	CLK		
Clock Low Level Width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	CLK		
Data-Out edge to Clock edge Skew	tAC	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns		
DQS-Out edge to Clock edge Skew	tDQSCK	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns		
DQS-Out edge to Data-Out edge Skew	tDQSQA	-0.5	0.5	-0.5	0.5	-0.6	0.6	ns		
Data-Out hold time from DQS	tQH	tHPmin -0.75ns	-	tHPmin -0.75ns	-	tHPmin -0.75ns	-	ns	1	
Clock Half Period	tHP	tCH/L min	-	tCH/L min	-	tCH/L min	-	ns	1	
Input Setup Time (fast slew rate)	tIS	0.9	-	0.9	-	1.0	-	ns	2,3,5,6	
Input Hold Time (fast slew rate)	tIH	0.9	-	0.9	-	1.0	-	ns	2,3,5,6	
Input Setup Time (slow slew rate)	tIS	1.1	-	1.1	-	1.1	-	ns	2,4,5,6	
Input Hold Time (slow slew rate)	tIH	1.1	-	1.1	-	1.1	-	ns	2,4,5,6	
Input Pulse Width	tIPW	2.2	-	2.2	-	-	-	ns	6	
Write DQS High Level Width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	CLK		
Write DQS Low Level Width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	CLK		
CLK to First Rising edge of DQS-In	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	CLK		
Data-In Setup Time to DQS-In (DQ & DM)	tDS	0.5	-	0.5	-	0.6	-	ns	7	
Data-in Hold Time to DQS-In (DQ & DM)	tDH	0.5	-	0.5	-	0.6	-	ns	7	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

- continued -

Parameter	Symbol	-K(PC266A)		-H(PC266B)		-L(PC200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQ & DM Input Pulse Width	tDIPW	1.75	-	1.75	-	2	-	ns	
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	CLK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	0	-	CLK	
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	0.25	-	CLK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	CLK	
Mode Register Set Delay	tMRD	2	-	2	-	2	-	CLK	
Power Down Exit Time	tPDEX	10	-	10	-	10	-	ns	
Exit Self Refresh to Command	tXSC	200	-	200	-	200	-	CLK	8
Average Periodic Refresh Interval	tREFI	-	7.8	-	7.8	-	7.8	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A12, BA0~BA1, CKE, \overline{CS} , \overline{RAS} , CAS, \overline{WE} .
3. For command/address input slew rate $\geq 1.0V/ns$
4. For command/address input slew rate $\geq 0.5V/ns$ and $< 1.0V/ns$
5. CK, /CK slew rates are $\geq 1.0V/ns$
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strokes(DQS) : DQ, DM
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL operation

WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	\overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE}	DM	ADDR	A10/AP	BA	Note
Data Write	H	X	X	L		X		1,
Data-In Mask	H	X	X	H		X		1,

Note :

1. Write Mask command masks burst write data with reference to DQS(Data Strokes) and it is not related with read data.

SIMPLIFIED COMMAND TRUTH TABLE

Command	CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	ADDR	A10/ AP	BA	Note
Extended Mode Register Set	H	X	L	L	L	L	OP code		1,2	
Mode Register Set	H	X	L	L	L	L	OP code		1,2	
Device Deselect	H	X	H	X	X	X	X		1	
No Operation			L	H	H	H				
Bank Active	H	X	L	L	H	H	RA	V	1	
Read	H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge								H		1,3
Write	H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge								H		1,4
Precharge All Banks	H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank								L	V	1
Read Burst Stop	H	X	L	H	H	L	X		1	
Auto Refresh	H	H	L	L	L	H	X		1	
Self Refresh	Entry	H	L	L	L	L	H	X		1
	Exit	L	H	H	X	X	X			1
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	H	H	H			1
	Exit	L	H	H	X	X	X			1
				L	H	H	H			1
Active Power Down Mode	Entry	H	L	H	X	X	X	X		1
				L	V	V	V			1
	Exit	L	H	X			1			

(H=Logic High Level, L=Logic Low Level, X=Dont Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

- DM states are "Dont Care". Refer to below Write Mask Truth Table.
- OP Code(Operand Code) consists of A0~A12 and BA0~BA1 used for Mode Registering during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
- If a Read with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+tRP).
- If a Write with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+tDPL+tRP). Last Data-In to Precharge delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
- If A10/AP is "High" when Row Precharge command being issued, BA 0/BA1 are ignored and all banks are selected to be precharged.

PACKAGE INFORMATION

400mil 66pin Thin Small Outline Package

