

54AC/74AC841 • 54ACT/74ACT841 54AC/74AC842 • 54ACT/74ACT842

10-Bit Transparent Latch

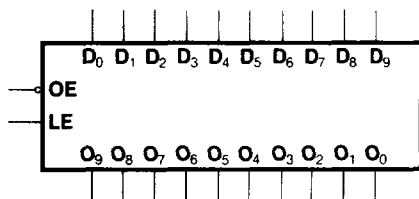
Description

The 'AC'/ACT841 and 'AC'/ACT842 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'AC'/ACT841 is a 10-bit transparent latch, a 10-bit version of the 'AC'/ACT373.

- 'ACT841 and 'ACT842 have TTL-Compatible Inputs

Ordering Code: See Section 6

Logic Symbol ('AC'/ACT841)*

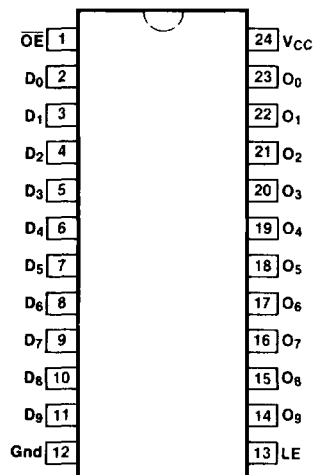


*The 'AC'/ACT842 has inverting outputs.

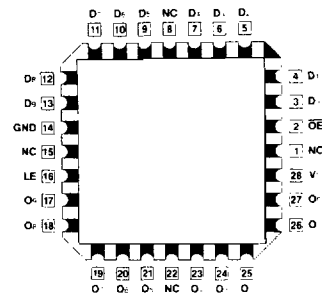
Pin Names

- | | |
|---|----------------------------|
| D ₀ - D ₉ | Data Inputs |
| O ₀ - O ₉ | Data Outputs ('AC'/ACT841) |
| \bar{O} ₀ - \bar{O} ₉ | Data Outputs ('AC'/ACT842) |
| $\bar{O}E$ | Output Enable |
| LE | Latch Enable |

Connection Diagrams



**Pin Assignment
for DIP, Flatpak and SOIC**



**Pin Assignment
for LCC**

AC841 • ACT841 • AC842 • ACT842

Functional Description

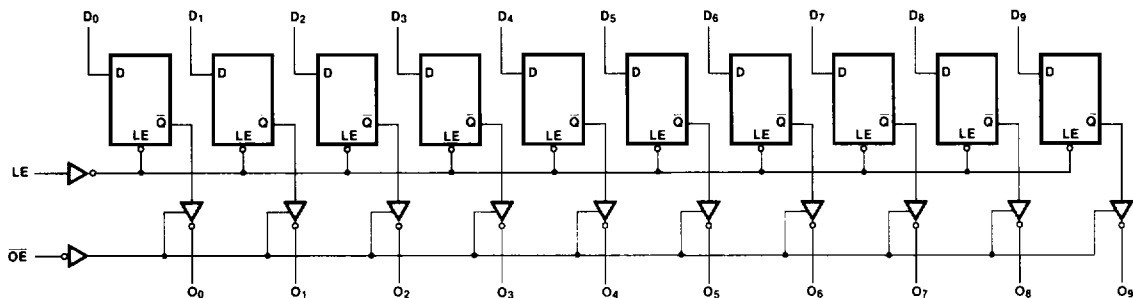
The 'AC/ACT841 and 'AC/ACT842 consist of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output		Function
\overline{OE}	LE	D	Q	O ('841)	\overline{O} ('842)	
X	X	X	X	Z	Z	High Z
H	H	L	L	Z	Z	High Z
H	H	H	H	Z	Z	High Z
H	L	X	NC	Z	Z	Latched
L	H	L	L	L	H	Transparent
L	H	H	H	H	L	Transparent
L	L	X	NC	NC	NC	Latched

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 NC = No Change

Logic Diagram ('AC/ACT841)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/ACT842 has the same logic diagram with inverting outputs.

AC841 • ACT841 • AC842 • ACT842

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input (*ACT841/842)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0	17.0 12.0							ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0	16.5 11.0							ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0	18.5 13.0							ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0	17.0 12.0							ns	3-6
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0	14.5 10.0							ns	3-7
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0	11.5 8.0							ns	3-8
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0	13.0 9.0							ns	3-7
t _{PLZ}	Output Disable Time OE to O _n	3.3 5.0	13.0 9.0							ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC841 • ACT841 • AC842 • AC842

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Setup Time, HIGH or LOW Dn to LE	3.3 5.0	4.0 2.5						ns	3-9
th	Hold Time, HIGH or LOW Dn to LE	3.3 5.0	0 0						ns	3-9
tw	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay Dn to Qn	5.0	12.0						ns	3-5	
tPHL	Propagation Delay Dn to Qn	5.0	11.0						ns	3-5	
tPLH	Propagation Delay LE to On	5.0	13.0						ns	3-6	
tPHL	Propagation Delay LE to On	5.0	12.0						ns	3-6	
tPZH	Output Enable Time OE to On	5.0	10.0						ns	3-7	
tPZL	Output Enable Time OE to On	5.0	8.0						ns	3-8	
tPHZ	Output Disable Time OE to On	5.0	9.0						ns	3-7	
tPLZ	Output Disable Time OE to On	5.0	9.0						ns	3-8	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT	54ACT	74ACT	Units	Fig. No.
			TA = +25°C CL = 50 pF	TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum			
ts	Setup Time, HIGH or LOW Dn to LE	5.0	2.5			ns	3-9
th	Hold Time, HIGH or LOW Dn to LE	5.0	0			ns	3-9
tw	LE Pulse Width, HIGH	5.0	2.5			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance		pF	Vcc = 5.5 V