No.2360

# LC3516A,AM,AS/LC3516AL,AML,ASL

Asynchronous Silicon Gate CMOS LSI

## 2048 Words x 8 Bits CMOS Static RAMs

### General Description

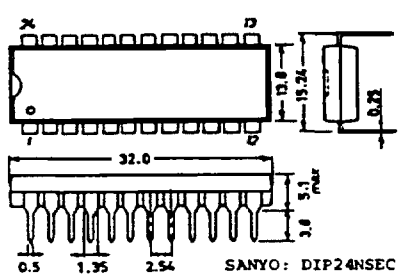
The LC3516A series are fully asynchronous silicon gate CMOS static RAMs organized as 2048 words x 8 bits.
The LC3516A series have two chip enable inputs: $\overline{CE1}$ for high-speed memory access and $\overline{CE2}$ for low standby current mode being valid at the time of battery backup.
The LC3516A series have a full CMOS circuit configuration. Since the current dissipation is low at the data retention mode or standby mode, they are especially suited for use in memory systems, battery-powered portable systems whose power dissipation must be minimized.
The LC3516AL/AML/ASL guarantee a maximum standby current of 1uA at 60°C.

### Features

- Address access time ($t_{AA}$)
  - 100ns(max): LC3516A-10/AL-10/AM-10/AML-10/AS-10/ASL-10
  - 120ns(max): LC3516A-12/AL-12/AM-12/AML-12/AS-12/ASL-12
  - 150ns(max): LC3516A-15/AL-15/AM-15/AML-15/AS-15/ASL-15
- Low standby current
  - 0.2uA(max) / Ta=25°C } LC3516AL-10/12/15,LC3516AML-10/12/15,
  - 1.0uA(max) / Ta=60°C } LC3516ASL-10/12/15
  - 5.0uA(max) / Ta=60°C } LC3516A-10/12/15,LC3516AM-10/12/15,
  - 30uA(max) / Ta=85°C } LC3516AS-10/12/15
- Single 5V supply: 5V±10%
- Data retention supply voltage: 2.0 to 5.5V
- No clock required (Fully static memory)
- Directly TTL compatible: All inputs and outputs
- Common data input and output using 3-state outputs
- Package
  - Dual-in-line plastic package :LC3516A,AL
  - Miniflat package :LC3516AM,AML
  - Dual-in-line slim plastic pakage:LC3516AS,ASL

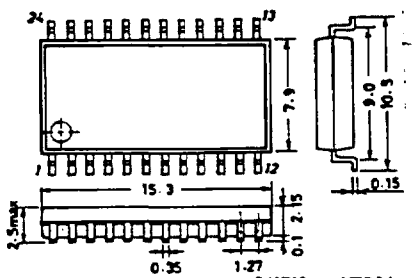


LC3516A,AL
[DIP24(600mil)]
**Case Outline** 3072-D24NSEC
(unit:mm)



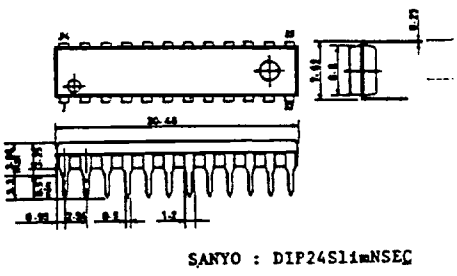
SANYO: DIP24NSEC

LC3516AM,AML
[MFP24(375mil)]
**Case Outline** 3045B-M24IC
(unit:mm)



SANYO : MFP24

LC3516AS,ASL
[DIP24Slim(300mil)]
**Case Outline** 3092-D24NSEC
(unit:mm)

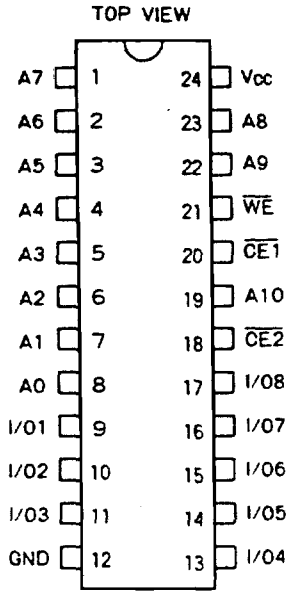

SANYO : DIP24SlimNSEC



These specifications are subject to change without notice.

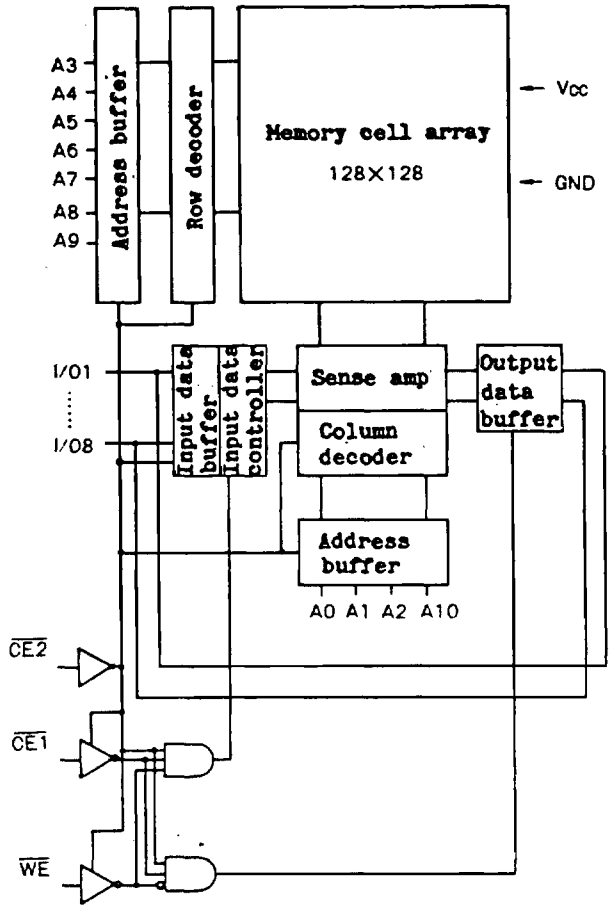
SANYO ELECTRIC CO.,LTD. SEMICONDUCTOR DIVISION
15-13, 6-CHOME, SOTOKANDA, CHIYODA-KU, TOKYO 101 JAPAN

**Pin Assignment**




| | |
|---|---|
| A0 to A10 | Address input |
| $\overline{WE}$ | Read/write control input |
| $\overline{CE1}$ | Chip enable input |
| $\overline{CE2}$ | Chip enable input |
| I/01 to I/08 | Data input/output |
| $V_{CC}$/GND | Power supply pin |

**Block Diagram**




**Function Table**

| Mode | $\overline{CE2}$ | $\overline{CE1}$ | $\overline{WE}$ | I/O | Supply Current |
|---|---|---|---|---|---|
| Read Cycle | L | L | H | Data output | $I_{CCA}$ |
| Write Cycle | L | L | L | Data input | $I_{CCA}$ |
| Nonselect | L | H | X | High impedance | $I_{CCA}$ |
| Nonselect | H | X | X | High impedance | $I_{CCS}$ |

X:H or L

**Absolute Maximum Ratings**

| Parameter | Symbol | Condition | Limits | unit |
|---|---|---|---|---|
| Maximum Supply Voltage | $V_{CC}max$ | | +7.0 | V |
| Input Pin Voltage | $V_{IN}$ | | -0.3 to $V_{CC}$+0.3 | V |
| I/O Pin Voltage | $V_{I/O}$ | | -0.3 to $V_{CC}$+0.3 | V |
| Operating Temperature | Topg | | -30 to +85 | °C |
| Storage Temperature | Tstg | | -55 to +125 | °C |

**DC Allowable Operating Conditions** at Ta=-30 to +85°C

| Parameter | Symbol | min | typ | max | unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input "H"-Level Voltage | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 | V |
| Input "L"-Level Voltage | $V_{IL}$ | -0.3 | | 0.8 | V |

**DC Electrical Characteristics** at Ta=-30 to +85°C, $V_{CC}$=5V±10%

| Parameter | Symbol | Conditions | | | min | typ* | max | unit |
|---|---|---|---|---|---|---|---|---|
| Input Leak Current | $I_{LI}$ | $V_{IN}$=0 to $V_{CC}$ | | | -1.0 | | 1.0 | uA |
| I/O Leak Current | $I_{LO}$ | $V_{\overline{CE1}}$ or $V_{CE2}$=$V_{IH}$, $V_{I/O}$=0 to $V_{CC}$ | | | -5.0 | | 5.0 | uA |
| Supply Current(DC) | $I_{CCA1}$ | $V_{\overline{CE2}}$=0V, $V_{IN}$=$V_{CC}$/GND, I/O=0mA | | | | 30 | 55 | mA |
| | $I_{CCA2}$ | $V_{\overline{CE2}}$=$V_{IL}$, $V_{IN}$=$V_{IH}$/$V_{IL}$, I/O=0mA | | | | 40 | 70 | mA |
| Average Supply Current | $I_{CCA3}$ | cycle=min, duty=100%, I/O=0mA | | | | 50 | 80 | mA |
| Standby Supply Current | $I_{CCS1}$ | $V_{\overline{CE2}}$=$V_{CC}$-0.2V, $V_{IN}$=0 to $V_{CC}$ | LC3516A/AM/AS | Ta=60°C | | | 5.0 | uA |
| | | | | Ta=85°C | | | 30 | uA |
| | | | LC3516AL/AML/AMS | Ta=25°C | | | 0.2 | uA |
| | | | | Ta=60°C | | | 1.0 | uA |
| | $I_{CCS2}$ | $V_{\overline{CE2}}$=$V_{IH}$, $V_{IN}$=0 to $V_{CC}$ | | | | 1.0 | 3.0 | mA |
| Output "H"-Level Voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | | | 2.4 | | | V |
| Output "L"-Level Voltage | $V_{OL}$ | $I_{OL}$=2.0mA | | | | | 0.4 | V |

* Reference value at $V_{CC}$=5.0V, Ta=+25°C

**Input/Output Capacitance** at Ta=+25°C, f=1kMHz

| Parameter | Symbol | Condition | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Input/Output Capacitance | $C_{I/O}$ | $V_{I/O}$=0V | | | 10 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | | | 5 | pF |

**AC Electrical Characteristics** Ta=-30 to +85°C, $V_{CC}$=5V±10%

AC Test Conditions

Input pulse voltage level: 0.6V, 2.4V

Input rise/fall time: 5ns

Input/output timing level: Input "H" level $V_{IH}$=2.2V, Output "H" level $V_{OH}$=2.2V
Input "L" level $V_{IL}$=0.8V, Output "L" level $V_{OL}$=0.8V

Output load: 1TTL gate + $C_L$=100pF

Read Cycle

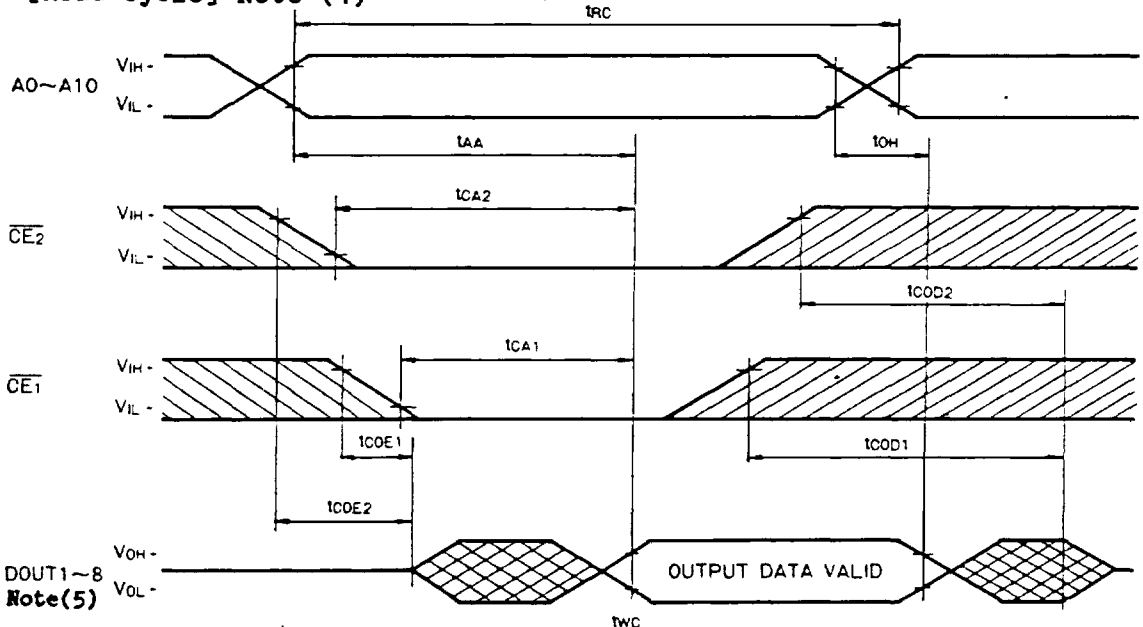
| Parameter | Symbol | LC3516A/AM/AS-10 LC3516AL/AML/ASL-10 | | LC3516A/AM/AS-12 LC3516AL/AML/ASL-12 | | LC3516A/AM/AS-15 LC3516AL/AML/ASL-15 | | unit |
|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | |
| Read Cycle Time | $t_{RC}$ | 100 | | 120 | | 150 | | ns |
| Address Access Time | $t_{AA}$ | | 100 | | 120 | | 150 | ns |
| $\overline{CE1}$ Access Time | $t_{CA1}$ | | 60 | | 70 | | 80 | ns |
| $\overline{CE2}$ Access Time | $t_{CA2}$ | | 100 | | 120 | | 150 | ns |
| Output Hold Time | $t_{OH}$ | 5 | | 5 | | 5 | | ns |
| $\overline{CE1}$-Output Enable Time | $t_{COE1}$ | 5 | | 5 | | 5 | | ns |
| $\overline{CE2}$-Output Enable Time | $t_{COE2}$ | 5 | | 5 | | 10 | | ns |
| $\overline{CE1}$-Output Disable Time | $t_{COD1}$ | | 35 | | 40 | | 50 | ns |
| $\overline{CE2}$-Output Disable Time | $t_{COD2}$ | | 35 | | 40 | | 50 | ns |

## Write Cycle

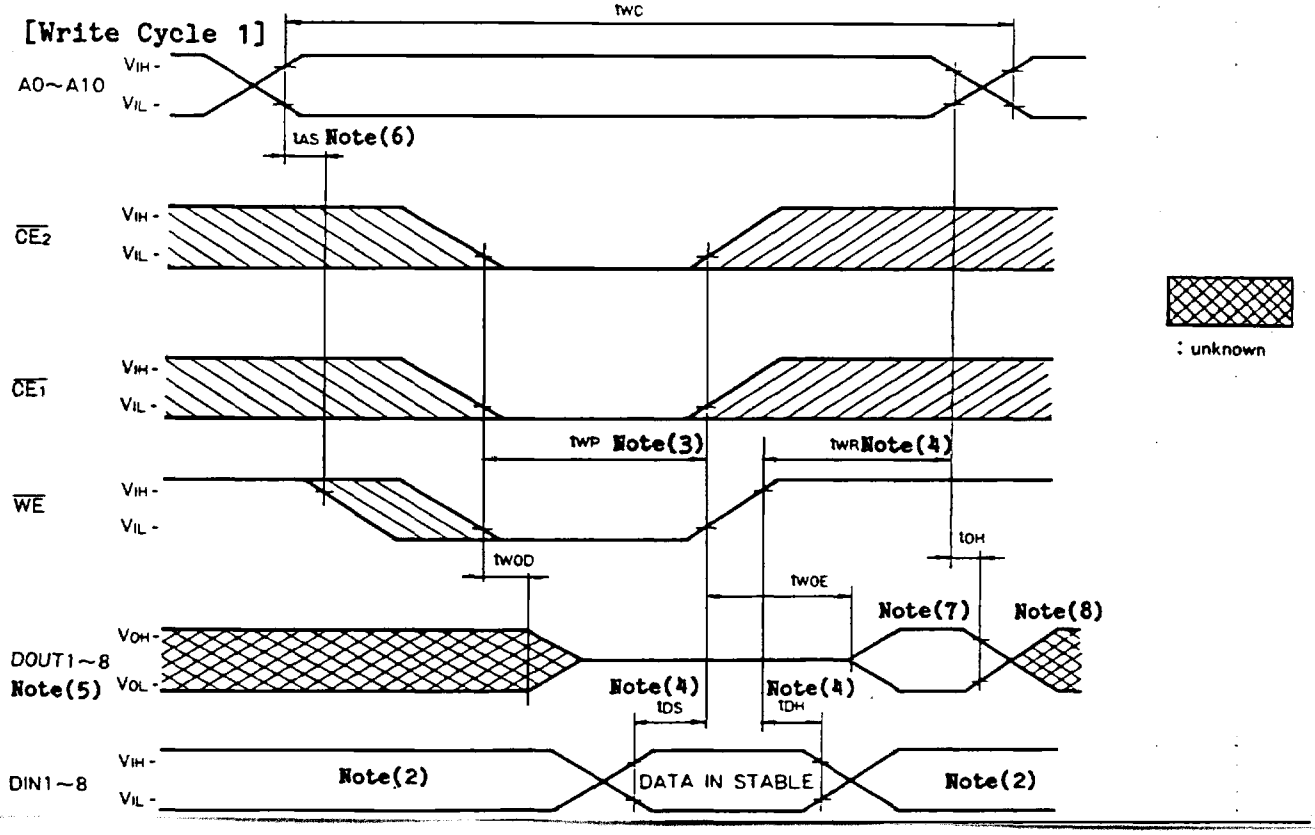
| Parameter | Symbol | LC3516A/AM/AS-10 LC3516AL/AML/ASL-10 min | max | LC3516A/AM/AS-12 LC3516AL/AML/ASL-12 min | max | LC3516A/AM/AS-15 LC3516AL/AML/ASL-15 min | max | unit |
|---|---|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 100 | | 120 | | 150 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | ns |
| Write Pulse Width | $t_{WP}$ | 75 | | 95 | | 120 | | ns |
| Write Recovery Time | $t_{WR}$ | 10 | | 10 | | 10 | | ns |
| Data Setup Time | $t_{DS}$ | 50 | | 60 | | 70 | | ns |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | ns |
| $\overline{WE}$-Output Enable Time | $t_{WOE}$ | 5 | | 5 | | 5 | | ns |
| $\overline{WE}$-Output Disable Time | $t_{WOD}$ | | 35 | | 40 | | 50 | ns |

## Timing Chart

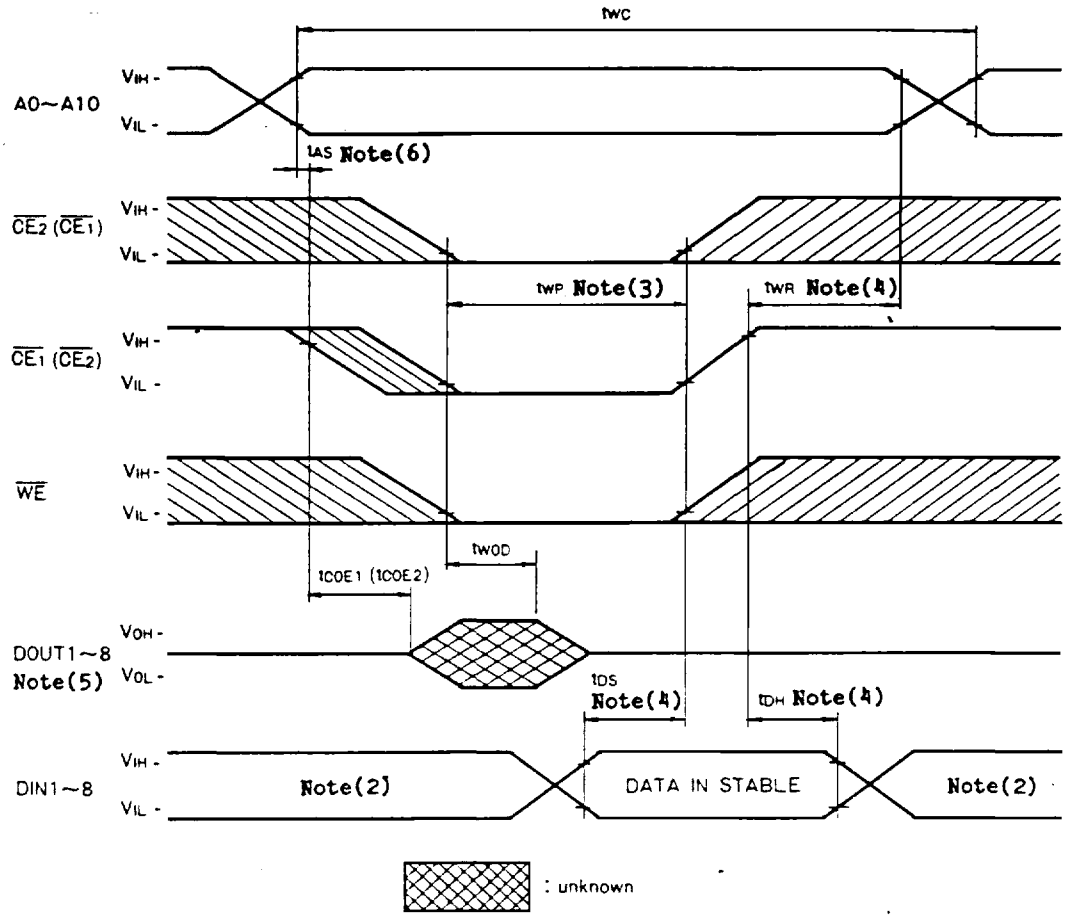
[Read Cycle] Note (1)




[Write Cycle 1]



[Write Cycle 2]

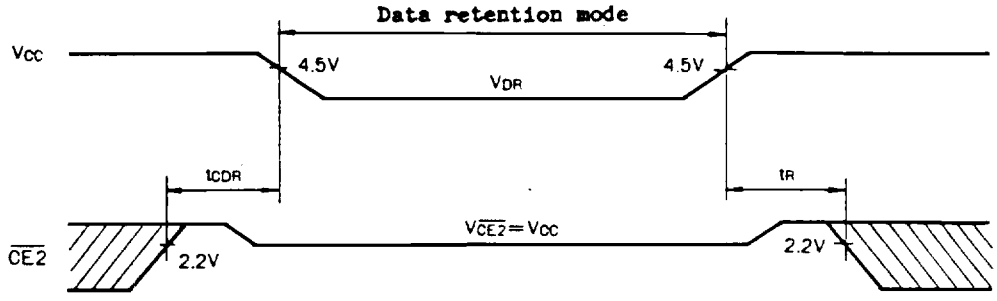



Note) (1) $\overline{WE}$ must be high during read cycle.
(2) When $D_{OUT}$ is in the output state, no opposite polarity signal must be applied externally.
(3) A wrte occurs during the overlap of a low $\overline{CE1}$, $\overline{CE2}$ and a low $\overline{WE}$.
(4) $t_{WR}$, $t_{DS}$, $t_{DH}$ are referenced to the earliest going high of CE1, or $\overline{CE2}$, or $\overline{WE}$.
(5) $D_{OUT}$ is in a high impedance state when $\overline{CE1}$ is high or $\overline{CE2}$ is high or $\overline{WE}$ is low.
(6) $t_{AS}$ is referenced to the point at which all of $\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$ go low.
(7) $D_{OUT}$ has the same polarity as write data of this write cycle.
(8) $D_{OUT}$ is the read-out data of the next address.

**Data Retention Characteristics** Ta=-30 to +85°C

| Parameter | Symbol | Conditions | | | min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|
| Data Retention Supply Voltage | $V_{DR}$ | $V_{\overline{CE2}}=V_{CC}$, $V_{IN}$=0to$V_{CC}$ | | | 2.0 | | 5.5 | V |
| Data Retention Supply Current | $I_{CCDR}$ | $V_{\overline{CE2}}=V_{CC}$ | LC3516A/ | Ta=60°C | | | 4.0 | uA |
| | | $V_{CC}$=3.0V | AM/AS | Ta=85°C | | | 20 | uA |
| | | $V_{IN}$=0to$V_{CC}$ | LC3516AL/ | Ta=25°C | | | 0.2 | uA |
| | | | AML/ASL | Ta=60°C | | | 1.0 | uA |
| $\overline{CE2}$ Setup Time | $t_{CDR}$ | | | | 0 | | | us |
| $\overline{CE2}$ Hold Time | $t_R$ | | | | $t_{RC}$ Note(1) | | | us |

Note) (1) $t_{RC}$=Read cycle time.


Data retention mode
Vcc
4.5V
VDR
4.5V
tCDR
tR
CE2
2.2V
VCE2=Vcc
2.2V