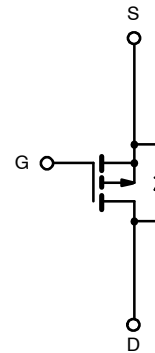
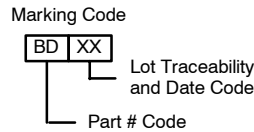
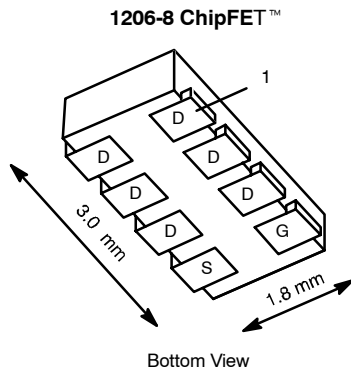




P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-20	0.040 @ V _{GS} = -4.5 V	-6.7
	0.052 @ V _{GS} = -2.5 V	-5.9
	0.072 @ V _{GS} = -1.8 V	-5.0

TrenchFET®
Power MOSFETs
1.8-V Rated



P-Channel MOSFET

Ordering Information: Si5433DC-T1

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	-20		V
Gate-Source Voltage		V _{GS}	±8		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	-6.7	-4.8	A
	T _A = 85°C		-4.8	-3.5	
Pulsed Drain Current		I _{DM}	-20		
Continuous Source Current ^a		I _S	-2.1	-1.1	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.5	1.3	W
	T _A = 85°C		1.3	0.7	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 5 sec	R _{thJA}	40	50	°C/W
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)		R _{thJF}	15	20	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

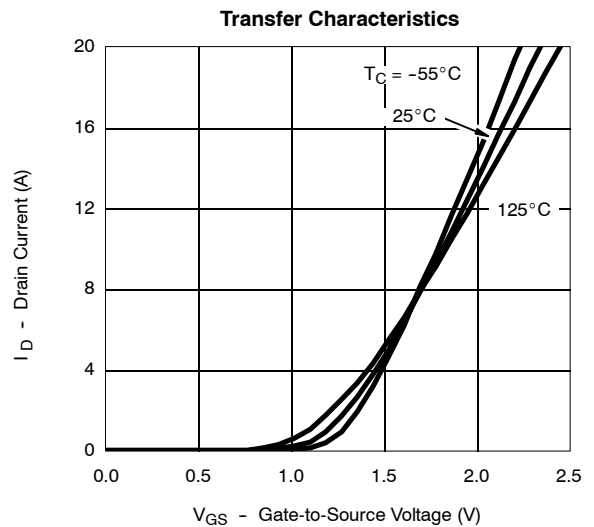
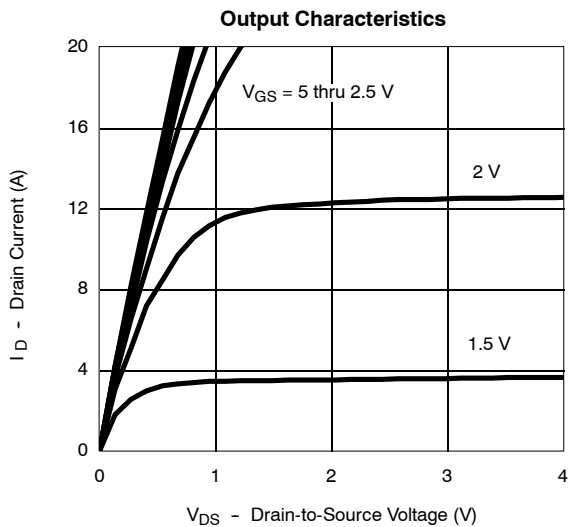


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.45			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -4.8 A		0.036	0.040	Ω
		V _{GS} = -2.5 V, I _D = -4.2 A		0.045	0.052	
		V _{GS} = -1.8 V, I _D = -1 A		0.062	0.072	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -4.8 A		15		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.1 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -4.8 A		15	22	nC
Gate-Source Charge	Q _{gs}			3.6		
Gate-Drain Charge	Q _{gd}			2.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		22	35	ns
Rise Time	t _r			29	45	
Turn-Off Delay Time	t _{d(off)}			94	140	
Fall Time	t _f			54	80	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.1 A, di/dt = 100 A/μs		30	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

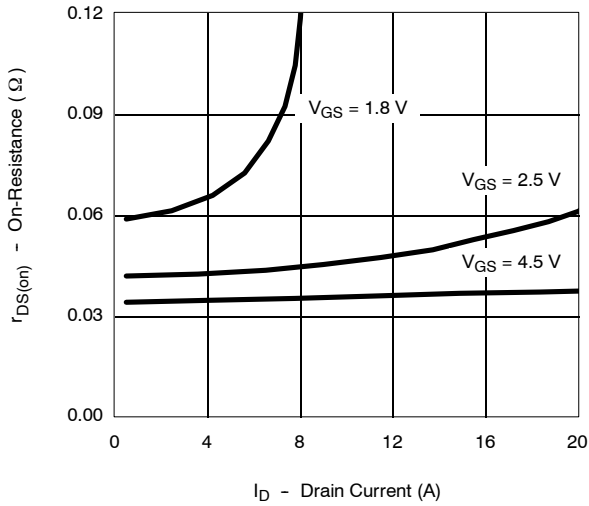
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



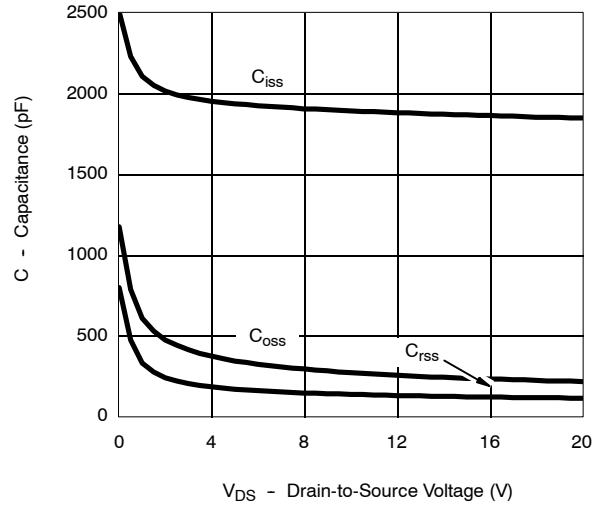


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

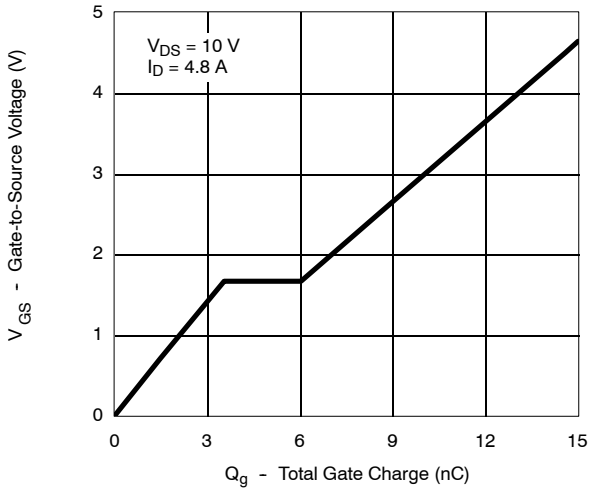
On-Resistance vs. Drain Current



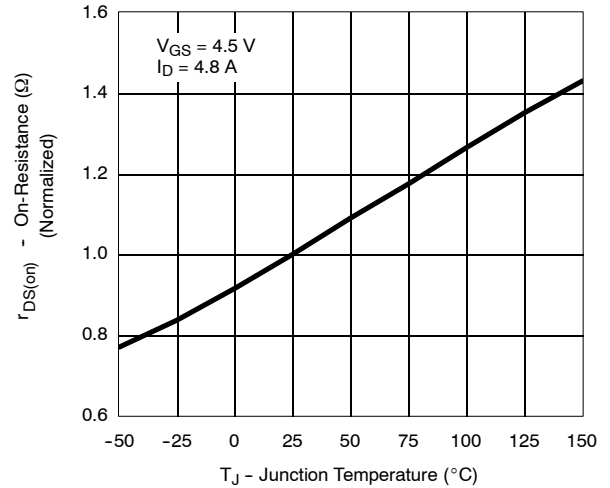
Capacitance



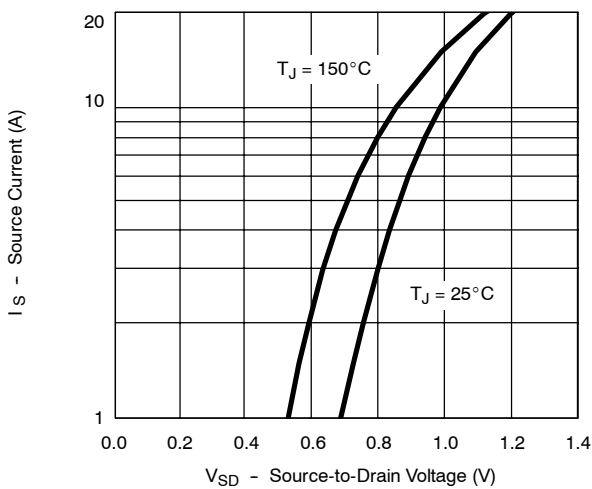
Gate Charge



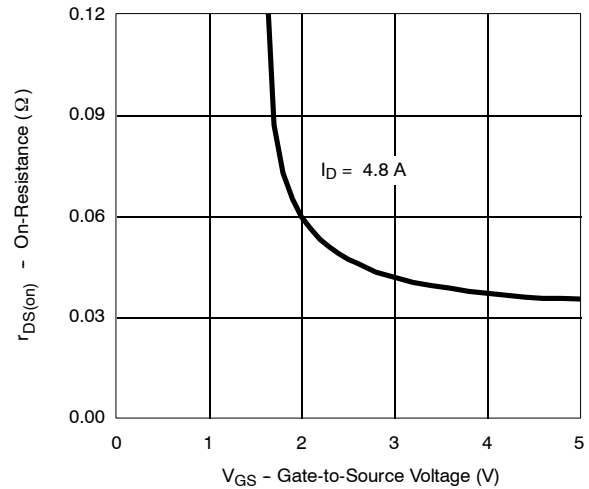
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

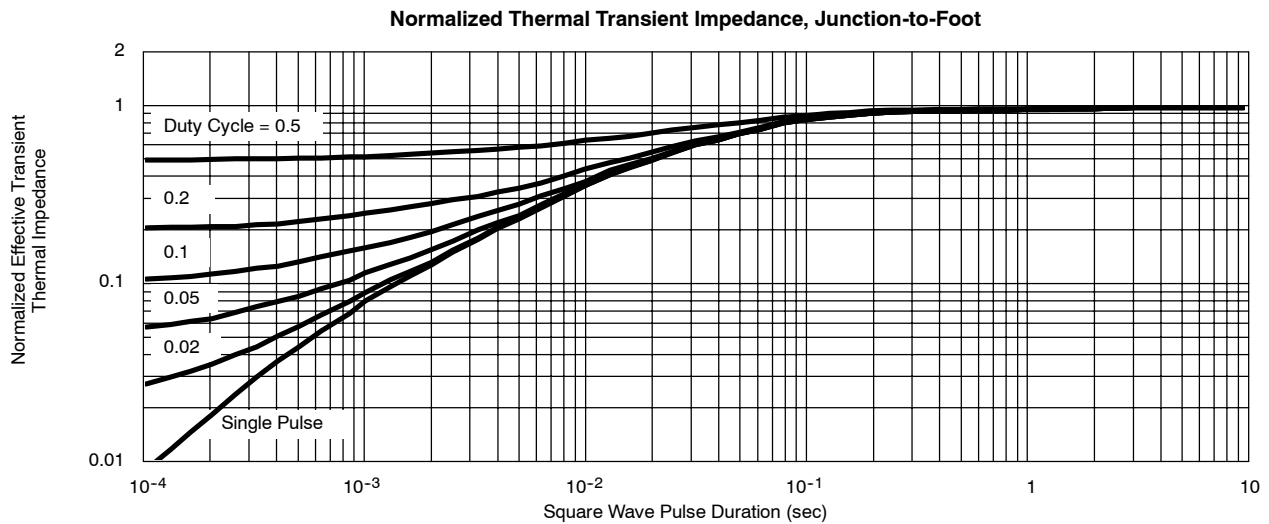
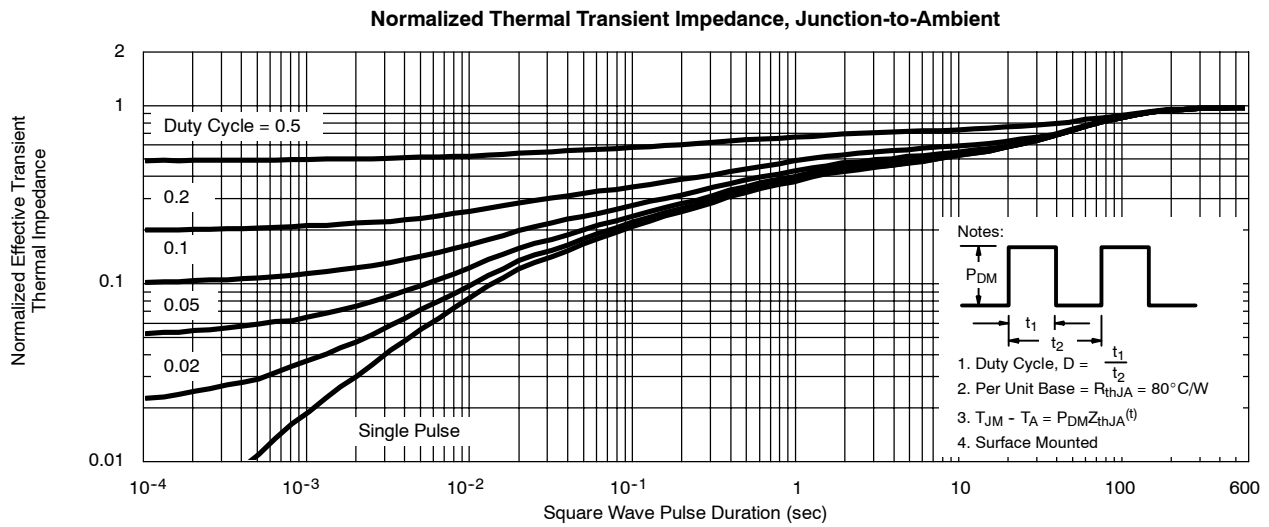
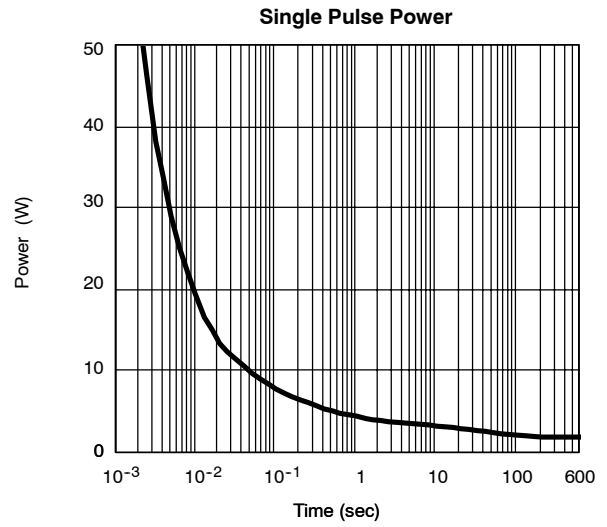
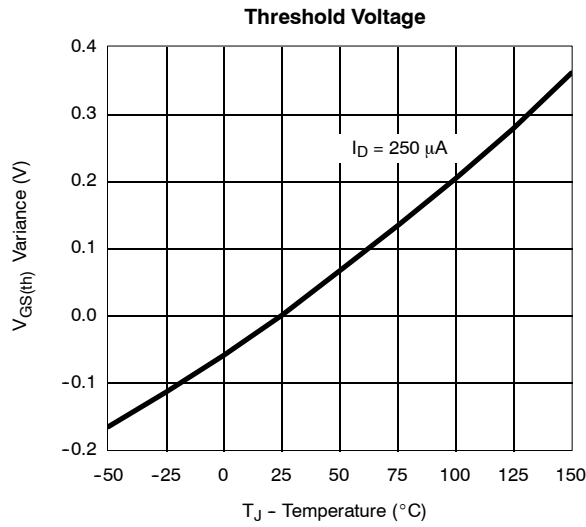


On-Resistance vs. Gate-to-Source Voltage





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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