PRELIMINARY

CY7C1041D

4-Mbit (256K x 16) Static RAM

Features

- **Pin- and function-compatible with CY7C1041B**
- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— I_{CC} = 80 mA @ 10 ns (Commercial)**
  - **— I_{CC} = 90 mA @ 10 ns (Industrial)**
- **Low CMOS standby power**
  - **— I_{SB2} = 10 mA**
- **2.0 V Data Retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Available in Lead-Free 44-Lead (400-Mil) Molded SOJ V44 and 44-Pin TSOP II ZS44 packages**

Functional Description[1]

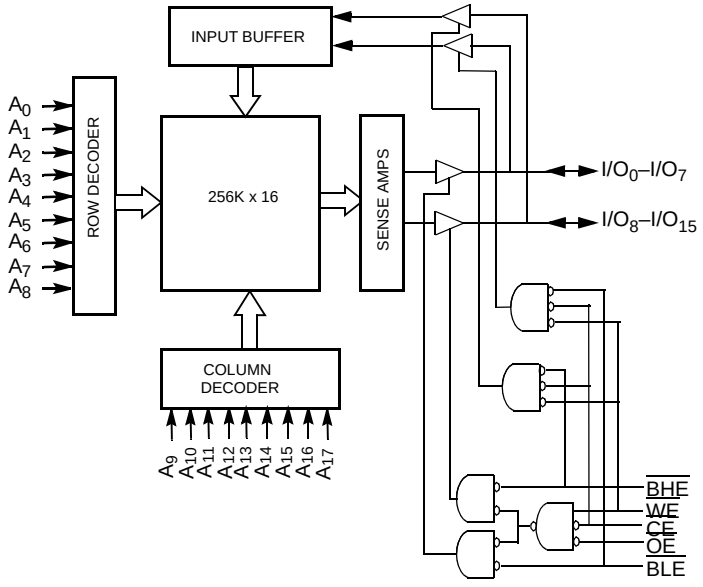
The CY7C1041D is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

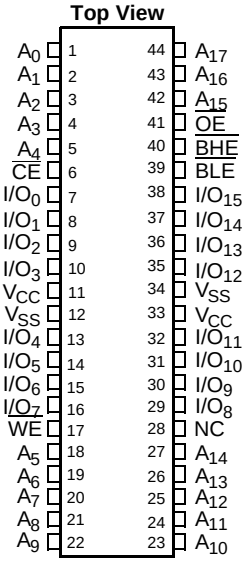
The CY7C1041D is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configuration

SOJ
TSOP II
Top View



Selection Guide

		7C1041D-10	7C1041D-12	7C1041D-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial	80	75	70	mA
	Industrial	90	85	80	
Maximum CMOS Standby Current	Commercial/Industrial	10	10	10	mA

Note:
1. For guidelines on SRAM system design, please refer to the “System Design Guidelines” Cypress application note, available on the internet at www.cypress.com.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) .....20 mA

Static Discharge Voltage..... .....>2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 0.5
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1041D-10 Min.	7C1041D-10 Max.	7C1041D-12 Min.	7C1041D-12 Max.	7C1041D-15 Min.	7C1041D-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[2]			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Com'l		80		75		70	mA
			Ind'l		90		85		80	
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/ Ind'l		20		20		20	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/ Ind'l		10		10		10	mA

Capacitance[3]

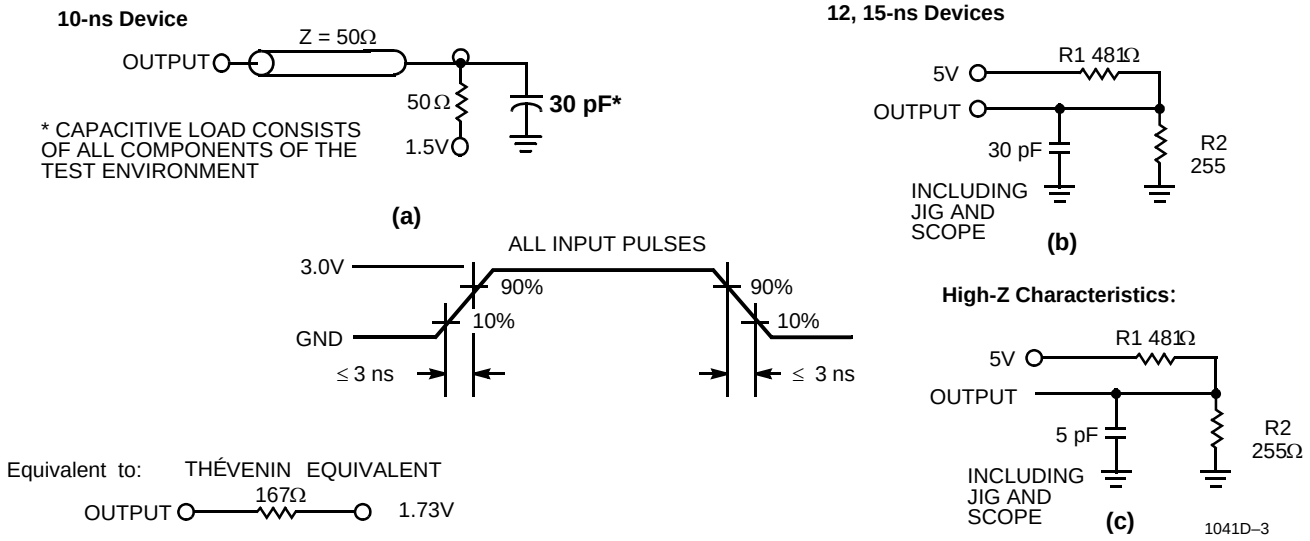
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance[3]

Parameter	Description	Test Conditions	All - Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[3]		TBD	°C/W

Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[4]



Switching Characteristics[5] Over the Operating Range

Parameter	Description	7C1041D-10		7C1041D-12		7C1041D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}	V_{CC}(typical) to the First Access[6]	100		100		100		µs
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		ns
t_{HZBE}	Byte Disable to High Z		5		6		7	ns

Notes:
4. AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.

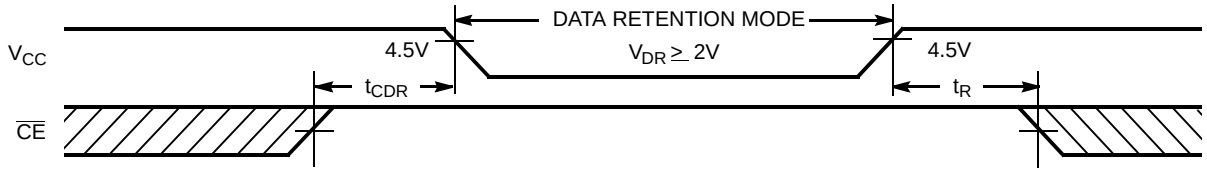
Switching Characteristics[5] Over the Operating Range(continued)

Parameter	Description	7C1041D-10		7C1041D-12		7C1041D-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle[8, 9]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		10		12		ns
t_{AW}	Address Set-Up to Write End	7		10		12		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		10		12		ns
t_{SD}	Data Set-Up to Write End	6		7		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		6		7	ns
t_{BW}	Byte Enable to End of Write	7		10		12		ns

Data Retention Characteristics Over the Operating Range

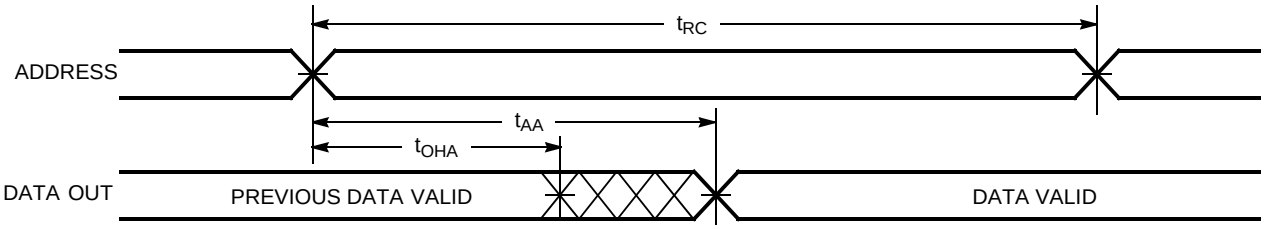
Parameter	Description	Conditions[11]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		10	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0		ns
t_R[10]	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform



Switching Waveforms

Read Cycle No. 1[12, 13]

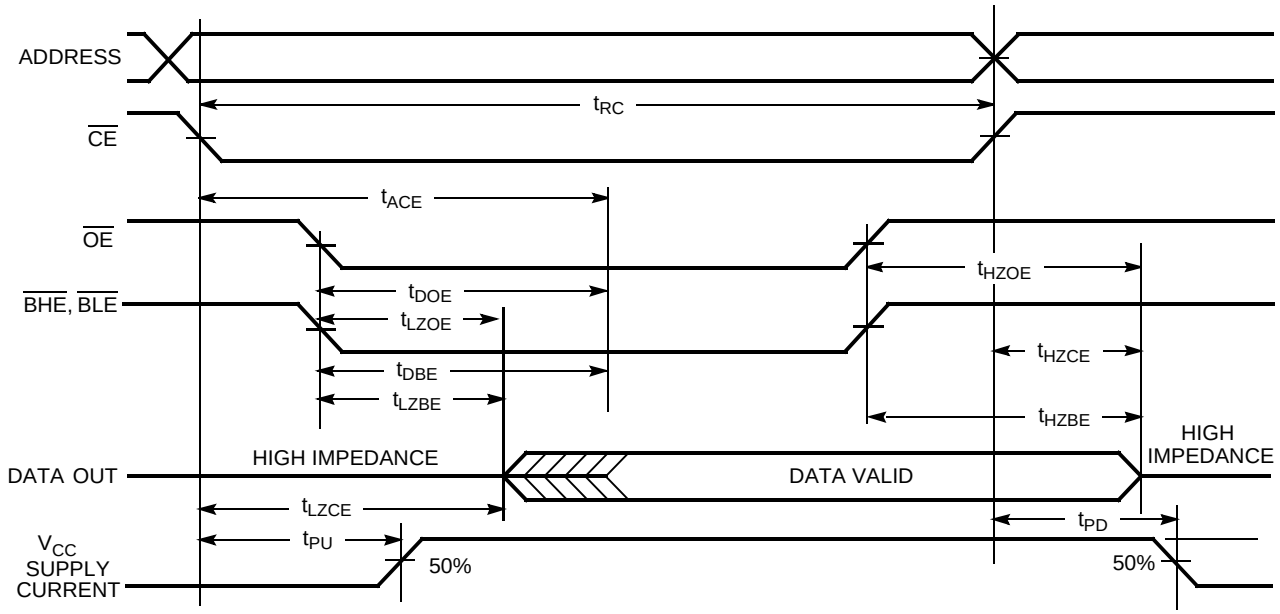


Notes:

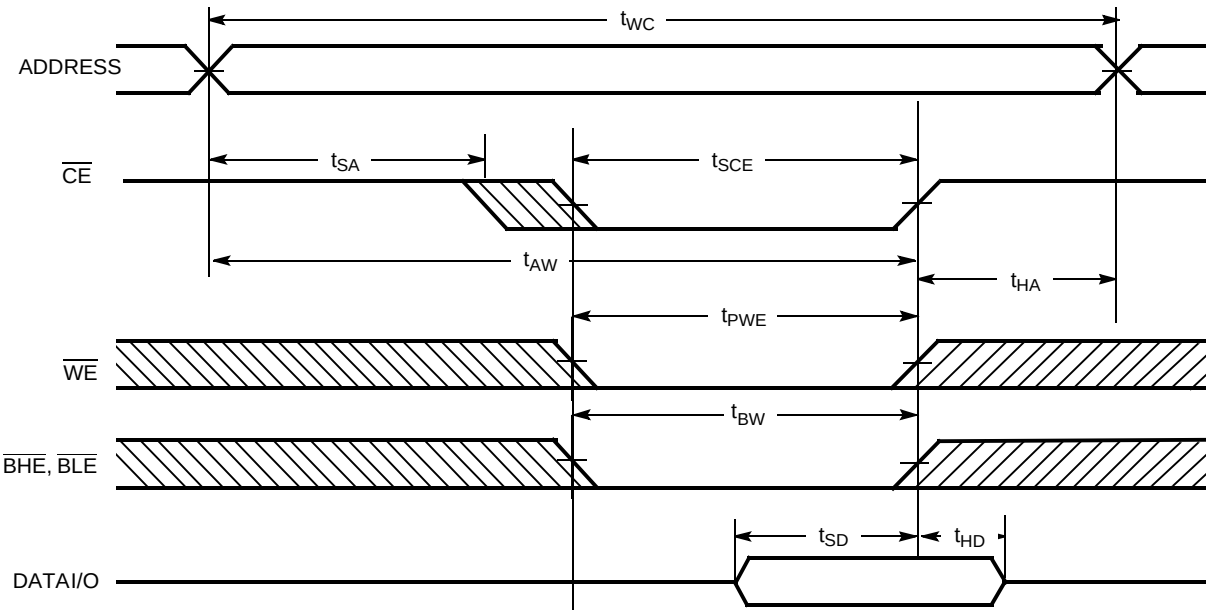
8. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
9. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu s$ or stable at $V_{CC(min.)} \geq 50\ \mu s$
11. No input may exceed V_{CC} + 0.5V
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BHE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (OE Controlled) [13, 14]



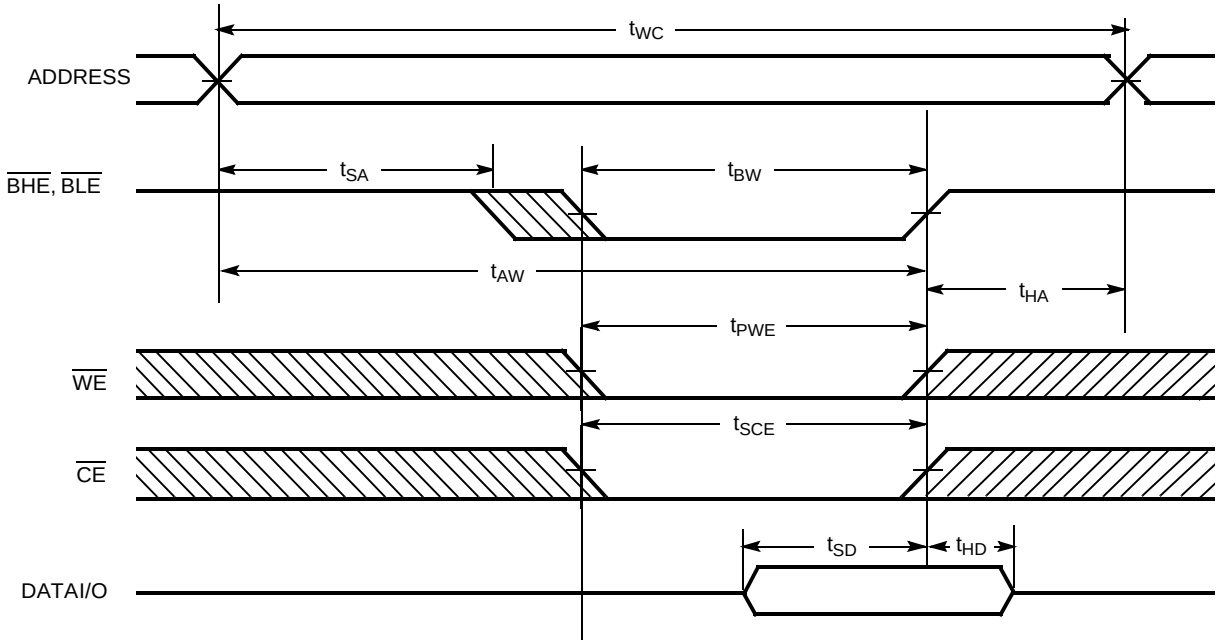
Write Cycle No. 1 (CE Controlled) [15, 16]



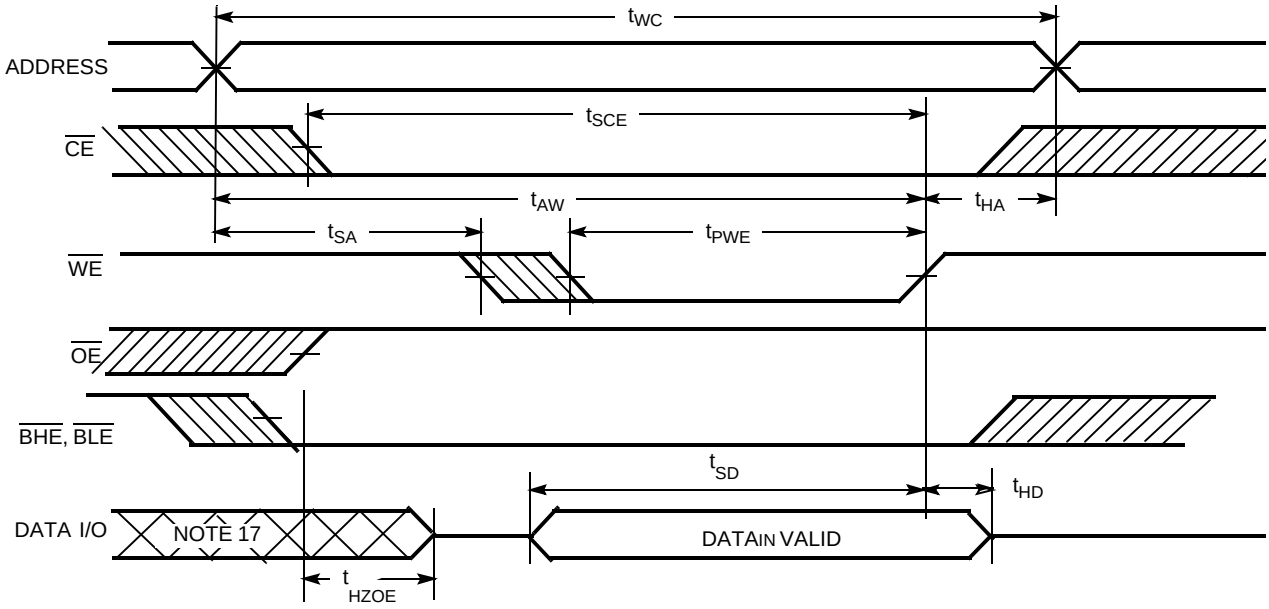
Notes:
14. Address valid prior to or coincident with CE transition LOW
15. Data I/O is high impedance if OE or BHE and/or BLE= V_{IH}.
16. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (BLE or BHE Controlled)

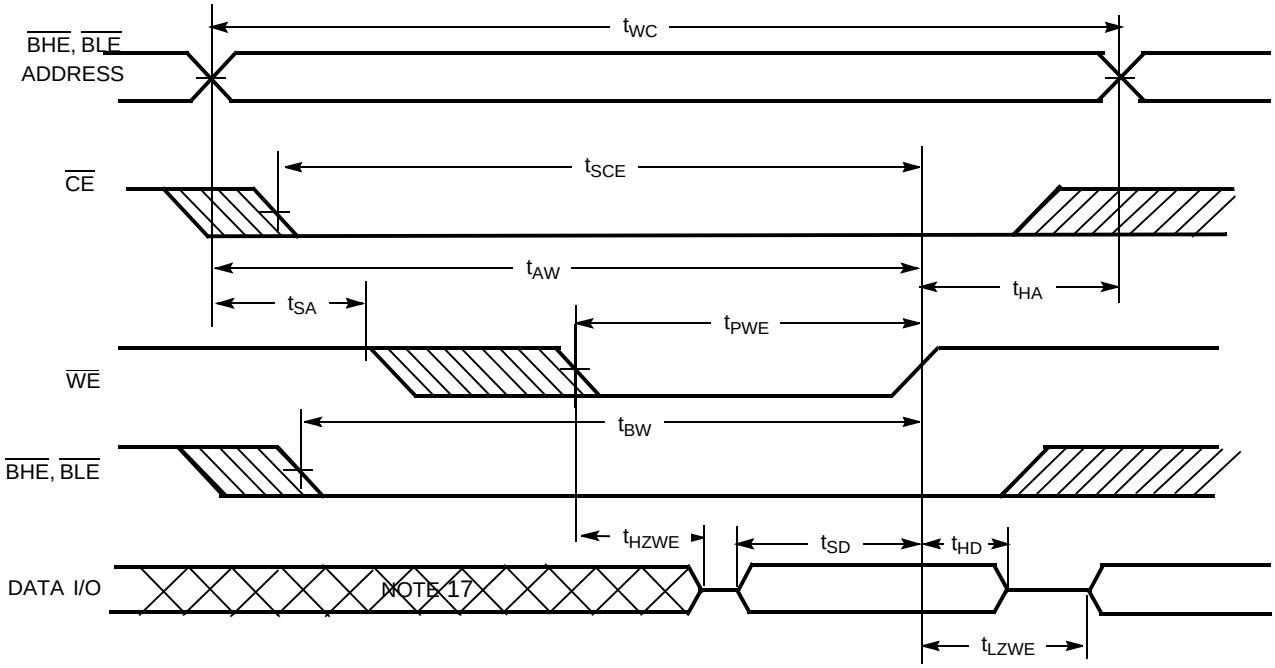


Write Cycle No. 3 (WE Controlled, OE HIGH During Write)[15, 16]



Note:
17. During this period the I/Os are in the output state and input signals should not be applied.

Write Cycle No. 4 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read Lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write Lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

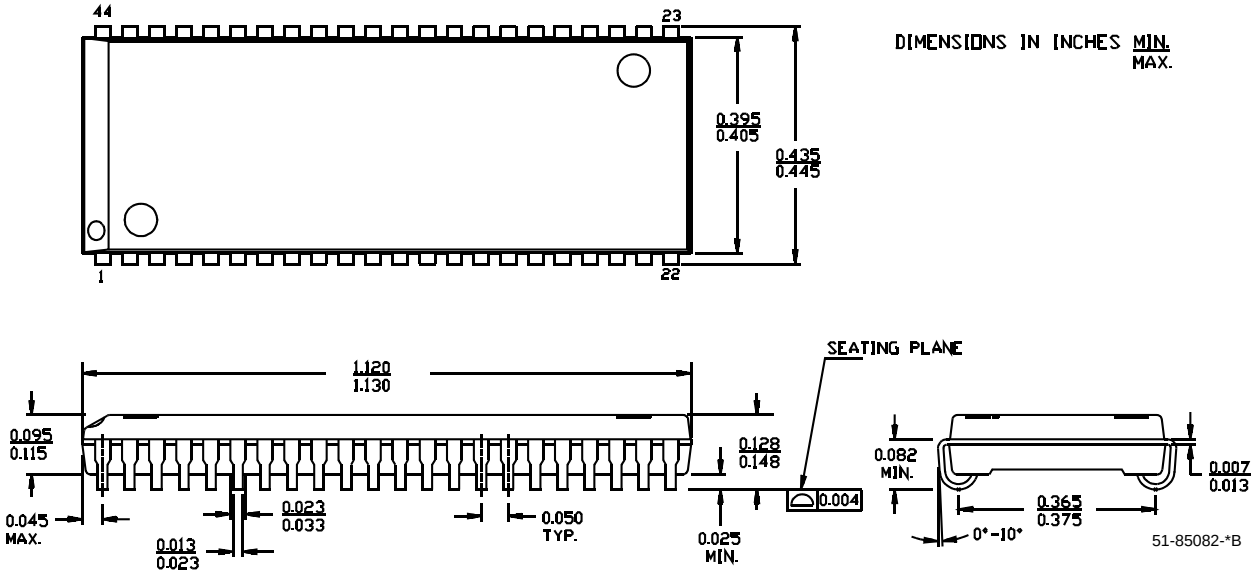
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1041D-10VXC	V44	44-Lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1041D-10ZSXC	ZS44	44-Lead TSOP Type II (Pb-Free)	
	CY7C1041D-10ZSXI	ZS44	44-Lead TSOP Type II (Pb-Free)	Industrial
	CY7C1041D-10VXI	V44	44-Lead (400-Mil) Molded SOJ (Pb-Free)	
12	CY7C1041D-12VXC	V44	44-Lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1041D-12ZSXC	ZS44	44-Lead TSOP Type II (Pb-Free)	
	CY7C1041D-12ZSXI	ZS44	44-Lead TSOP Type II (Pb-Free)	Industrial
	CY7C1041D-12VXI	V44	44-Lead (400-Mil) Molded SOJ (Pb-Free)	
15	CY7C1041D-15VXC	V44	44-Lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1041D-15ZSXC	ZS44	44-Lead TSOP Type II (Pb-Free)	
	CY7C1041D-15ZSXI	ZS44	44-Lead TSOP Type II (Pb-Free)	Industrial
	CY7C1041D-15VXI	V44	44-Lead (400-Mil) Molded SOJ (Pb-Free)	

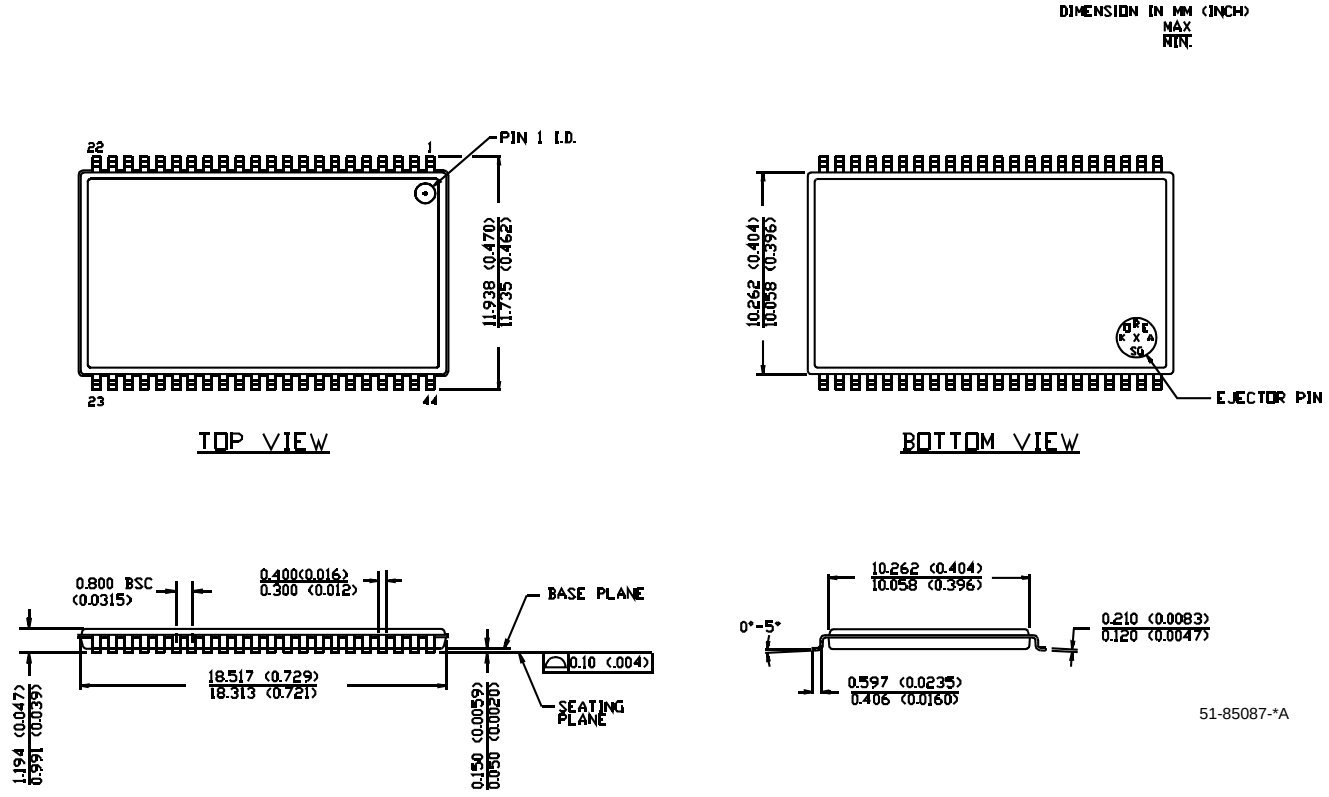
Shaded area contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

44-Lead (400-Mil) Molded SOJ V44



44-Pin TSOP II ZS44



Document History Page

Document Title: CY7C1041D 4-Mbit (256K x 16) Static RAM Document Number: 38-05472				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Datasheet for C9 IPP
*A	233729	See ECN	RKF	1.AC, DC parameters are modified as per EROS (Spec # 01-2165) 2.Pb-free offering in the 'ordering information'
*B	351117	See ECN	PCI	Changed from Advance to Preliminary Removed 17 and 20 ns Speed bin Added footnote # 4 Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I_{CC} (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Changed footnote # 10 on t_R Changed t_{SCE} from 8 to 7 ns for 10 ns speed bin Added Static Discharge Voltage and latch-up current spec Added $V_{IH(max)}$ spec in footnote # 2 Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Write Cycle ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) Timing Diagram Changed part names from Z to ZS in the Ordering Information Table Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Ordering Information Shaded Ordering Information Table