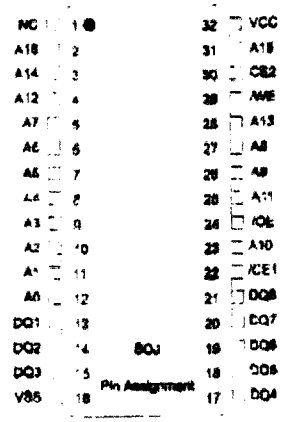
128K x 8 Bit High-Speed CMOS SRAM

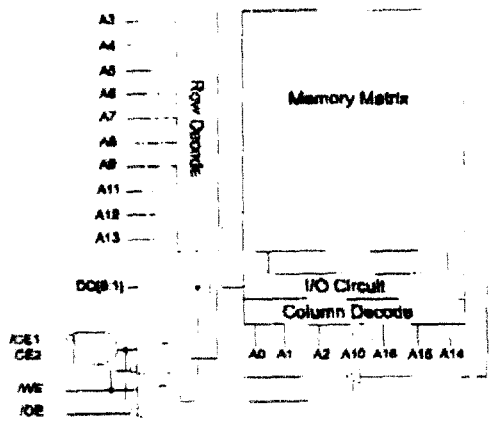


Features

- Fast Address Access Times
  10ns, 12ns, 15ns
- Fast Output Enable Access Times
  6ns, 6ns, 7ns
- Low Power Consumption
  140mA
- Single 5V ±10% Power Supply
- Industry Standard Pin Assignment
- Package Options
  300 mil 32 pin SOJ
  32 pin TSOP Type I (8x20mm)

Description

The EK681024M from Eureka is a one-megabit density fast static random access memory organized as 131,072 words by 8 bits. It is designed for use in high performance memory applications such as main memory storage and high speed communication buffers. Fabricated using high performance CMOS technology, access times down to 10ns are achieved. Memory expansion by banking is easily accomplished using the chip enable pins /CE1 and CE2.



Pin Assignment

Symbol	Description
A0-A16	Address Inputs
DQ1-DQ8	Data Inputs/Outputs
/CE1, CE2	Chip Enables
/WE	Write Enable
/OE	Output Enable
Vcc	Power Supply
Vss	Ground

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{CC}	-0.5 to 7.0	V
Input Voltage	V_{IN}	-0.5 to Vcc + 0.5	V
Output Voltage	V_{OUT}	-0.5 to Vcc +0.5	V
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STO}	-55 to +150	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

/CE1	CE2	/OE	/WE	Mode	DQ Pin	Supply Current
H	X	X	X	Not Selected	High - Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High - Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disabled	High - Z	I_{CCA}
L	H	L	H	Read	Data Out	I_{CCA}
L	H	X	L	Write	Data In	I_{CCA}

Electrical Characteristics and DC Operating Conditions

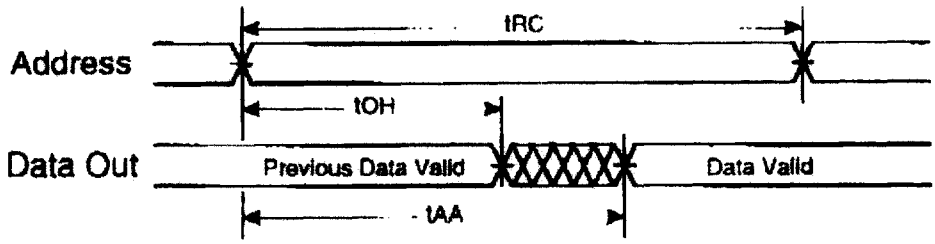
(T_A =0 to + 70°C; Vcc = +5V ±10% unless otherwise noted; Note 1)

Description	Symbol	Conditions	Min	Max	Units
Power Supply Voltage	Vcc		4.5	5.5	V
Input Low Voltage	V_{IL}		-0.5	0.8	V
Input High Voltage	V_{IH}		2.2	Vcc+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = Vss to Vcc	-5	5	µA
Output Leakage Current	I_{LO}	V_{IN}=Vss to Vcc: /CE1=V_{IH} or CE2=V_{IL} or /OE=V_{IH} or /WE=V_{IL}	-5	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4	-	V
Power Supply Operating Current	I_{CCA}	/CE1 = V_{IL}, CE2=V_{IH}; f=max, DQ=0mA		140	mA
Power Supply Standby Current	I_{SB}	/CE1=V_{IH} or CE2=V_{IL}, DQ=0mA		40	mA
CMOS Standby Current	I_{SB1}	Vcc=max; /CE1> Vcc-0.2V or CE2< Vss+0.2v; f=0mhz; DQ=0ma		6	mA

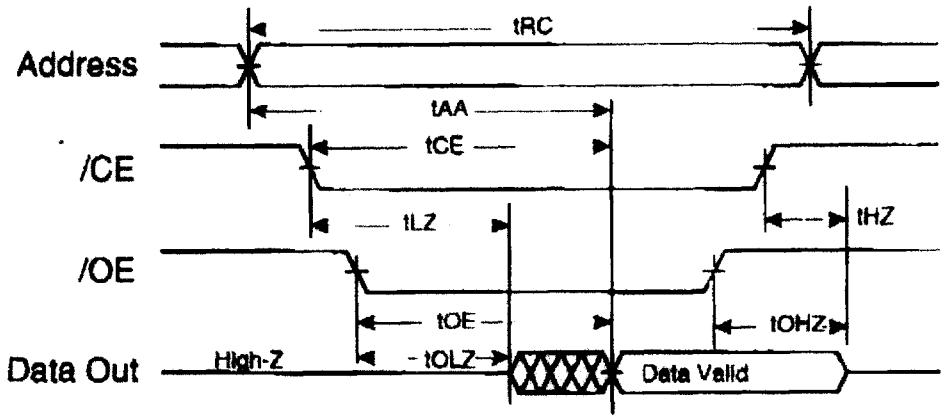
Capacitance

Parameter	Symbol	Max	Units
Input Capacitance	C_{IN}	6	pF
Input/Output Capacitance	C I/O	8	pF

Read Cycle (Address Access)



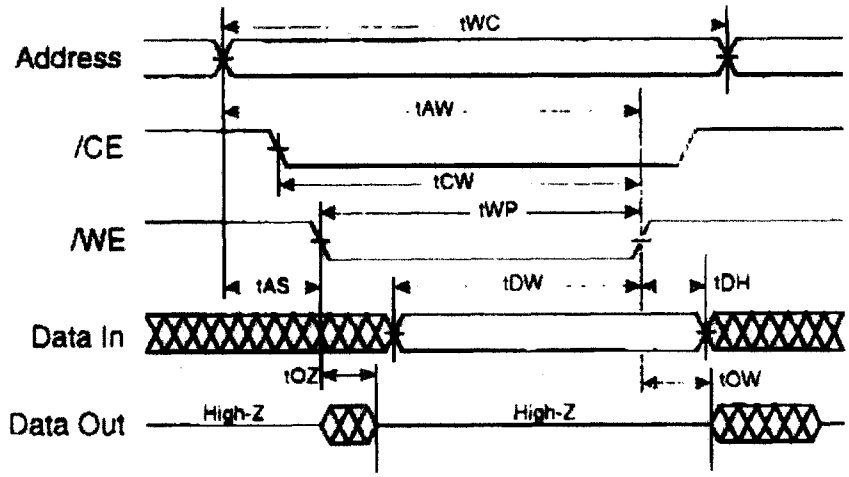
Read Cycle (Chip Enable Access)



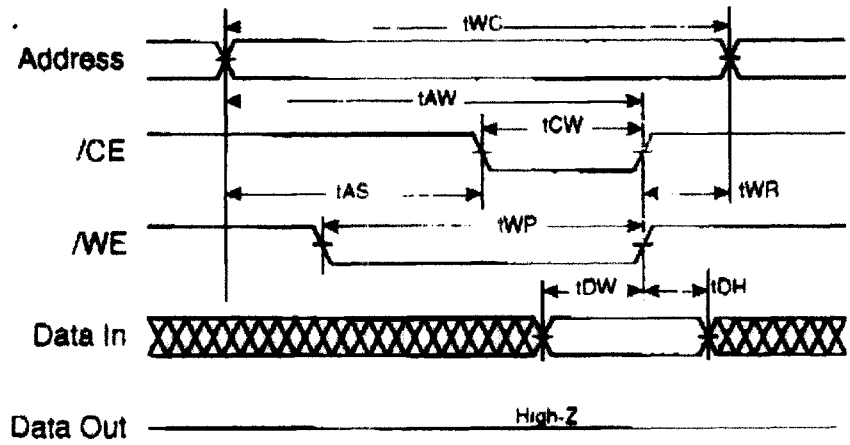
Read Cycle

DESCRIPTION		-10		-12		-15			
	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Read Cycle Time	tRC	10	-	12	-	15	-	ns	2,3,6
Address Access Time	tAA	-	10	-	12	-	15	ns	2,3
Chip Enable Access Time	tCE	-	10	-	12	-	15	ns	2,3
Output Enable Access Time	tOE	-	6	-	6	-	7	ns	2,3
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns	2,3
Chip Enable Active to Low-Z	tLZ	3	-	3	-	3	-	ns	2,3
Output Enable to Low-Z	tOLZ	0	-	0	-	0	-	ns	2,3
Chip Disable Active to High-Z	tHZ	0	3	0	3	0	4	ns	2,3,5
Output Disable to High-Z	tOHZ	0	3	0	3	0	4	ns	2,3,5

Write Cycle (/WE Controlled)



Write Cycle (/CE Controlled)



Write Cycle

DESCRIPTION		-10		-12		-15			
	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Write Cycle Time	tWC	10	-	12	-	15	-	ns	2,4,6
Address Setup Time	tAS	0	-	0	-	0	-	ns	2,4
Address Valid to End of Write	tAW	8	-	10	-	13	-	ns	2,4
Write Pulse Width	tWP	8	-	9	-	11	-	ns	2,4
Chip Enable to End of Write	tCW	8	-	10	-	13	-	ns	2,4
Data Valid to End of Write	tDW	5	-	6	-	8	-	ns	2,4
Data Hold from End of Write	tDH	0	-	0	-	0	-	ns	2,4
Write Low to Output High-Z	tOZ	0	5	0	5	0	5	ns	2,4,5
Write High to Output Low-Z	tOW	3	-	3	-	5	-	ns	2,4
Write Recovery Time	tWR	0	-	0	-	0	-	ns	2,4

AC Test Conditions

(TA = 0 to +70°C, Vcc = 5V ±10%)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	V_{IH}	3	V
Input Pulse Low Level	V_{IL}	0	V
Input Rise Time	TR	3.0	ns
Input Fall Time	TF	3.0	ns
Input and Output Timing Reference Level		1.5	V

AC Test Loads

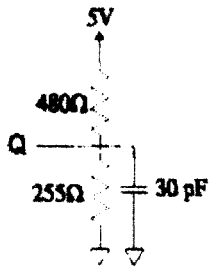


Figure 1A - AC Test Load

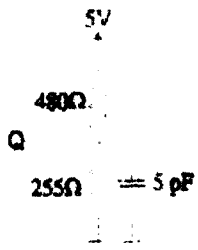


Figure 1B - Hi Z Test Load

Notes:

1. When /WE goes low, outputs are in a Hi-Z state and /OE is overridden.
2. /WE is high for a read cycle.
3. /CE1 and CE2 are represented by /CE in this data sheet. CE2 is of the opposite polarity of /CE in the timing diagrams.
4. A write occurs during the overlap of /CE and /WE.
5. Measured at ±500mv from steady state with the Hi-Z load.
6. Referenced from the last valid address to the first transitioning address pin.

Ordering Information

(Order by Complete Part Number)