

Am8120

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops

GENERAL DESCRIPTION

The Am8120 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

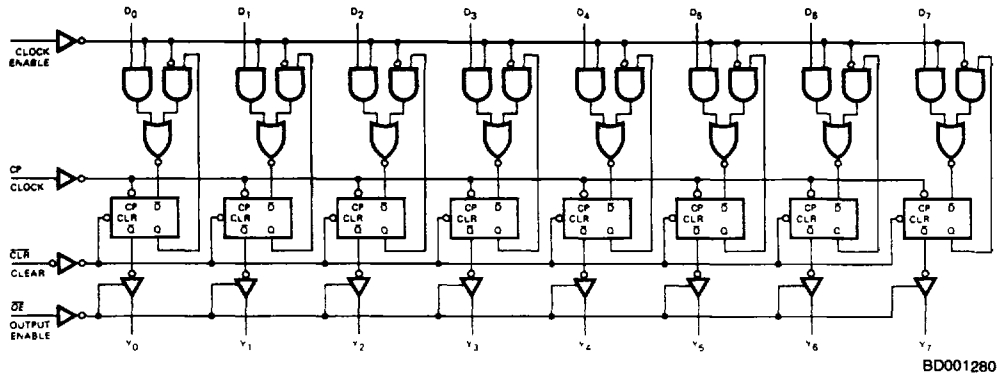
When the three-state output enable (\overline{OE}) input is LOW, the Y outputs are enabled and appear as normal TTL outputs.

When the output enable (\overline{OE}) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input (\overline{E}) is used to selectively load data into the register. When the \overline{E} input is HIGH, the register will retain its current data. When the \overline{E} is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a slim 24-pin package (0.3 inch row spacing).

BLOCK DIAGRAM

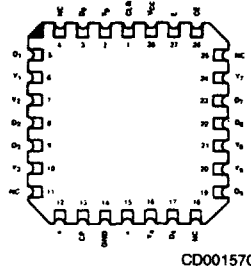
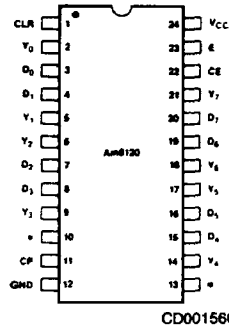


RELATED PRODUCTS

Part No.	Description
Am25S18	Quad D Register
Am2920	Octal D Type Flip-flop
Am2954/5	Octal D Registers

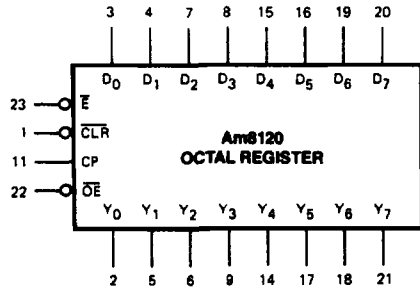
CONNECTION DIAGRAM Top View

Leadless Chip Carrier L-28-1



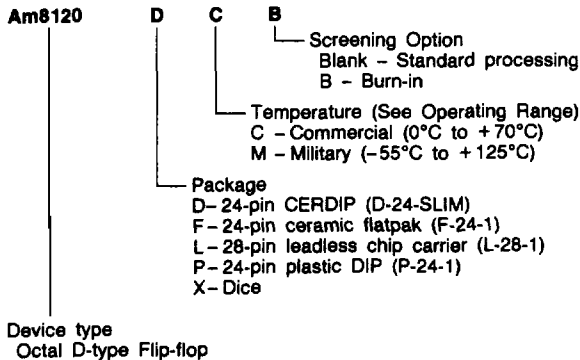
Note: Pin 1 is marked for orientation
*Reserved - do not use.

LOGIC SYMBOL



ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am8120	DC, DM FM LC, LM PC XC, XM

Valid Combinations
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D _i	I	The D flip-flop data inputs.
1	CLR	I	When the clear input is LOW, the Q _i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.
11	CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
	Y _i	O	The register three-state outputs.
23	E	I	Clock Enable. When the clock enable is LOW, data on the D _i input is transferred to the Q _i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q _i outputs do not change state, regardless of the data or clock input transitions.
22	OE	I	Output Control. When the OE input is HIGH, the Y _i outputs are in the high impedance state. When the OE input is LOW, the TRUE register data is present at the Y _i outputs.

Function Table

Inputs					Internal	Outputs	Function
OE	CLR	E	D _i	CP	Q _i	Y _i	
H	X	X	X	X	X	Z	Hi-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH NC = No Change
 L = LOW ↑ = LOW-to-HIGH Transition
 X = Don't Care Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential	
Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs For	
High Output State	-0.5V to +V _{CC} max
DC Input Voltage	-0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V
Military (M) Devices	
Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	MIL, I _{OH} = -1.0mA	2.4	3.4		Volts
			COM'L, I _{OH} = -2.6mA	2.4	3.4		
V _{OL}	Output LOW Voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0mA			0.4	Volts
			I _{OL} = 8.0mA			0.45	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7 0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA				-1.5	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.4V				-0.36	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.7V				20	μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 7.0V				0.1	mA
I _O	Off-State (High-Impedance) Output Current	V _{CC} = MAX	V _O = 0.4V			-20	μA
			V _O = 2.4V			20	
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX		-15		-85	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX			24	37	mA

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. All outputs open, E = GND, D_i inputs = CLR = OE = 4.5V. Apply momentary ground, then 4.5V to clock input.

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units	
t_{PLH}	Clock to Y_i (\overline{OE} LOW)	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$		18	27	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)			10	3	ns	
t_h	Data (D_i)			10	3	ns	
t_s	Enable (\overline{E})		Active		15	10	ns
			Inactive		20	12	
t_h	Enable (\overline{E})			0	0	ns	
t_s	Clear Recovery (In-Active) to Clock			11	7	ns	
t_{pw}	Clock		HIGH		20	14	ns
			LOW		25	13	
t_{pw}	Clear			20	13	ns	
t_{ZH}	\overline{OE} to Y_i				9	13	ns
t_{ZL}					14	21	
t_{HZ}	\overline{OE} to Y_i	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		20	30	ns	
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

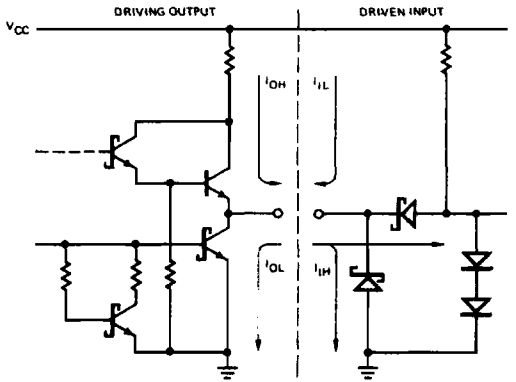
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units	
			Min	Max	Min	Max		
t_{PLH}	Clock to Y_i (\overline{OE} LOW)	$C_L = 50\text{pF}$ $R_L = 2.0\text{k}\Omega$		33		39	ns	
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)			12		15	ns	
t_h	Data (D_i)			12		15	ns	
t_s	Enable (\overline{E})		Active		17		20	ns
			Inactive		20		23	
t_h	Enable (\overline{E})			0		0	ns	
t_s	Clear Recovery (In-Active) to Clock			13		15	ns	
t_{pw}	Clock		HIGH		25		30	ns
			LOW		30		35	
t_{pw}	Clear			22		25	ns	
t_{ZH}	\overline{OE} to Y_i				19		25	ns
t_{ZL}					30		39	
t_{HZ}	\overline{OE} to Y_i	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		35		40	ns	
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.