INTEGRATED CIRCUITS
UNITRODE

UC1725
UC2725
UC3725

Isolated High Side FET Driver

FEATURES

- Receives Both Power and Signal Across the Isolation Boundary
- 9 to 15 Volt High Level Gate Drive
- Under-voltage Lockout
- Programmable Over-current Shutdown and Restart
- Output Enable Function

DESCRIPTION

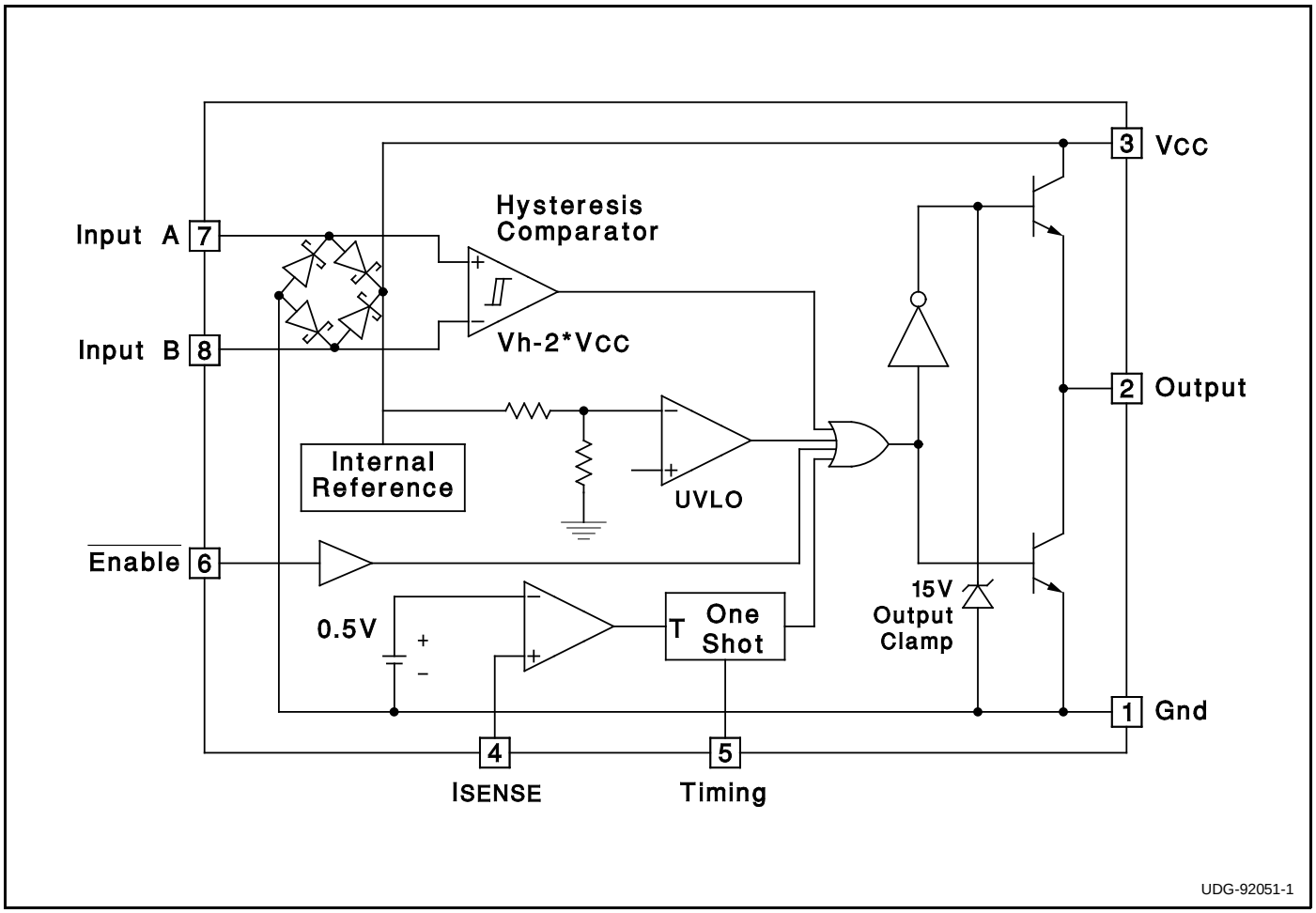
The UC1725 and its companion chip, the UC1724, provide all the necessary features to drive an isolated MOSFET transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signals across an isolation boundary with a minimum of external components.

Protection circuitry, including under-voltage lockout, over-current shutdown, and gate voltage clamping provide fault protection for the MOSFET. High level gate drive is guaranteed to be greater than 9 volts and less than 15 volts under all conditions.

Uses include isolated off-line full bridge and half bridge drives for driving motors, switches, and any other load requiring full electrical isolation.

The UC1725 is characterized for operation over the full military temperature range of -55°C to +125°C while the UC2725 and UC3725 are characterized for -25°C to +85°C and 0°C to +70°C respectively.

BLOCK DIAGRAM



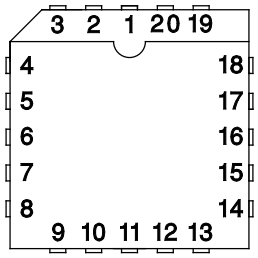
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 3) 30V
Power inputs (pins 7 & 8) 30V
Output current, source or sink (pin 2)
DC. 0.5A
Pulse (0.5 us) 2.0A
Enable and Current limit inputs (pins 4 & 6). . . . . -0.3 to 6V
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals (pin numbers refer to DIL-8 package).
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

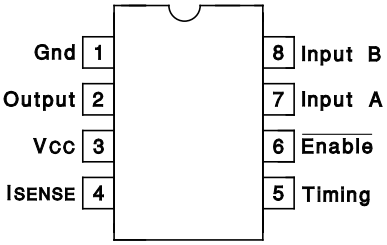
CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package

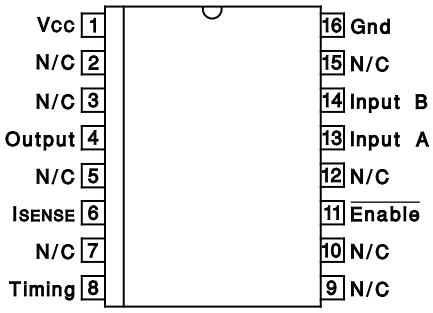


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
I_{SENSE}	2
N/C	3-5
Timing	6
$\overline{\text{Enable}}$	7
N/C	8-9
Input A	11
N/C	12-14
Input B	15
Gnd	16
V_{CC}	17
N/C	18-19
Output	20

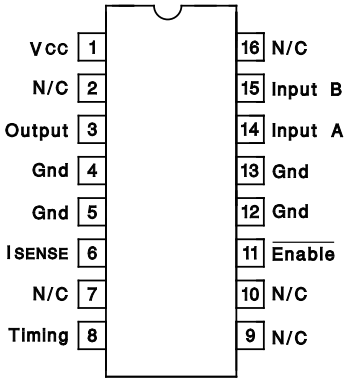
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE Or NE Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for $-55°C \leq T_A \leq +125°C$ for UC1725; $-25°C \leq T_A \leq +85°C$ for UC2725; $0°C \leq T_A \leq +70°C$ for UC3725; V_{CC} (pin 3) = 0 to 15V, R_T=10k, C_T=2.2nf, $T_A = T_J$, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT SECTION (PINS 7 & 8)					
Forward Diode Drop, Schottky Rectifier	I_F = 50ma		.55	.7	V
	I_F = 500ma		1.1	1.5	V
CURRENT LIMIT SECTION (PIN 4)					
Input bias current	V_{PIN4} = OV		-1	-10	µA
Threshold voltage		0.4	0.5	0.6	V
Delay to outputs	V_{PIN4} = 0 to 1V		100	250	ns
TIMING SECTION (PIN 5)					
Output Off Time		27	30	33	µs
Upper Mono Threshold		6.3	7.0	7.7	V
Lower Mono Threshold		1.9	2.0	2.3	V
HYSTERESIS AMPLIFIER (PINS 7 & 8)					
Input Open Circuit Voltage	Inputs (pins 7 & 8), Open Circuited, T_A= 25°C	7.0	Vcc/2	8.0	V
Input Impedance	T_A = 25°C	23	28	33	kΩ
Hysteresis		26.5	2*Vcc	30.5	V
Delay to Outputs	$V_{PIN7} - V_{PIN8} = V_{CC}$ + 1V		100	300	ns

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for -55°C≤T_A≤+125°C for UC1725; -25°C≤T_A≤+85°C for UC2725; 0°C≤T_A≤+70°C for UC3725; V_{CC} (pin 3) = 0 to 15V, Rt=10k, C_T=2.2nf, T_A =T_J, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE SECTION (PIN 6)					
High Level Input Voltage		2.1	1.4		V
Low Level Input Voltage			1.4	.8	V
Input Bias Current			-250	-500	µA
OUTPUT SECTION					
Output Low Level	I_{OUT} = 20mA		0.35	0.5	V
	I_{OUT} = 200mA		0.6	2.5	V
Output High Level	I_{OUT} = -20mA	13	13.5		V
	I_{OUT} = -200mA	12	13.4		V
	V_{CC} = 30V, Iout = -20mA		14	15	V
Rise/Fall Time	C_T = 1nf		30	60	ns
UNDER VOLTAGE LOCKOUT					
UVLO Low Saturation	20mA, V_{CC} = 8V		0.8	1.5	V
Start-up Threshold		11.2	12	12.6	V
Threshold Hysteresis		.75	1.0	1.12	V
TOTAL STANDBY CURRENT					
Supply Current			12	16	ma

APPLICATION AND OPERATION INFORMATION

INPUTS: Figure 1 shows the rectification and detection scheme used in the UC1725 to derive both power and signal information from the input waveform. Vcc is generated by peak detecting the input signal via the internal bridge rectifier and storing on a small external capacitor, C1. Note that this capacitor is also used to bypass high pulse currents in the output stage, and therefore should be placed direclty between pins 1 and 3 using minimal lead lengths.

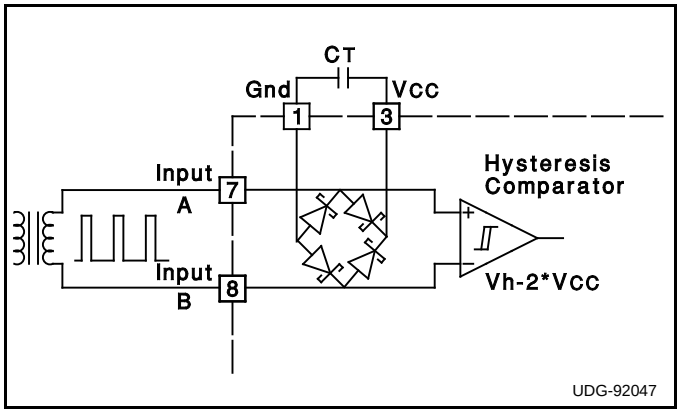


FIGURE 1 - Input Stage

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (resetting) the comparator only if the input signal exceeds Vcc (-Vcc). In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis amplifier as shown in Figure 3.

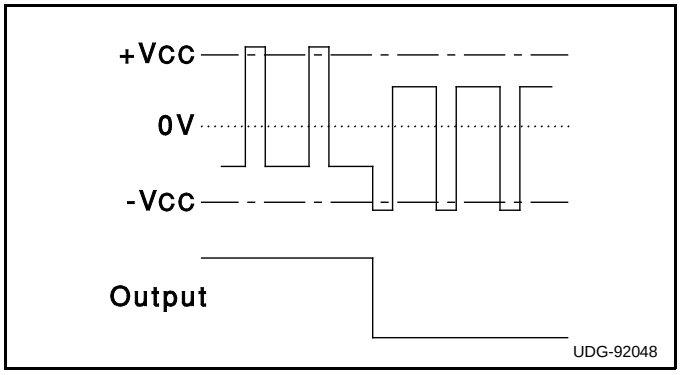


FIGURE 2 - Input Waveform (DIL-8 Pin 7 - Pin 8)

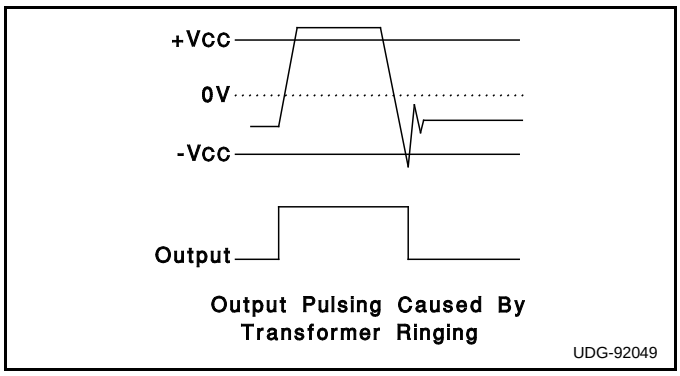


FIGURE 3 - Signal Detection

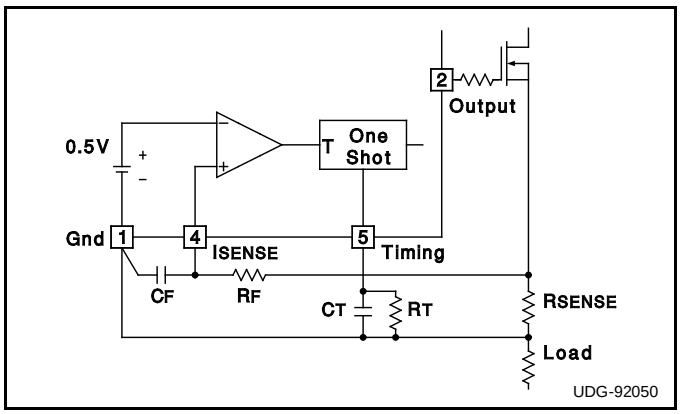


FIGURE 4 - Current Limit

CURRENT LIMIT AND TIMING: Current sensing and shutdown can be implemented directly at the output using the scheme shown in Figure 4. Alternatively, a current transformer can be used in place of RSENSE. A small RC filter in series with the input (pin 4) is generally needed to eliminate the leading edge current spike caused by parasitic circuit capacitances being charged during turn on. Due to the speed of the current sense circuit, it is very important to ground CF directly to Gnd as shown to eliminate false triggering of the one shot caused by ground drops.

One shot timing is easily programmed using an external capacitor and resistor as shown in Figure 4. This, in turn, controls the output off time according to the formula:

$$T_{OFF} = 1.28 \bullet RC.$$

If current limit feature is not required, simply ground pin 4 and leave pin 5 open.

OUTPUT: Gate drive to the power FET is provided by a totem pole output stage capable of sourcing and sinking currents in excess of 1 amp. The undervoltage lockout circuit guarantees that the high level output will never be less than 9 volts. In addition, during undervoltage lockout, the output stage will actively sink current to eliminate the need for an external gate to source resistor. High level output is also clamped to 15 volts. Under high capacitive loading however, the output may overshoot 2 to 3 volts, due to the drivers' inabitlity to switch from full to zero output current instantaneously. In a practical circuit this is not normally a concern. A few ohms of series gate resistance is normally required to prevent parasitic oscillations, and will also eliminate overshoot at the gate.

ENABLE: An enable pin is provided as a fast, digital input that can be used in a number of applications to directly switch the output. Figure 6 shows a simple means of providing a fast, high voltage translation by using a small signal, high voltage transistor in a cascode configuration. Note that the UC1725 is still used to provide power, drive and protection circuitry for the power FET.

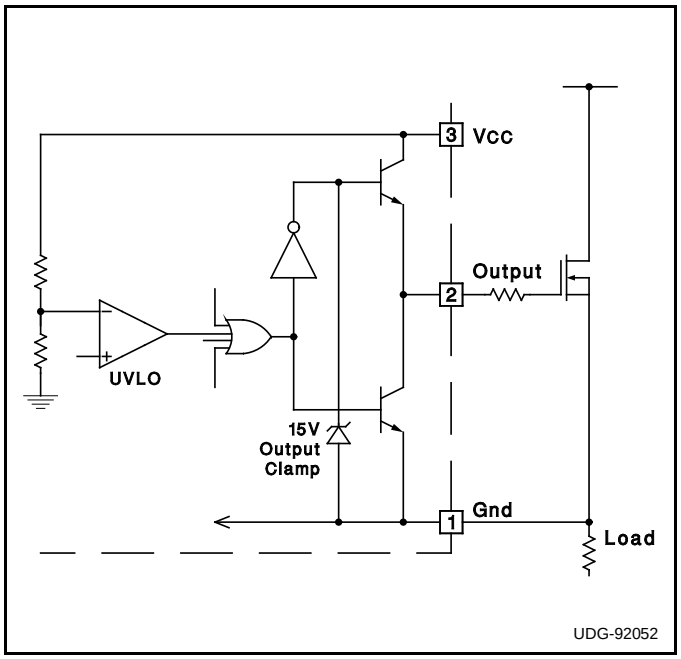


FIGURE 5 - Output Circuit

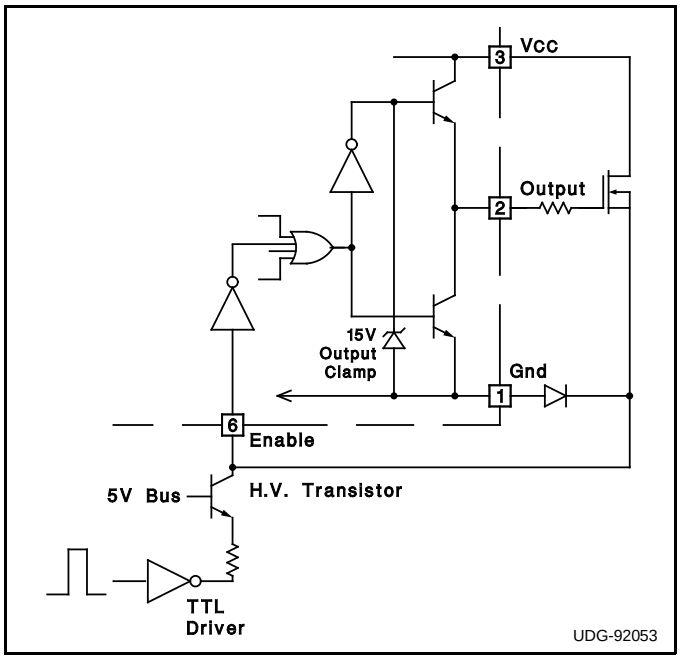


FIGURE 6 - Using Enable Pin as a High Speed Input Path

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UC2725J	OBSOLETE	CDIP	J	8		TBD	Call TI	Call TI
UC3725DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC3725DWTR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC3725N	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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