

- **DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Less Than 2-ns Maximum Propagation Delay at 2.5-V and 3.3-V  $V_{CC}$**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$**
- **Oversvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Package Options Include Plastic Small-Outline (DW), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages**

## description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

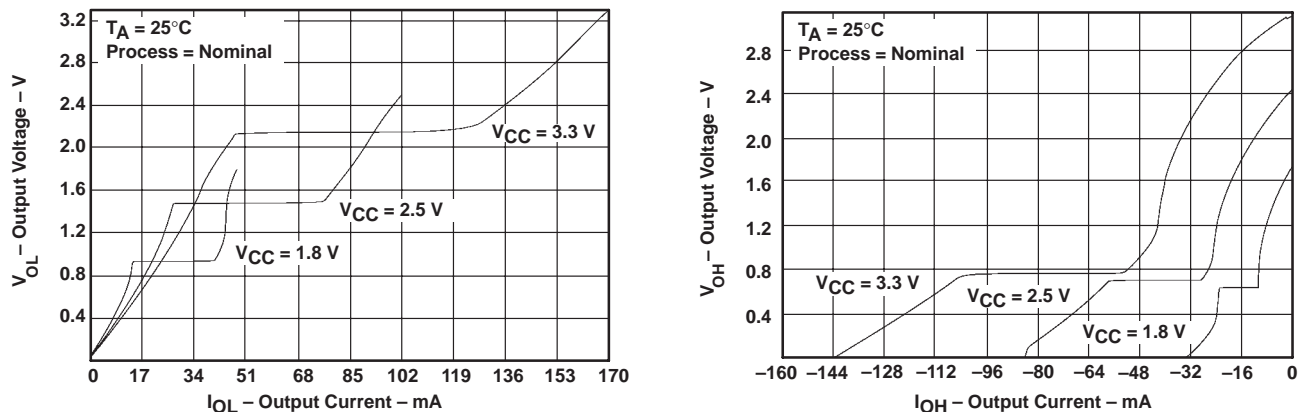


Figure 1. Output Voltage vs Output Current

This octal bus transceiver is operational at 1.2-V to 3.6-V  $V_{CC}$ , but is designed specifically for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74AVC245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.



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# SN74AVC245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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## description (continued)

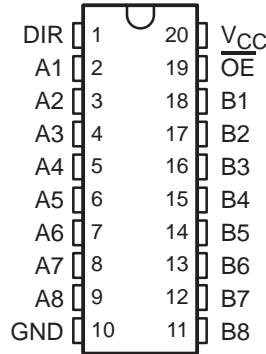
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## terminal assignments

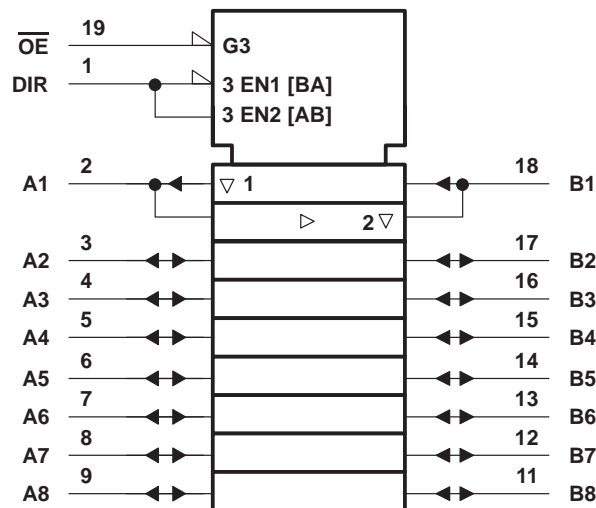
DGV, DW, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

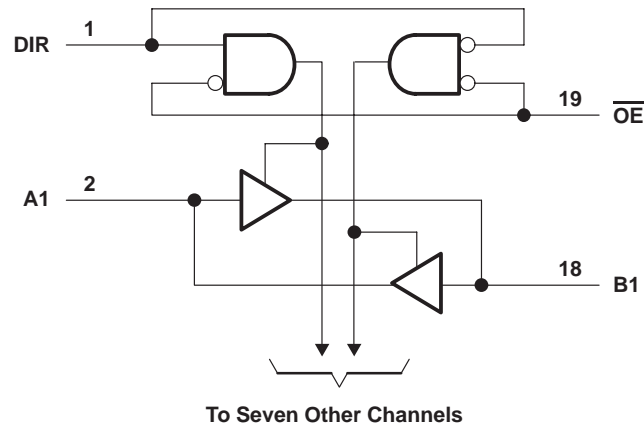
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1) .....	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any input/output when the output is in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 4.6 V
Voltage range applied to any input/output when the output is in the high or low state, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through each $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGV package .....	92°C/W
DW package .....	58°C/W
PW package .....	83°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.2		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.2 V	GND		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage	0	3.6	V	
V <sub>O</sub>	Output voltage	Active state	0	V <sub>CC</sub>	V
		3-state	0	3.6	
I <sub>OHS</sub>	Static high-level output current†	V <sub>CC</sub> = 1.65 V to 1.95 V	–4		mA
		V <sub>CC</sub> = 2.3 V to 2.7 V	–8		
		V <sub>CC</sub> = 3 V to 3.6 V	–12		
I <sub>OLS</sub>	Static low-level output current†	V <sub>CC</sub> = 1.65 V to 1.95 V	4		mA
		V <sub>CC</sub> = 2.3 V to 2.7 V	8		
		V <sub>CC</sub> = 3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.65 V to 3.6 V		5	ns/V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C	

† Dynamic drive capability is equivalent to standard outputs with I<sub>OH</sub> and I<sub>OL</sub> of ±24 mA at 2.5-V V<sub>CC</sub>. See Figure 1 for V<sub>OL</sub> vs I<sub>OL</sub> and V<sub>OH</sub> vs I<sub>OH</sub> characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number **SCEA006**, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OHS</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
		I <sub>OHS</sub> = -4 mA, V <sub>IH</sub> = 1.07 V	1.65 V	1.2			
		I <sub>OHS</sub> = -8 mA, V <sub>IH</sub> = 1.7 V	2.3 V	1.75			
		I <sub>OHS</sub> = -12 mA, V <sub>IH</sub> = 2 V	3 V	2.3			
V <sub>OL</sub>		I <sub>OLS</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
		I <sub>OLS</sub> = 4 mA, V <sub>IL</sub> = 0.57 V	1.65 V			0.45	
		I <sub>OLS</sub> = 8 mA, V <sub>IL</sub> = 0.7 V	2.3 V			0.55	
		I <sub>OLS</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	3 V			0.7	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±2.5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0			±10	μA
I <sub>OZ</sub> ‡		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V				pF
			3.3 V				
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V				pF
			3.3 V				

† Typical values are measured at T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A										ns
t <sub>en</sub>	$\overline{OE}$	A or B										ns
t <sub>dis</sub>	$\overline{OE}$	A or B										ns

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz			pF
		Outputs disabled				

**PRODUCT PREVIEW**

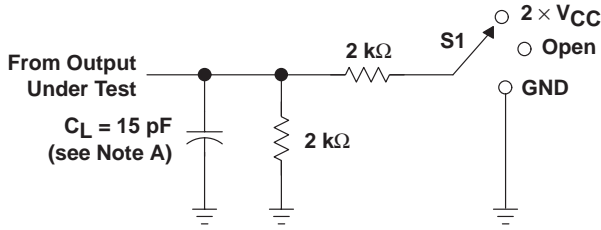


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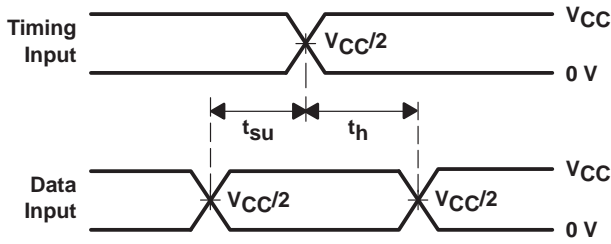
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.2\text{ V AND }1.5\text{ V} \pm 0.1\text{ V}$

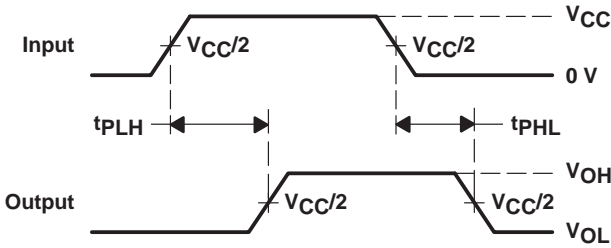


**LOAD CIRCUIT**

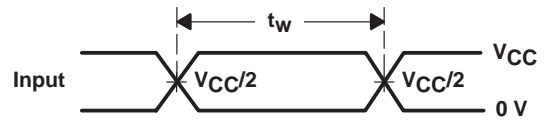
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



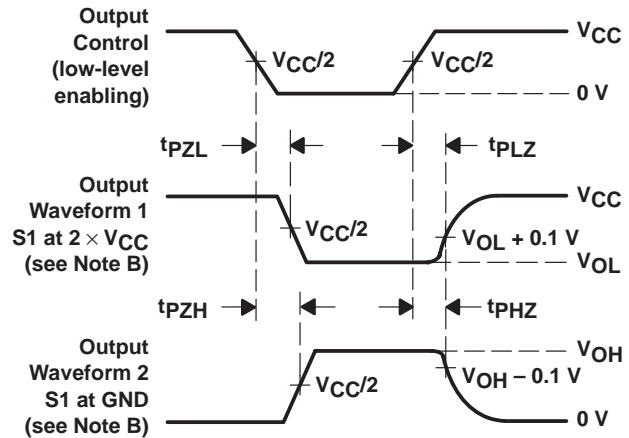
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

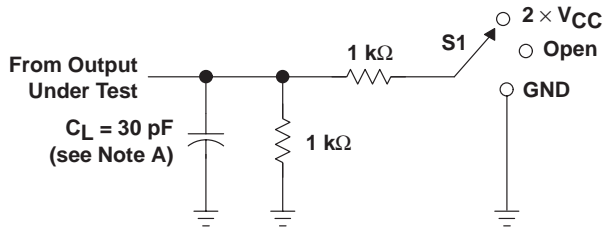
- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

**PRODUCT PREVIEW**

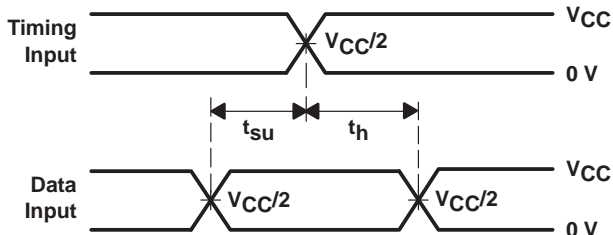
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

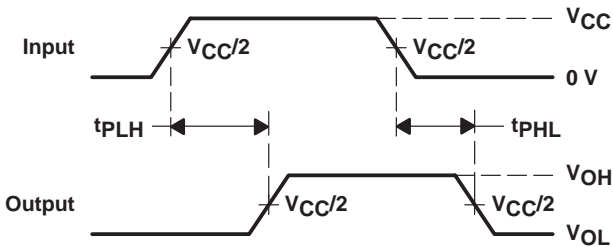


LOAD CIRCUIT

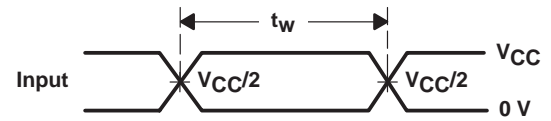
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



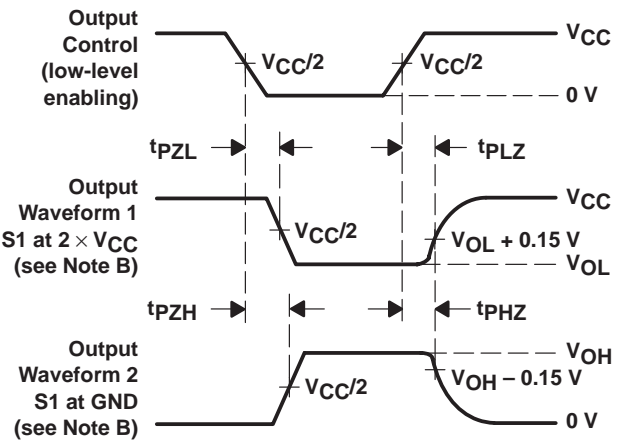
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

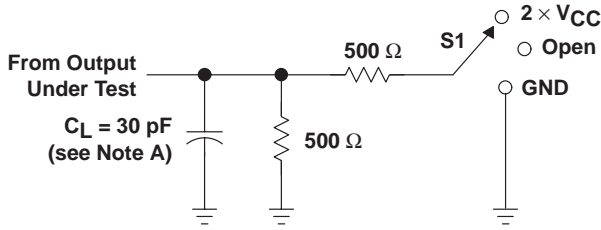
Figure 3. Load Circuit and Voltage Waveforms

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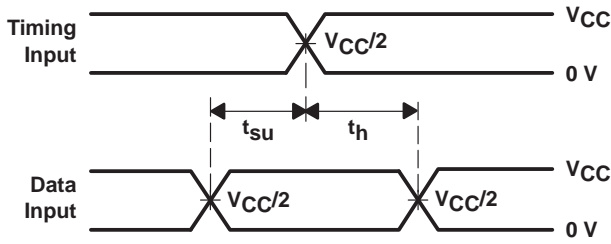
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5 V \pm 0.2 V$

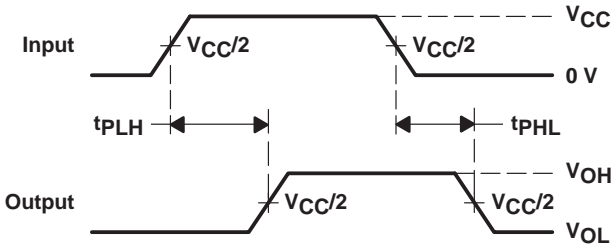


**LOAD CIRCUIT**

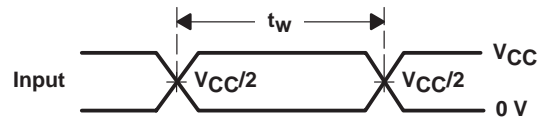
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



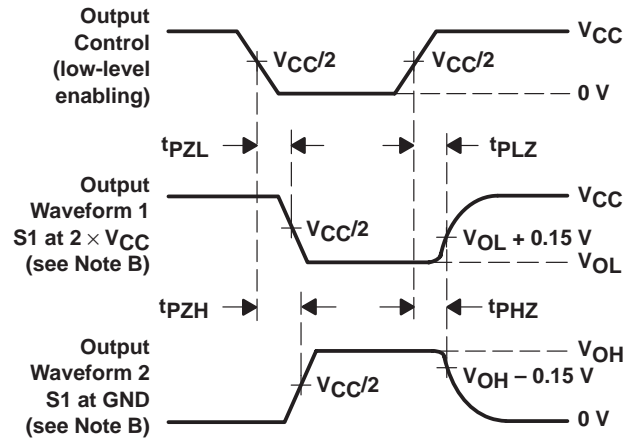
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

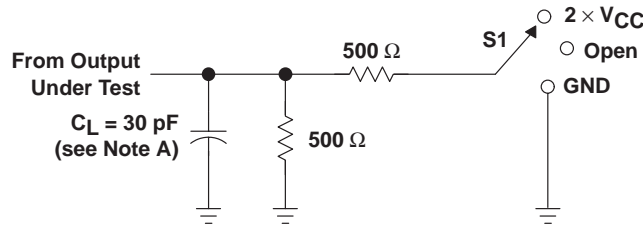
**Figure 4. Load Circuit and Voltage Waveforms**

**PRODUCT PREVIEW**



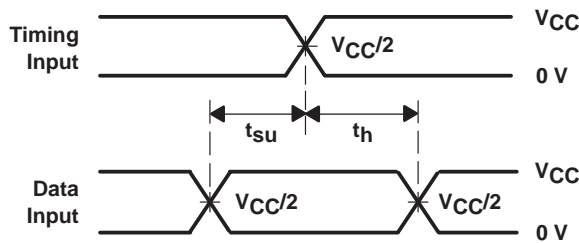
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

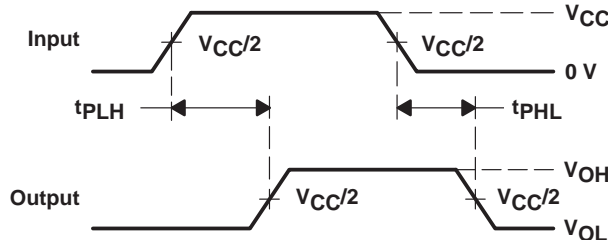


LOAD CIRCUIT

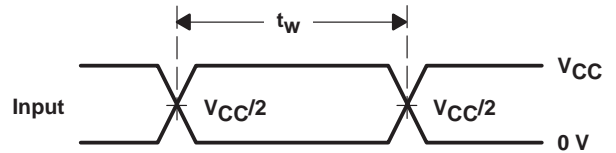
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



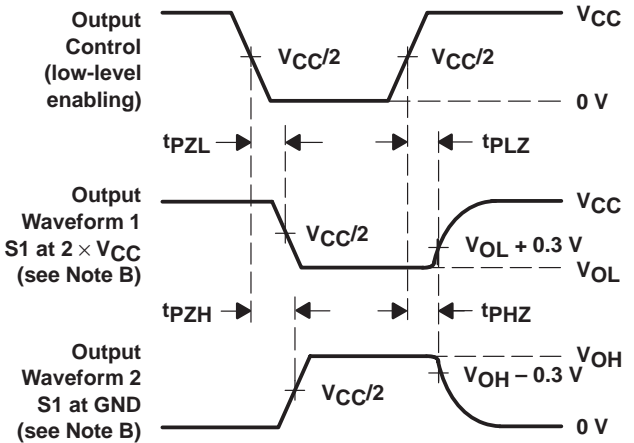
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 5. Load Circuit and Voltage Waveforms

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