IDT74LVC543A

3.3V CMOS OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

FEATURES:

- **0.5 MICRON CMOS Technology**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ± 0.3V, Normal Range**
- **V_{CC} = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-rail output swing for increased noise margin**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in SOIC, SSOP, QSOP, and TSSOP packages**

DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Reduced system switching noise**

APPLICATIONS:

- **5V and 3.3V mixed voltage systems**
- **Data communication and telecommunication systems**

DESCRIPTION:

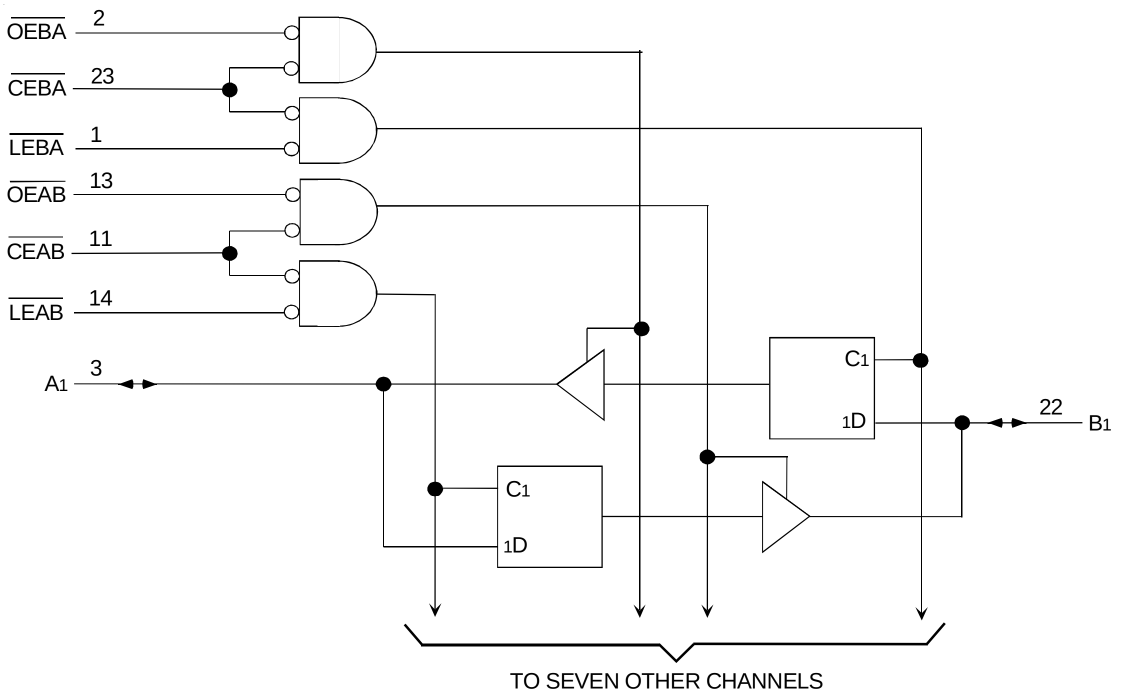
The LVC543A octal registered transceiver is built using advanced dual metal CMOS technology. The device contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data to B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ places the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow for B to A is similar to that of A to B, but uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

The LVC543A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

FUNCTIONAL BLOCK DIAGRAM



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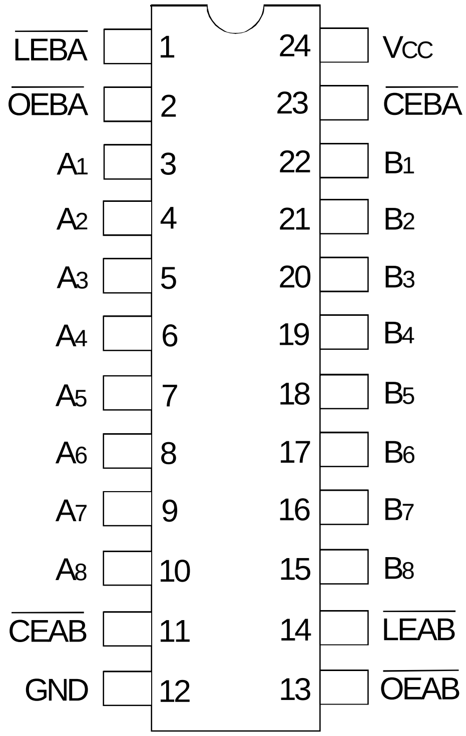
PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +6.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	–50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE[1,2]

Inputs				Outputs
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	Ax	Bx
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B[3]
L	L	L	L	L
L	L	L	H	H

NOTES:

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High-Impedance
2. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
3. Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.[1]	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			$3.6 \leq V_{IN} \leq 5.5V$[2]	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND		—	—	500	µA

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3V		2.4	—	
		V_{CC} = 3V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3V	I_{OL} = 24mA	—	0.55	

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs enabled	C_L = 0pF, f = 10Mhz	49	pF
C_{PD}	Power Dissipation Capacitance per Transceiver Outputs disabled		6	

SWITCHING CHARACTERISTICS(1)

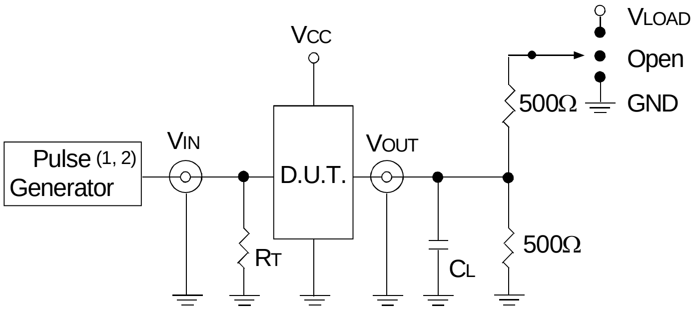
Symbol	Parameter	V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Bx to Ax	—	8	1	7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$ to Ax or Bx	—	9.5	1.2	8.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to Ax or Bx	—	9.2	1.3	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to Ax or Bx	—	9.3	1.3	8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ to Ax or Bx	—	7.5	1	7	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$ to Ax or Bx	—	7.5	1	7	ns
t_{SU}	Set-up Time HIGH or LOW Ax or Bx to $\overline{\text{LEAB}}$↑ or $\overline{\text{LEBA}}$↑, $\overline{\text{CEAB}}$↑ or $\overline{\text{CEBA}}$↑	3.3	—	3.3	—	ns
t_H	Hold Time HIGH or LOW Ax or Bx to $\overline{\text{LEAB}}$↑ or $\overline{\text{LEBA}}$↑, $\overline{\text{CEAB}}$↑ or $\overline{\text{CEBA}}$↑	1.6	—	1.6	—	ns
t_W	Pulse Duration, $\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$, $\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$ LOW	2.1	—	2.1	—	ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V_{CC}[1]=3.3V±0.3V	V_{CC}[1]=2.7V	V_{CC}[2]=2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x V_{CC}	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	V_{CC} / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



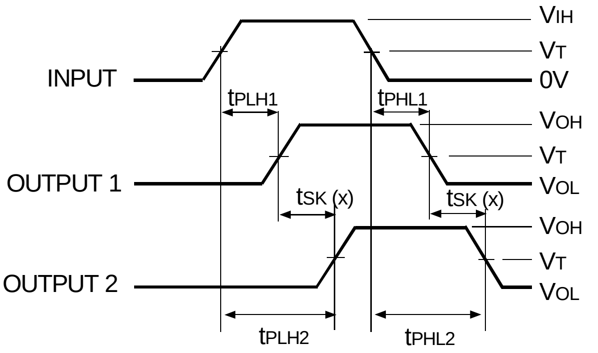
Test Circuit for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

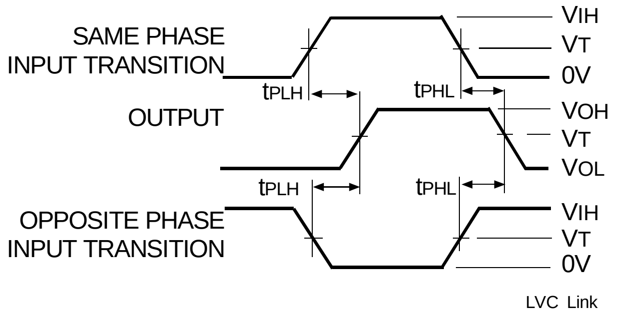


$t_{SK}(x) = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

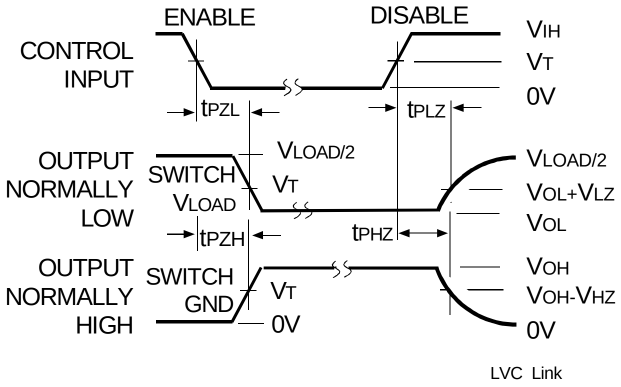
LVC Link

Output Skew - $t_{SK}(x)$

NOTES:
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

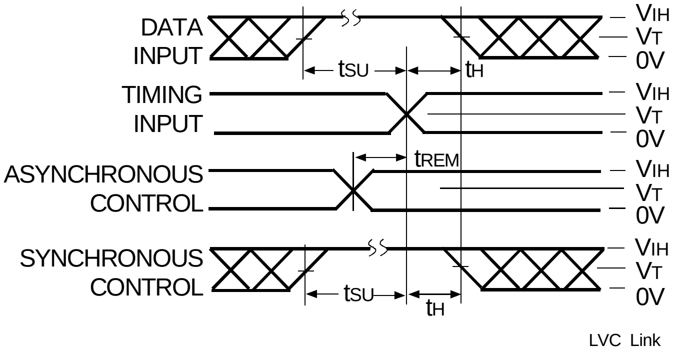


Propagation Delay

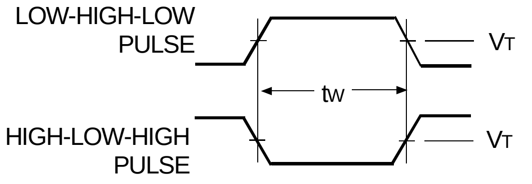


Enable and Disable Times

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

IDT XX	LVC X	XXXX	XX
Temp. Range	Bus-Hold	Device Type	Package

SO	Small Outline IC (gull wing)
PY	Shrink Small Outline Package
Q	Quarter Size Small Outline Package
PG	Thin Shrink Small Outline Package
543A	Octal Registered Transceiver with 3-State Outputs, ±24mA
Blank	No Bus-hold
74	–40°C to +85°C

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