

P54/74FCT841A/B – (P54/74PCT841A/B) P54/74FCT843A/B – (P54/74PCT843A/B) BUS INTERFACE LATCHES

★ FEATURES

- Function, Pinout and Drive Compatible with the FCT, F and AM29841/843 Logic
- FCT-A speed at 9.0ns max. (Com'I)
FCT-B speed at 6.5ns max. (Com'I)
- CMOS V_{OH} Levels for Low Power Consumption
— Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 48 mA Sink Current (Com'I), 32 mA (MII)
15 mA Source Current (Com'I), 12 mA (MII)
- Buffered Common Clear and Preset Input
- High Speed Parallel Latches
- Buffered Common Latch Enable Input
- Manufactured In 0.8 micron PACE Technology™

★ DESCRIPTION

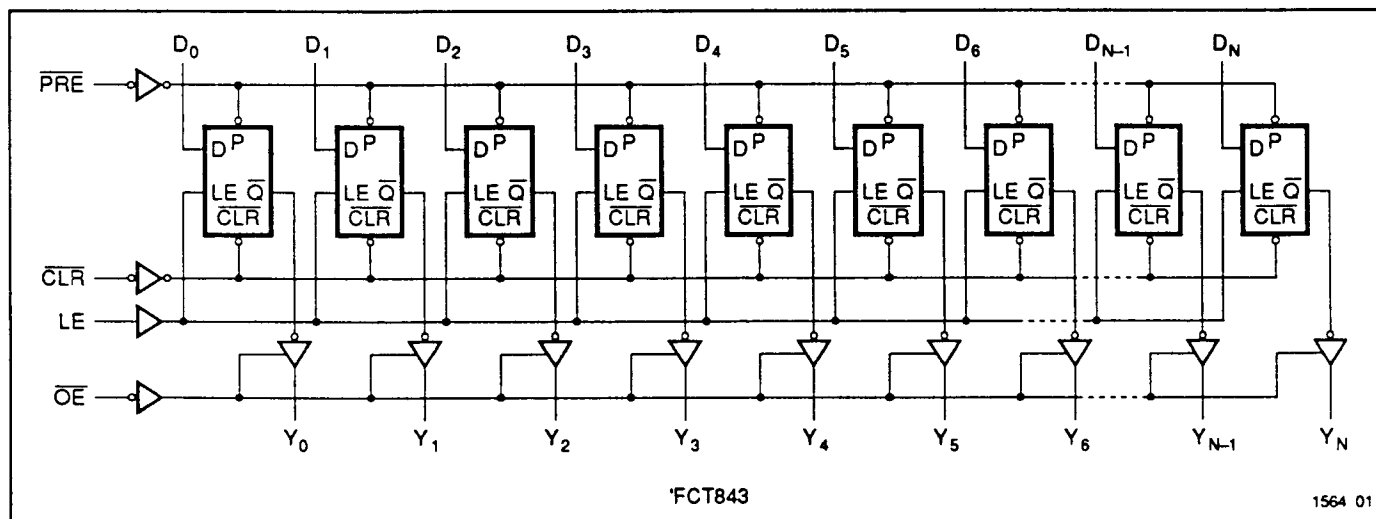
The 'FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841 is a buffered 10-bit wide version of the 'FCT373 function. The 'FCT843 is a 9-bit wide buffered latch with Preset (\overline{PRE}) and Clear (\overline{CLR}) controls making it ideal for parity bus interfacing in high-performance systems.

The 'FCT800 high performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The 'FCT840 interface family are manufactured using PACE Technology which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picosecond loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

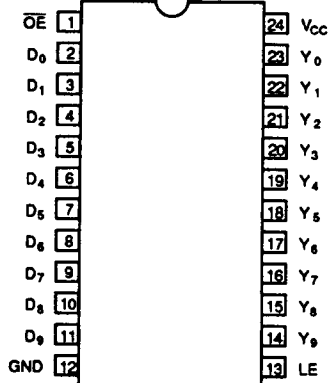
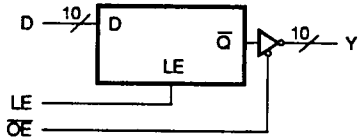
★ FUNCTIONAL BLOCK DIAGRAM



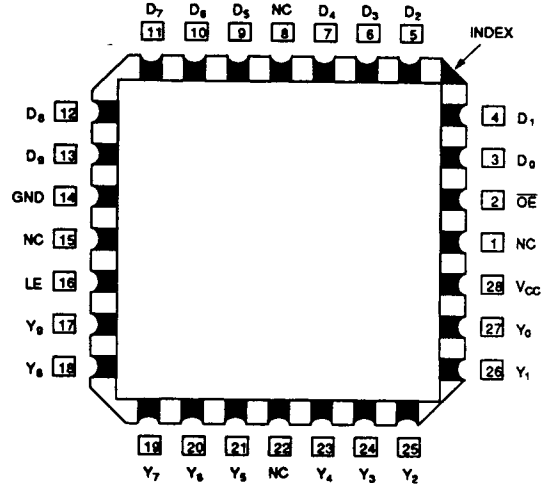
LOGIC SYMBOLS

PIN CONFIGURATIONS

'FCT841 (10-Bit Latch)



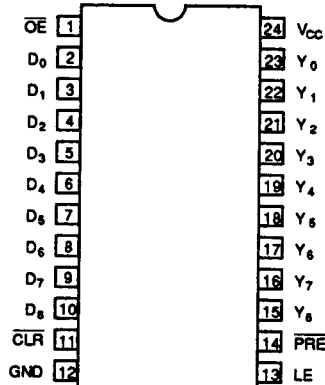
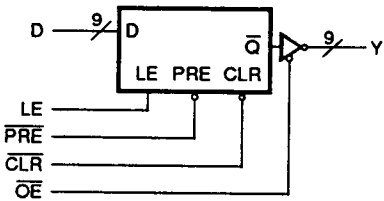
DIP (D4,P4)
SOIC (S4)



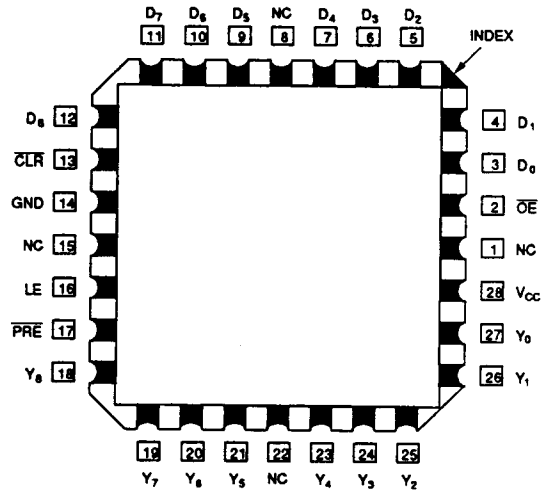
LCC (L5-1)

1564 02

'FCT843 (9-Bit Latch)



DIP (D4,P4)
SOIC (S4)



LCC (L5-1)

1564 03

PIN DESCRIPTION

Name	I/O	Description
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is low, the outputs are LOW if $\overline{\text{OE}}$ is LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the latch.
D_1	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_1	O	The three-state latch outputs.
$\overline{\text{OE}}$	I	The output enable control. When $\overline{\text{OE}}$ is LOW, the outputs are enabled. When $\overline{\text{OE}}$ is HIGH, the outputs Y_1 are in the high-impedance (off) state.
$\overline{\text{PRE}}$	I	Preset line. When $\overline{\text{PRE}}$ is LOW, the outputs are HIGH if $\overline{\text{OE}}$ is LOW. Preset overrides $\overline{\text{CLR}}$.

1564 Tbl 01

FUNCTION TABLES[§]
FCT841/843

Inputs					Internal	Outputs	Function
$\overline{\text{CLR}}$	$\overline{\text{PRE}}$	$\overline{\text{OE}}$	LE	D_1	O_1	Y_1	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

§ H = HIGH, L = LOW, X = Don't care, NC = No Change, Z = High Impedance.

1564 Tbl 02

ABSOLUTE MAXIMUM RATINGS^(1,2)

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _A	Ambient Temperature Under Bias	-65 to +135	°C
V _{CC}	V _{CC} Potential to Ground	-0.5 to +7.0	V
I _{IN}	Input Current	-30 to +5.0	mA

Notes:

- Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature-range.

1564 Tbl 05

Symbol	Parameter	Value	Unit
I _{OUTPUT}	Current Applied to Output	120	mA
V _{IN}	Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{OUT}	Voltage Applied to Output	-0.5 to V _{CC} + 0.5	V

1564 Tbl 04

- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	-55°C	+125°C
Commercial	0°C	+70°C

1564 Tbl 05

Supply Voltage (V _{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1564 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	Min	Typ ¹	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		
V _{IL}	Input LOW Voltage			0.8	V		
V _H	Hysteresis		0.35		V		All inputs
V _{CD}	Input Clamp Diode Voltage		-0.7	-1.2	V	MIN	I _{IN} = -18mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V		V _{CC} - 0.2	V _{CC}	V	I _{OH} = -32μA
		Military/Commercial (CMOS)		V _{CC} - 0.2	V _{CC}	V	MIN I _{OH} = -300μA
		Military (TTL)		2.4	4.3	V	MIN I _{OH} = -12mA
		Commercial (TTL)		2.4	4.3	V	MIN I _{OH} = -15mA
V _{OL}	Output LOW Voltage	V _{CC} = 3V, V _{IN} = 0.2V, or V _{CC} - 0.2V			GND	0.2	V I _{OL} = 300μA
		Military/Commercial (CMOS)			GND	0.2	V MIN I _{OL} = 300μA
		Military (TTL)			0.3	0.5	V MIN I _{OL} = 32mA
		Commercial (TTL)			0.3	0.5	V MIN I _{OL} = 48mA
		Commercial (TTL)			0.3	0.5	V MIN I _{OL} = 64mA
I _{IH}	Input HIGH Current			5	μA	MAX	V _{IN} = V _{CC}
I _{IL}	Input LOW Current			-5	μA	MAX	V _{IN} = GND
I _{IH}	Input HIGH Current ³			5	μA	MAX	V _{IN} = 2.7V
I _{IL}	Input LOW Current ³			-5	μA	MAX	V _{IN} = 0.5V
I _{OZH}	Off State I _{OUT} HIGH-Level Output Current			10	μA	MAX	V _{OUT} = V _{CC}
I _{OZL}	Off State I _{OUT} LOW-Level Output Current			-10	μA	MAX	V _{OUT} = GND
I _{OZH}	Off State I _{OUT} HIGH-Level Output Current ³			10	μA	MAX	V _{OUT} = 2.7V
I _{OZL}	Off State I _{OUT} LOW-Level Output Current ³			-10	μA	MAX	V _{OUT} = 0.5V
I _{OS}	Output Short Circuit Current ²	-75	-120	-225	mA	MAX	V _{OUT} = 0.0V
C _{IN}	Input Capacitance ³		5	10	pF	MAX	All inputs
C _{OUT}	Output Capacitance ³		9	12	pF	MAX	All outputs

1564 Tbl 07

Notes:

- Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

- This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ ¹	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	.003	0.3	mA	$V_{CC} = \text{MAX}$, $V_{IN} \leq 0.2V$ or $f_1 = 0$, Outputs Open
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)		2.0	mA	$V_{CC} = \text{MAX}$, $V_{in} = 3.4V^2$, $f = 0$, Outputs Open
I_{CCD}	Dynamic Power Supply Current ³	0.15	0.25	mA/ mHz	$V_{CC} = \text{MAX}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		1.7	4.0	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10\text{MHz}$, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current ⁵	2.0	5.0	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1 = 10\text{mHz}$, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
		3.2	6.5 ⁴	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5 ⁴	mA	$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$
					$V_{CC} = \text{MAX}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1 = 2.5\text{MHz}$, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$

Notes:

- Typical values are at $V_{CC} = 3.3V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 2.7V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o/2 + f_1 N_1)$$

$$I_{CC} = \text{Quiescent Current with CMOS input levels}$$

$$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 2.7V \text{)}$$

- D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_o = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_1 = Input Frequency
 N_1 = Number of Inputs at f_1
 All currents are in milliamps and all frequencies are in megahertz.

1564 Tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

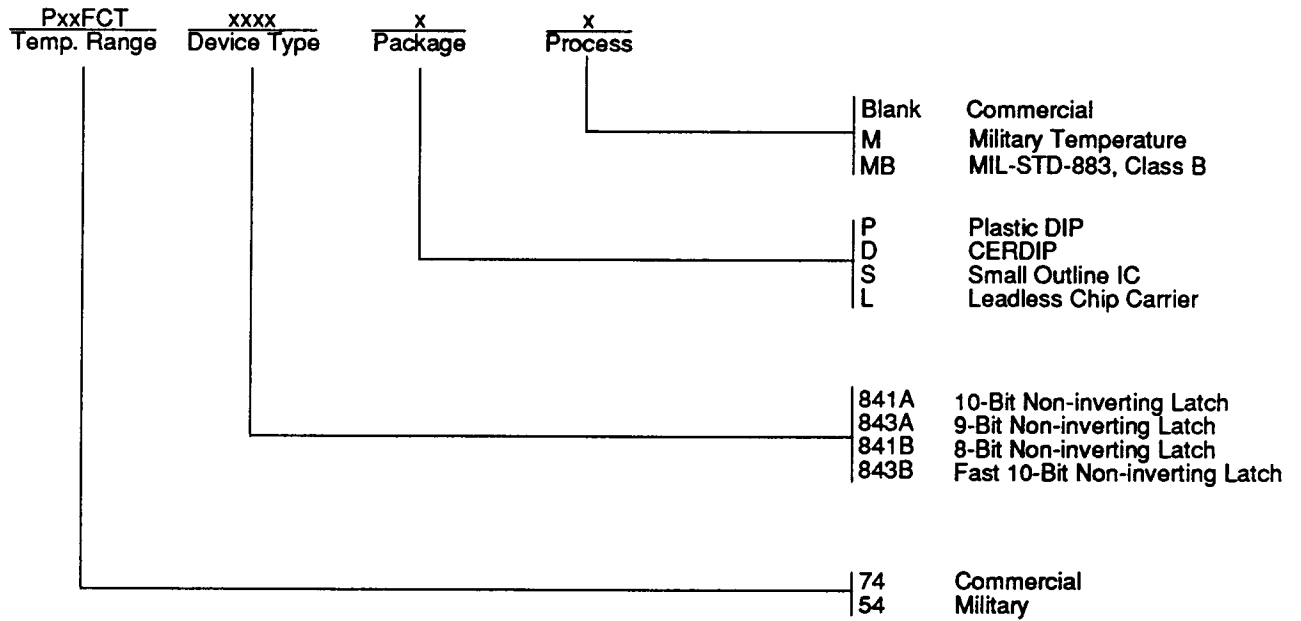
Sym.	Parameter	Test Conditions ¹	'FCT841A/843A				'FCT841B/843B			
			MIL		COM'L		MIL		COM'L	
			Min. ²	Max.	Min. ²	Max.	Min. ²	Max.	Min. ²	Max.
t_{PLH} t_{PHL}	Propagation Delay D_1 to Y_1 (LE = HIGH)	$C_L = 50\text{pF}$ $R_L = 500\Omega$		10.0		9.0		7.5		6.5
		$C_L = 300\text{pF}^3$ $R_L = 500\Omega$		15.0		13.0		15.0		13.0
t_{SU}	Data to LE Set-up Time	$C_L = 50\text{pF}$	2.5		2.5		2.5		2.5	
t_H	Data to LE Hold Time	$R_L = 500\Omega$	3.0		2.5		2.5		2.5	
t_{PLH} t_{PHL}	Propagation Delay LE to Y_1	$C_L = 50\text{pF}$ $R_L = 500\Omega$		13.0		12.0		10.5		8.0
		$C_L = 300\text{pF}^3$ $R_L = 500\Omega$		20.0		16.0		18.0		15.5
t_{PLH}	Propagation Delay \overline{PRE} to Y_1	$C_L = 50\text{pF}$ $R_L = 500\Omega$		14.0		12.0		10.0		8.0
t_{REH}	Recovery Time \overline{PRE} to Y_1			17.0		14.0		13.0		10.0
t_{PHL}	Propagation Delay \overline{CLR} to Y_1			14.0		13.0		11.0		10.0
t_{REH}	Recovery Time \overline{CLR} to Y_1			17.0		14.0		10.0		10.0
t_W	LE Pulse Width ³		HIGH	5.0		4.0		4.0		4.0
t_W	\overline{PRE} Pulse Width ³		LOW	7.0		5.0		4.0		4.0
t_W	\overline{CLR} Pulse Width ³		LOW	5.0		4.0		4.0		4.0
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} to Y_1		$C_L = 50\text{pF}$ $R_L = 500\Omega$		13.0		11.5		8.5	
		$C_L = 300\text{pF}^3$ $R_L = 500\Omega$		25.0		23.0		15.0		14.0
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OE} to Y_1	$C_L = 5\text{pF}^3$ $R_L = 500\Omega$		9.0		7.0		6.5		6.0
		$C_L = 50\text{pF}$ $R_L = 500\Omega$		10.0		8.0		7.5		7.0

1564 Tbl 09

Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameters are guaranteed but not tested.

ORDERING INFORMATION



1564 05