



16,384 x 4 Static R/W RAM  
Separate I/O

Features

- Automatic power-down when deselected
- Transparent write (7C161)
- CMOS for optimum speed/power
- High speed  
— 15 ns  $t_{AA}$
- Low active power  
— 633 mW
- Low standby power  
— 220 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge.

Functional Description

The CY7C161 and CY7C162 are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ( $CE_1$ ,  $CE_2$ ) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 65% when deselected.

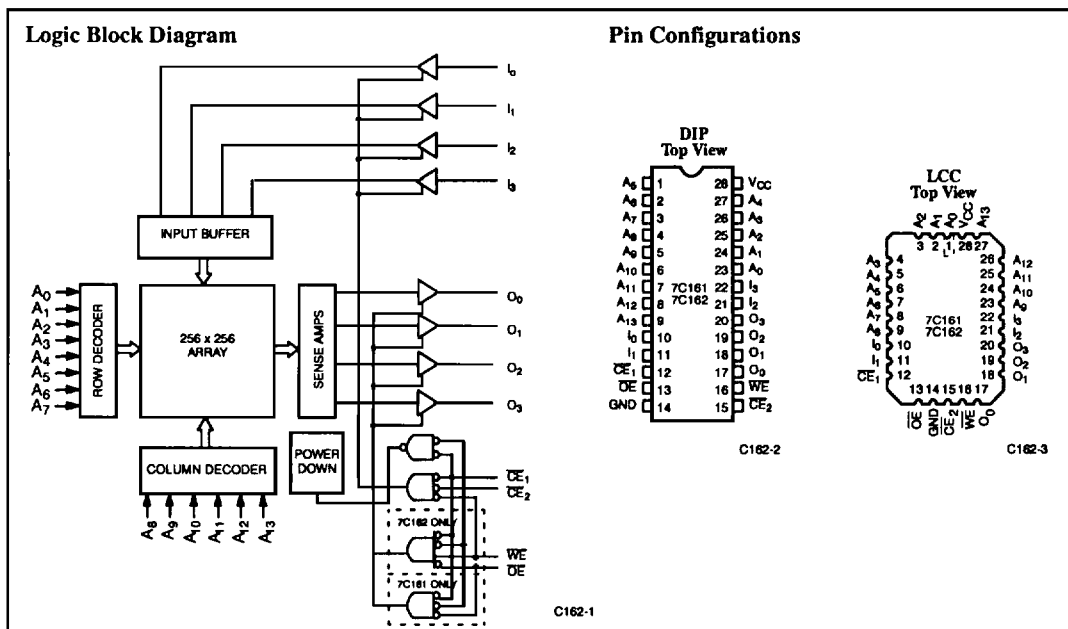
Writing to the device is accomplished when the chip enable ( $CE_1$ ,  $CE_2$ ) and write enable ( $WE$ ) inputs are both LOW. Data on the four input pins ( $I_0$  through  $I_3$ ) is written

into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

Reading the device is accomplished by taking the chip enables ( $CE_1$ ,  $CE_2$ ) LOW while write enable ( $WE$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ( $WE$ ) is LOW (7C162 only), or one of the chip enables ( $CE_1$ ,  $CE_2$ ) are HIGH.

A die coat is used to insure alpha immunity.



Selection Guide<sup>(1)</sup>

	7C161-10 7C162-10	7C161-12 7C162-12	7C161-15 7C162-15	7C161-20 7C162-20	7C161-25 7C162-25	7C161-35 7C162-35	7C161-45 7C162-45
Maximum Access Time (ns)	10	12	15	20	25	35	45
Maximum Operating Current (mA)	160	160	115	80	70	70	50
Maximum Standby Current (mA)	40/20	40/20	40/20	40/20	20/20	20/20	20/20

Shaded areas indicate advanced information.

Note:

1. For military specifications, see the CY7C161A/CY7C162A datasheet.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

### Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C161-10 7C162-10		7C161-12 7C162-12		7C161-15 7C162-15		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	-3.0	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-350		-350		-350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		160		160		115	mA
I <sub>SB1</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , Min. Duty Cycle = 100%		40		40		40	mA
I <sub>SB2</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		20		20		20	mA

Shaded areas indicate advanced information.

**Electrical Characteristics** Over the Operating Range (continued)

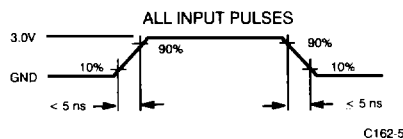
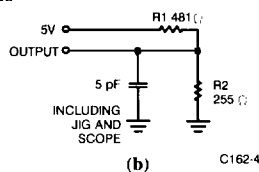
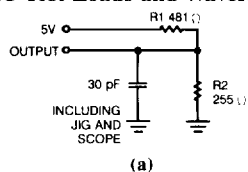
Parameters	Description	Test Conditions	7C161-20 7C162-20		7C161-25,35 7C162-25,35		7C161-45 7C162-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OIH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = - 4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		- 350		- 350		- 350	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		80		70		50	mA
I <sub>SB1</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> Min. Duty Cycle = 100%		40		20		20	mA
I <sub>SB2</sub>	Automatic $\overline{CE}_1$ Power-Down Current	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		20		20		20	mA

**Capacitance<sup>[4]</sup>**

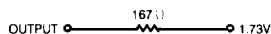
Parameters	Description	Test Conditions	Max.	Units
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

- V<sub>IL</sub> min. = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


Equivalent to: THEVENIN EQUIVALENT



**Switching Characteristics Over the Operating Range<sup>5, 6]</sup>**

Parameters	Description	7C161-10 7C162-10		7C161-12 7C162-12		7C161-15 7C162-15		7C161-20 7C162-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	10		12		15		20		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15		20	ns
t <sub>OHA</sub>	Output Hold from Address Change	3		3		3		5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		10		12		10		10	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z		5		7		8		8	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	2		3		3		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7,8]</sup>		5		7		8		8	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
<b>WRITE CYCLE<sup>[9]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	10		12		15		20		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		8		12		15		ns
t <sub>AW</sub>	Address Set-Up to Write End	8		8		12		15		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		8		12		15		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		6		10		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C162)	2		3		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[7,8]</sup> (7C162)		6		6		7		7	ns
t <sub>AWE</sub>	$\overline{WE}$ LOW to Data Valid (7C161)		10		12		15		20	ns
t <sub>ADV</sub>	Data Valid to Output Valid (7C161)		10		12		15		20	ns
t <sub>DLE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns

Shaded areas indicate advanced information.

Switching Characteristics Over the Operating Range<sup>5, 6</sup>

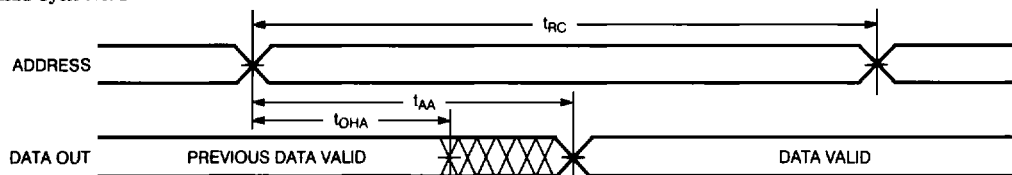
Parameters	Description	7C161–25 7C162–25		7C161–35 7C162–35		7C161–45 7C162–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	25		35		45		ns
t <sub>AA</sub>	Address to Data Valid		25		35		45	ns
t <sub>OHA</sub>	Output Hold from Address Change	5		5		5		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		12		15		20	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z		10		12		15	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	5		5		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7,8]</sup>		10		15		15	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
<b>WRITE CYCLE<sup>[9]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	20		25		40		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	20		25		30		ns
t <sub>AW</sub>	Address Set-Up to Write End	20		25		30		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	WE Pulse Width	15		20		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		15		15		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup> (7C162)	5		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[7,8]</sup> (7C162)		7		10		15	ns
t <sub>AWE</sub>	$\overline{WE}$ LOW to Data Valid (7C161)		25		30		35	ns
t <sub>ADV</sub>	Data Valid to Output Valid (7C161)		20		30		35	ns
t <sub>IDLE</sub>	$\overline{CE}$ LOW to Data Valid		25		30		35	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OIH</sub> and 30-pF load capacitance.
- Both CE<sub>1</sub> and CE<sub>2</sub> are represented by CE in the Switching Characteristics and Waveforms sections.
- At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub> for any given device.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of CE<sub>1</sub> LOW, CE<sub>2</sub> LOW, and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

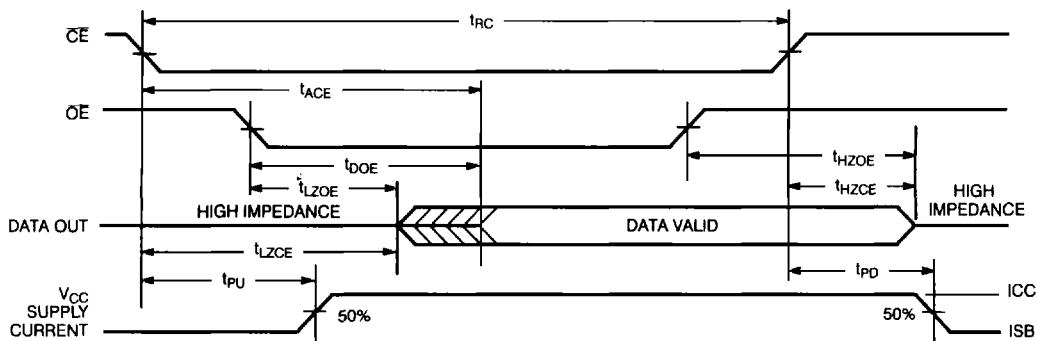
### Switching Waveforms<sup>[8]</sup>

#### Read Cycle No. 1<sup>[10, 11]</sup>



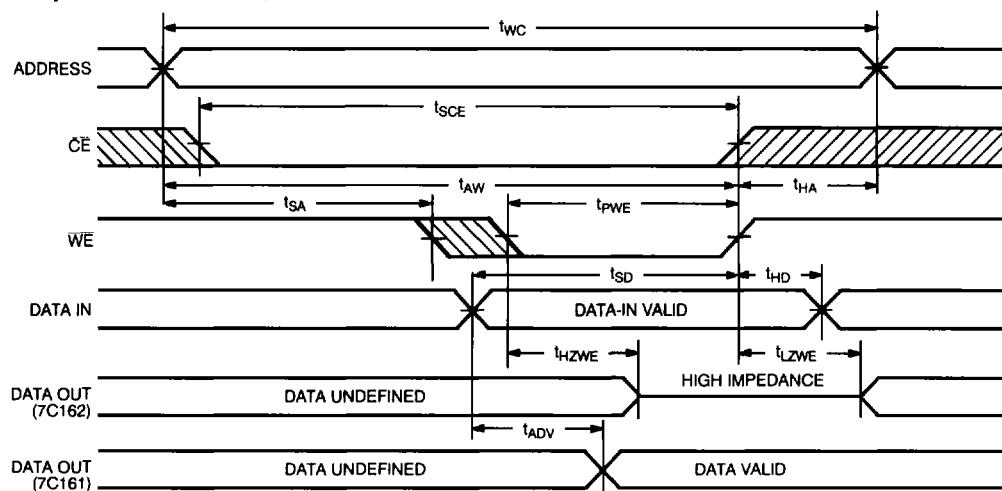
C162.6

#### Read Cycle No. 2<sup>[10, 12]</sup>



C162.7

#### Write Cycle No. 1 (WE Controlled)<sup>[9]</sup>



C162.8

**Notes:**

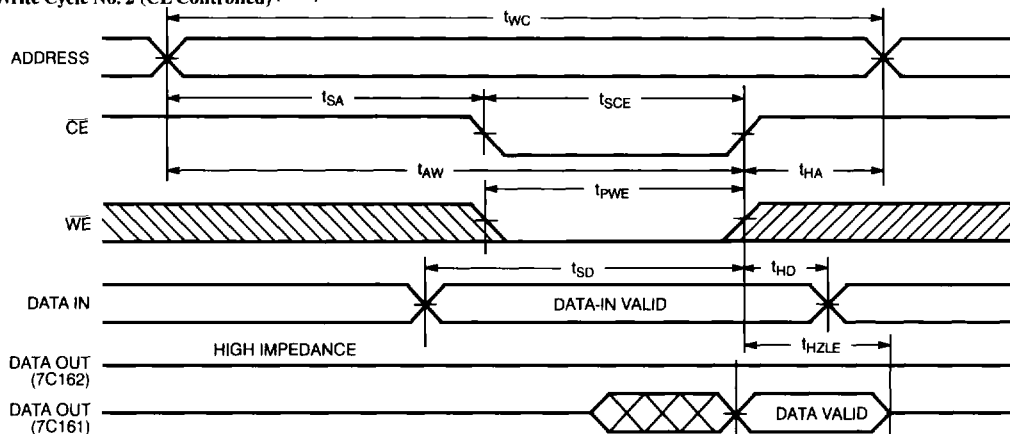
10.  $\overline{WE}$  is HIGH for read cycle.

11. Device is continuously selected,  $\overline{CE}_1, \overline{CE}_2 = V_{IL}$ .

12. Address valid prior to or coincident with  $\overline{CE}_1, \overline{CE}_2$  transition LOW.

Switching Waveforms<sup>[8]</sup> (continued)

Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[9, 13]</sup>

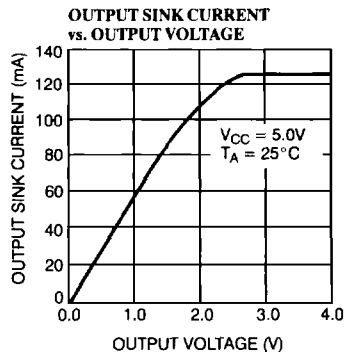
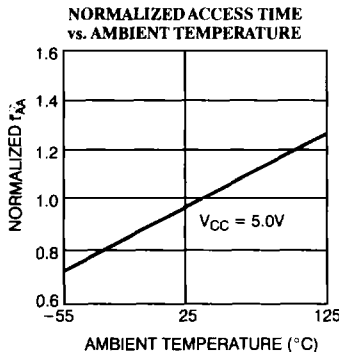
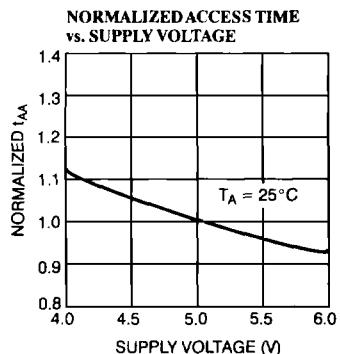
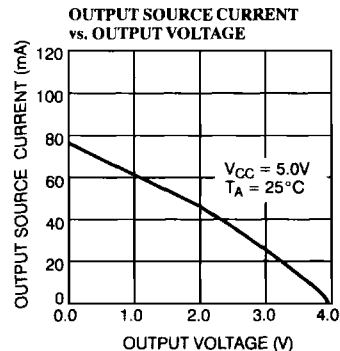
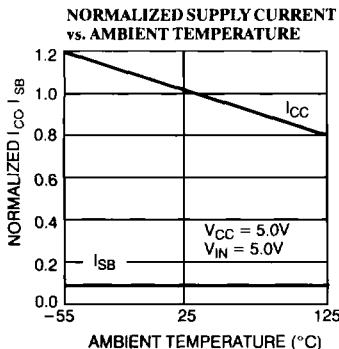
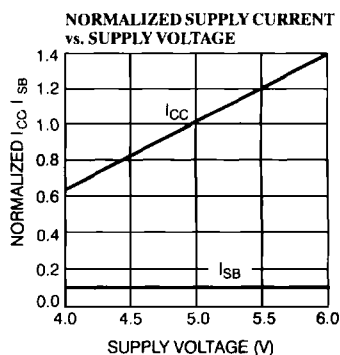


C162-9

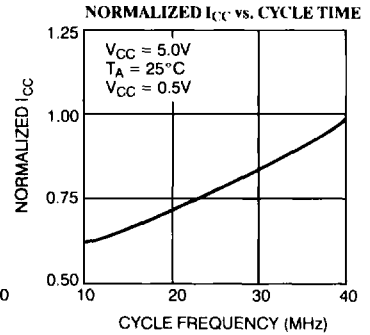
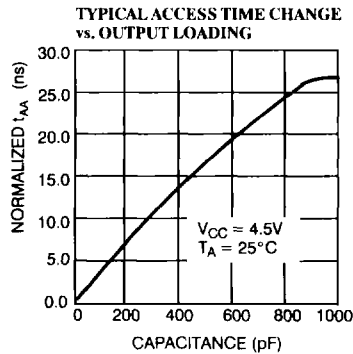
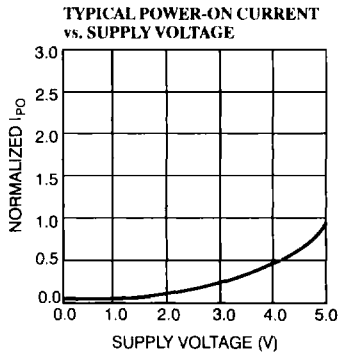
Note:

13. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state (7C162 only).

Typical DC and AC Characteristics



**Typical DC and AC Characteristics (continued)**



**Address Designators**

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27



**Ordering Information**

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C161-10PC	P21	Commercial
	CY7C161-10VC	V21	
	CY7C161-10DC	D22	
	CY7C161-10LC	L54	
12	CY7C161-12PC	P21	Commercial
	CY7C161-12VC	V21	
	CY7C161-12DC	D22	
	CY7C161-12LC	L54	
15	CY7C161-15PC	P21	Commercial
	CY7C161-15VC	V21	
	CY7C161-15DC	D22	
	CY7C161-15LC	L54	
20	CY7C161-20PC	P21	Commercial
	CY7C161-20VC	V21	
	CY7C161-20DC	D22	
	CY7C161-20LC	L54	
25	CY7C161-25PC	P21	Commercial
	CY7C161-25VC	V21	
	CY7C161-25DC	D22	
	CY7C161-25LC	L54	
35	CY7C161-35PC	P21	Commercial
	CY7C161-35VC	V21	
	CY7C161-35DC	D22	
	CY7C161-35LC	L54	
45	CY7C161-45PC	P21	Commercial
	CY7C161-45VC	V21	
	CY7C161-45DC	D22	
	CY7C161-45LC	L54	

Shaded areas indicate advanced information.

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Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C162-10PC	P21	Commercial
	CY7C162-10VC	V21	
	CY7C162-10DC	D22	
	CY7C162-10LC	L54	
12	CY7C162-12PC	P21	Commercial
	CY7C162-12VC	V21	
	CY7C162-12DC	D22	
	CY7C162-12LC	L54	
15	CY7C162-15PC	P21	Commercial
	CY7C162-15VC	V21	
	CY7C162-15DC	D22	
	CY7C162-15LC	L54	
20	CY7C162-20PC	P21	Commercial
	CY7C162-20VC	V21	
	CY7C162-20DC	D22	
	CY7C162-20LC	L54	
25	CY7C162-25PC	P21	Commercial
	CY7C162-25VC	V21	
	CY7C162-25DC	D22	
	CY7C162-25LC	L54	
35	CY7C162-35PC	P21	Commercial
	CY7C162-35VC	V21	
	CY7C162-35DC	D22	
	CY7C162-35LC	L54	
45	CY7C162-45PC	P21	Commercial
	CY7C162-45VC	V21	
	CY7C162-45DC	D22	
	CY7C162-45LC	L54	

Shaded areas indicate advanced information.

**2**  
**SRAMs**