



PI74FCT16373T
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Product Features:

Common Features:

- PI74FCT16373T and PI74FCT162373T have high current drive and four speed grades.
 Standard speeds at 8.0 ns max.
 "A" speeds at 5.2 ns max.
 "C" speeds at 4.2 ns max.
 "D" speeds at 3.8 ns max.
 "E" speeds at 3.4 ns max.
- $V_{CC} = 5\text{ V} \pm 10\%$
- Hysteresis on all inputs
- Packaged in 48-pin plastic TSSOP and SSOP

PI74FCT16373T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit "live insertion"
- Typical V_{OLP} (Output Ground Bounce) $< 1.0\text{ V}$ at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PI74FCT162373T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6\text{ V}$ at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

Fast CMOS 16-Bit Transparent Latches

Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

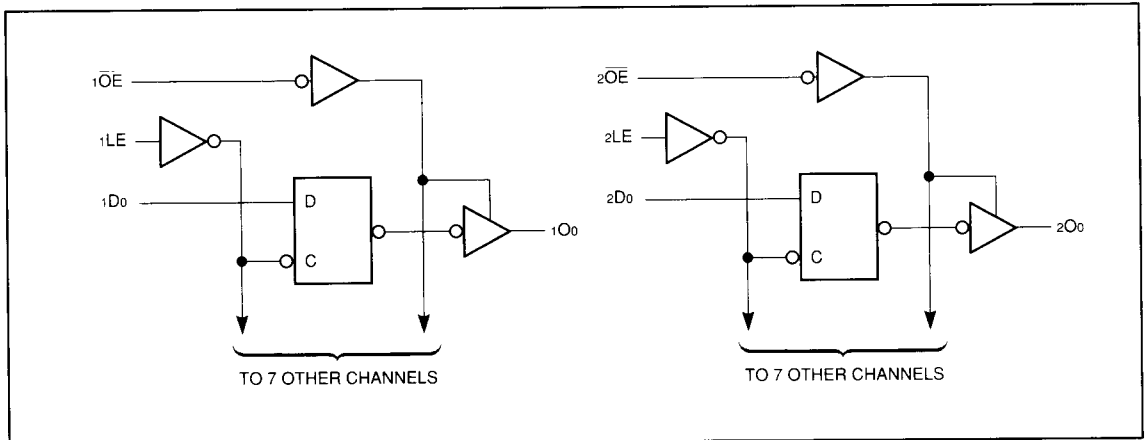
The PI74FCT16373T and PI74FCT162373T are 16-bit transparent latches designed with 3-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

The PI74FCT16373T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The PI74FCT162373T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

All products are available in 48-pin 240 mil wide plastic TSSOP and 300 mil wide plastic SSOP packages.

Logic Block Diagram



Product Pin Description

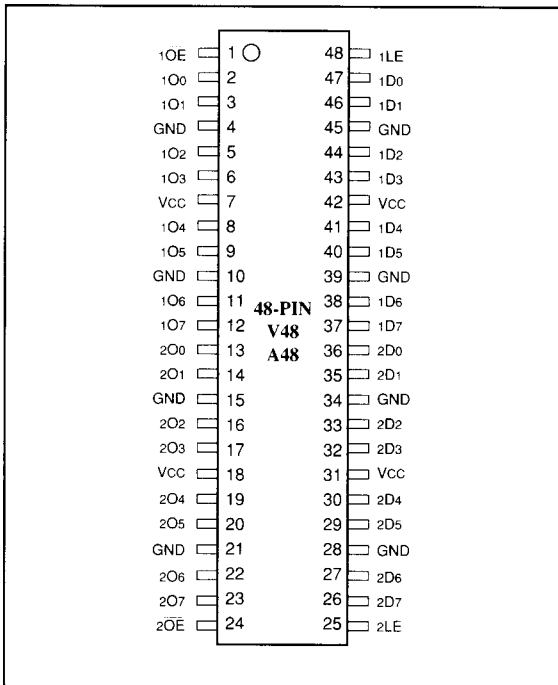
Pin Name	Description
xOE	Output Enable Inputs (Active LOW)
xLE	Latch Enable Inputs (Active HIGH)
xDx	Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

Truth Table

Inputs ⁽¹⁾			Outputs ⁽¹⁾
xDx	xOE	xLE	xOx
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE: 1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to Vcc
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			±5	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			±5	μA
I _{OZH}	High Impedance	V _{CC} = Max., V _{OUT} = 2.7 V			±10	μA
I _{OZL}	Output Current	V _{CC} = Max., V _{OUT} = 0.5 V			±10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5 V	-50		-180	mA
V _H	Input Hysteresis			100		mV

PI74FCT16373T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.2	0.55	V	
I _{OFF}	Power Down Disable	V _{CC} = 0 V, V _{IN} or V _{OUT} ≤ 4.5 V			±100	μA	

PI74FCT162373T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5 V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5 V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5 V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5 V ⁽³⁾	-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0 V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0 V	5.5	8	pF

Notes:

- For conditions show as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{cc}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		2	500	μA
ΔI _{cc}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4 V ⁽³⁾		0.5	1.5	mA
I _{ccd}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open x \overline{OE} = GND, xLE = V _{CC} One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		60	100	μA/ MHz
I _c	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle x \overline{OE} = GND, xLE = V _{CC} One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		0.7	2.5 ⁽⁵⁾	mA
			V _{IN} = 3.4 V V _{IN} = GND		0.9	3.3 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle x \overline{OE} = GND, xLE = V _{CC} 16 Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND		2.5	5.5 ⁽⁵⁾	
			V _{IN} = 3.4 V V _{IN} = GND		6.5	17.5 ⁽⁵⁾	

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0 V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{cc} formula. These limits are guaranteed but not tested.

$$I_c = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_c = I_{\text{CC}} + \Delta I_{\text{CC}} D_{\text{HNT}} + I_{\text{CCD}} (f_{\text{CP}}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4 V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16373T Switching Characteristics over Operating Range

Preliminary

Parameters	Description	Conditions ⁽¹⁾	'16373T		'16373AT		'16373CT		'16373DT		'16373ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay xDx to xOx	Cl = 50 pF Rl = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	3.7	ns
tPZH	Output Enable Time		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
tPZL	Output Disable Time		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.0	—	1.0	—	ns
tW	xLE Pulse Width HIGH		6.0	—	5.0	—	5.0	—	3.0	—	3.0 ⁽⁴⁾	—	ns
tSK(O)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162373T Switching Characteristics over Operating Range

Preliminary

Parameters	Description	Conditions ⁽¹⁾	'162373T		'162373AT		'162373CT		'162373DT		'162373ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH	Propagation Delay xDx to xOx	Cl = 50 pF Rl = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	3.7	ns
tPZH	Output Enable Time		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
tPZL	Output Disable Time		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	1.5	—	1.0	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.0	—	1.0	—	ns
tW	xLE Pulse Width HIGH		6.0	—	5.0	—	5.0	—	3.0	—	3.0 ⁽⁴⁾	—	ns
tSK(O)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.