CYPRESS *ADVANCED INFORMATION* **CY7C1019**

128K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options**

Functional Description

The CY7C1019 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption significantly when deselected.

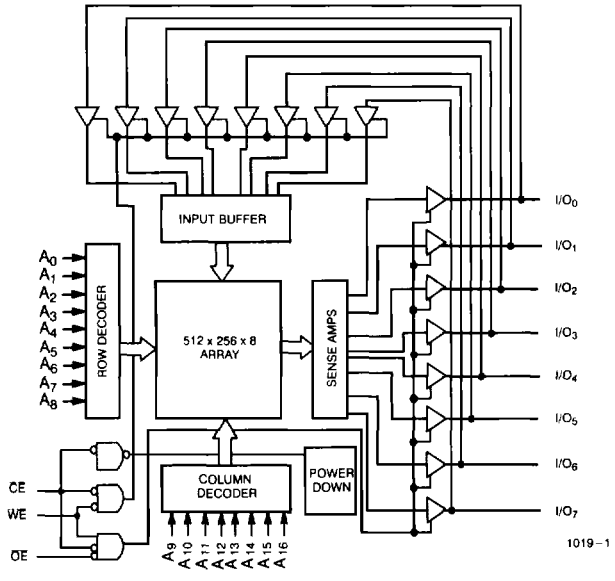
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

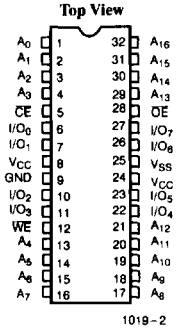
The CY7C1019 is available in standard 400-mil-wide SOJs.

Logic Block Diagram



Pin Configurations

SOJ
Top View



Selection Guide

		7C1019-10	7C1019-12	7C1019-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	195	185	170
	Military		195	180
Maximum Standby Current (mA)	Commercial	50	45	40
	Military		50	40

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